

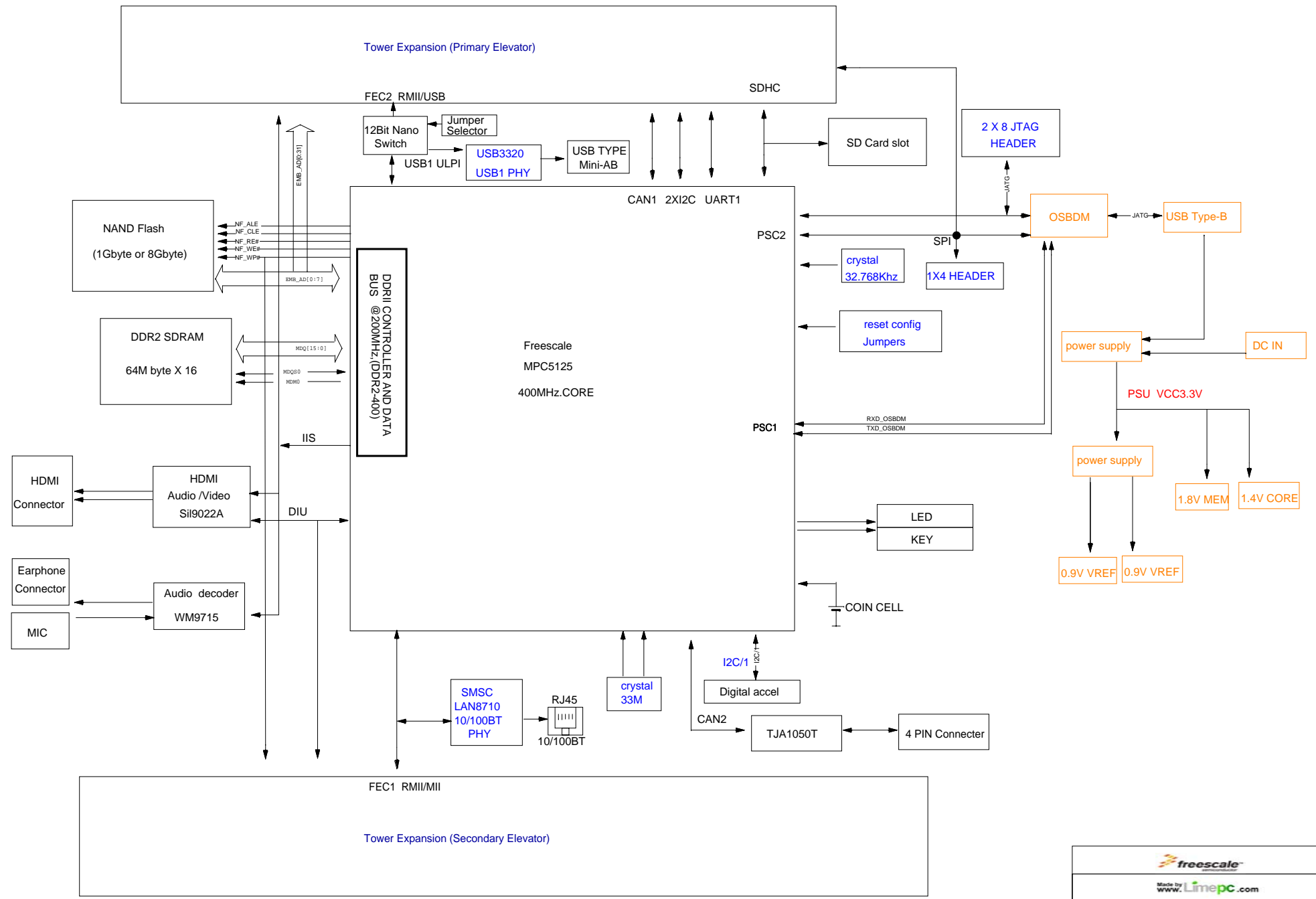


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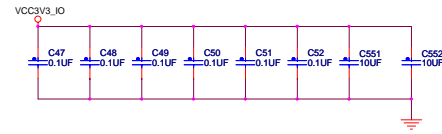
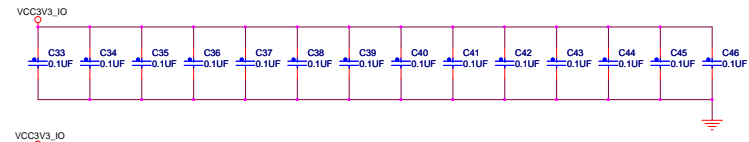
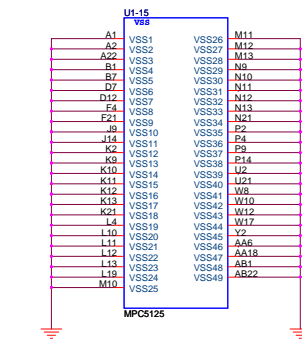
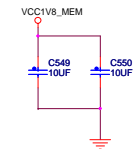
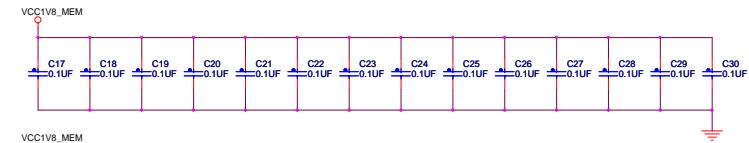
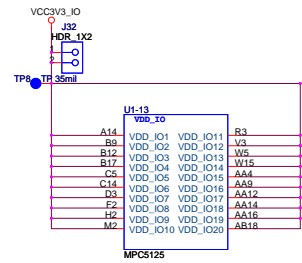
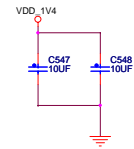
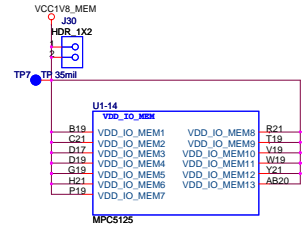
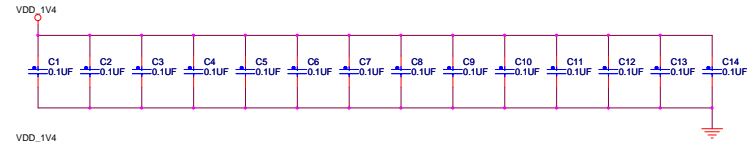
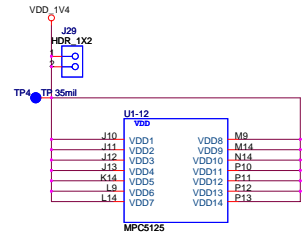


BLOCK DIAGRAM



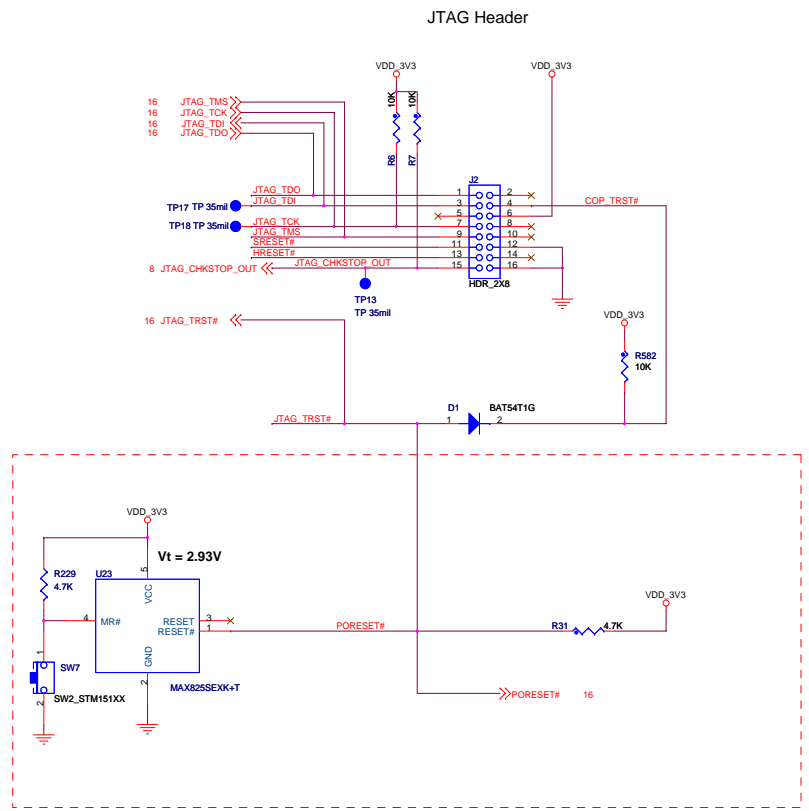
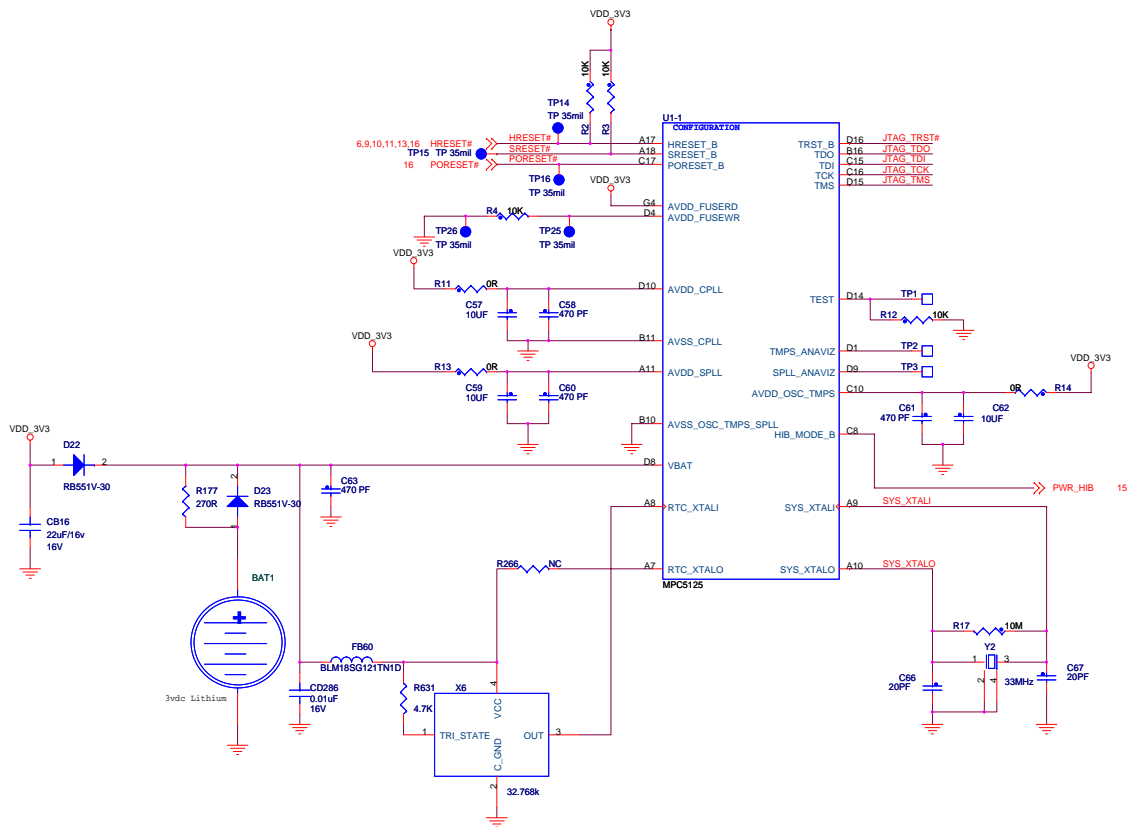


MPC5125 POWER AND DECAPS





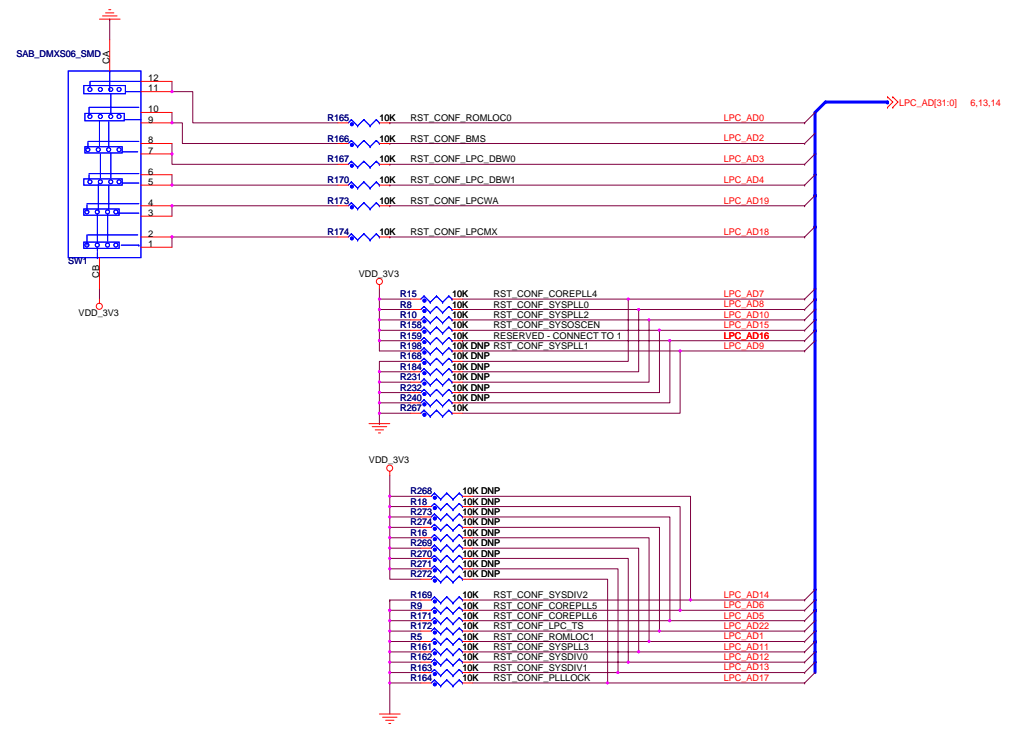
MPC5125 - CONFIGURATION





RESET CONFIGURATION JUMPERS

RST FUNCTION	LPC PIN	DESCRIPTION
RST_CONF_LOC	LPC_AD[1:0] Default 01	Selects boot device 00 LPC boot 01 NAND (NFC) boot2 10 Factory Test mode, use TPR port at LPC 11 Factory Test mode, use TPR port at DIU
RST_CONF_BMS	LPC_AD[2] Default 1	Boot mode select: Selects e300 boot vector and configures default value for LPC CS0 or NFC base address.
RST_CONF_LPC_DBW	LPC_AD[4:3] Default 00	LPC Data Port Size 00 8 bit 10 Reserved 01 16 bit 11 32 bit
RST_CONF_COREPLL	LPC_AD[7:5] 2.0 : 1 Default 100	Core PLL Multiply factor See clock module for programming options
RST_CONF_SYSPLL	LPC_AD[11:8] 24 : 1 Default 0101	System PLL Multiply factor See clock module for programming options
RST_CONF_SYSDIV	LPC_AD[14:12] 2 Default 000	System PLL divider ratio See clock module for programming options
RST_CONF_SYSOSCEN	LPC_AD[15] Default 1	Oscillator Bypass Mode 0 System Oscillator bypass mode 1 System Oscillator mode
RST_CONF_LONGFB	LPC_AD[16] Default 1	Reserved (must be tied to logic high)
RST_CONF_PLLLOCK	LPC_AD[17] Default 0	Use PLL lock signal 1 use counter 0 use PLL lock signal
RST_CONF_LPCMX	LPC_AD[18] Default 0	LPC Mux mode configuration 0 Non-multiplexed mode 1 Multiplexed mode
RST_CONF_LPCWA	LPC_AD[19] Default 1	LPC Word/Byte address 1 Address is interpreted as byte address 0 Address is interpreted as word address
RST_CONF_LPC_TS	LPC_AD[22] Default 0	Use LPC_TS, LPC_TSIZE[1:0] if boot from LPC 1 use LPC_TS, LPC_TSIZE[1:0] if boot from LPC 0 set LPC_TS, LPC_TSIZE[1:0] is set to one if boot from LPC



Parameter	BMS=0(Boot low)	BMS=1(Boot high)
e300 Boot Vector	0 X 00000100	0 X FFF00100

Parameter	BMS=0(Boot low)	BMS=1(Boot high)
LPC CSBOOT Start	0 X 00000000	0 X FFF00000
LPC CSBOOT End	0 X 0007FFFF	0 X FFFFFFFF
NFC Base Address	0 X 00000000	0 X FFF00000

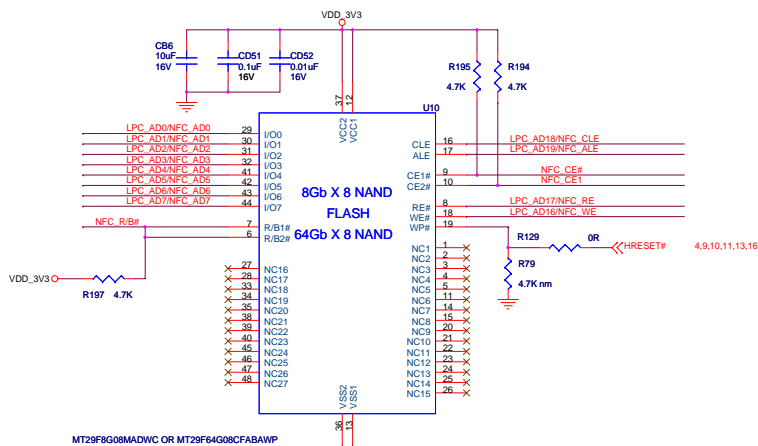
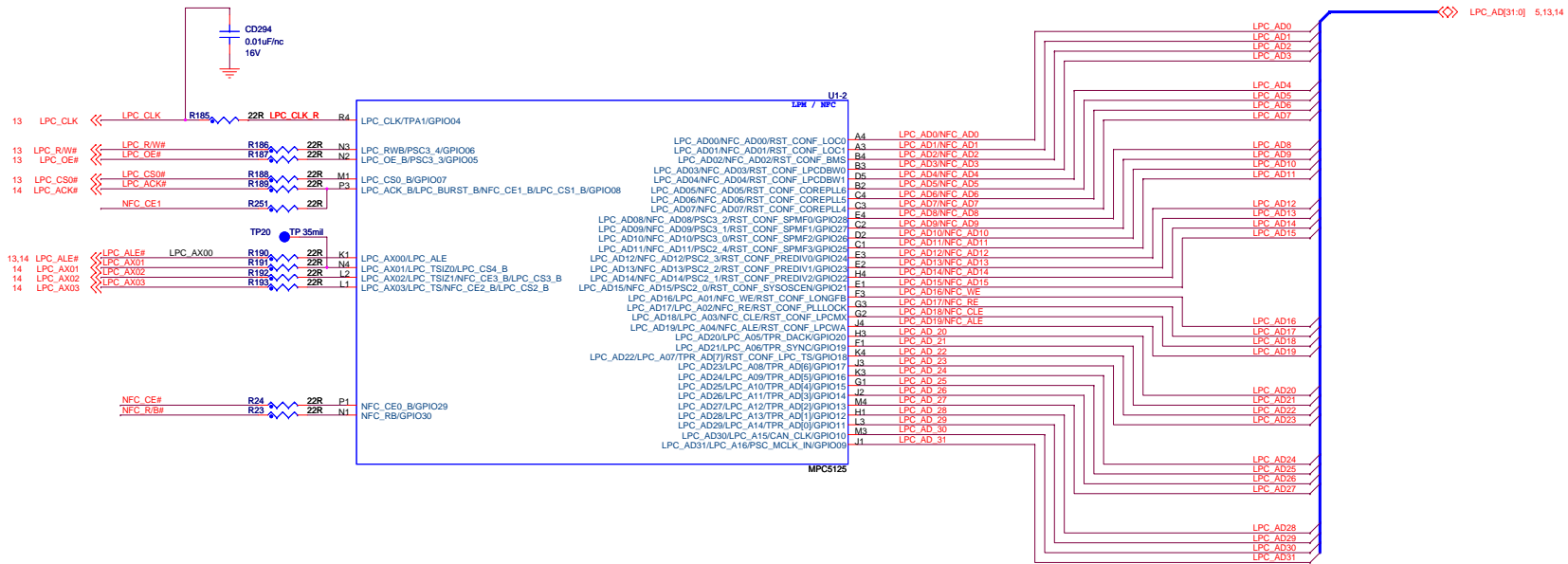
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RESET CONFIG JUMPERS

File		
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C	TWR-MPC5125	v2.1
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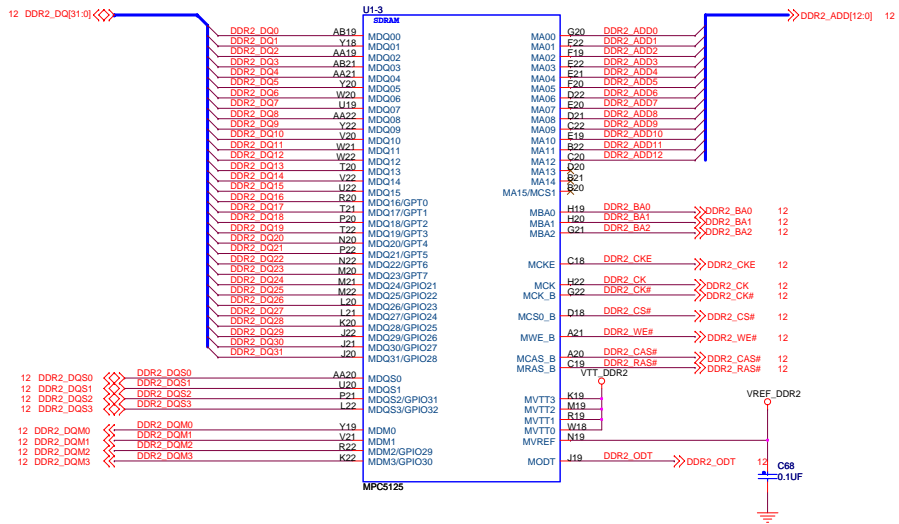


MPC5125 - LPC AND NFC

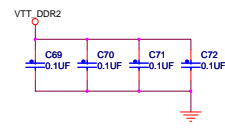




MPC5125 - DDR-2 MEMORY INTERFACE

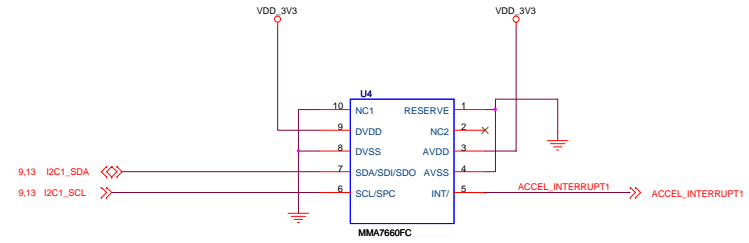
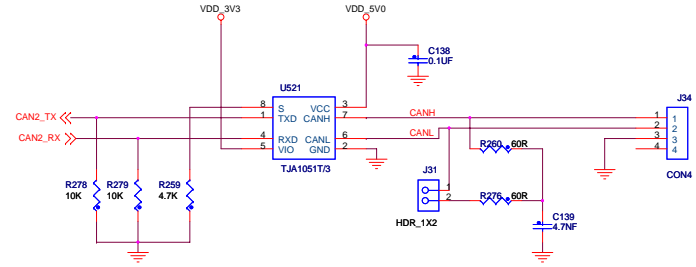
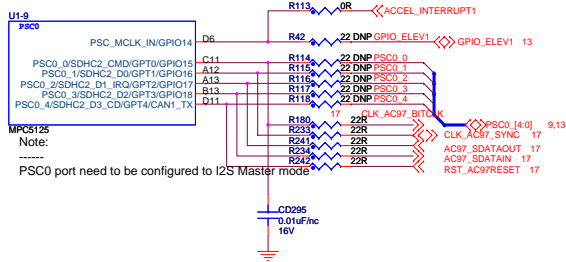
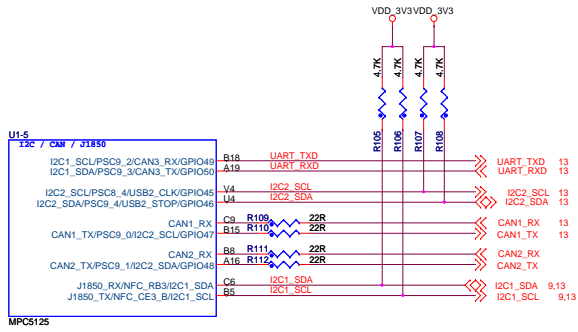
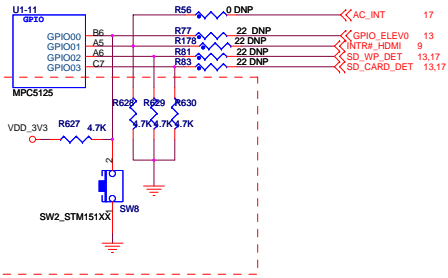
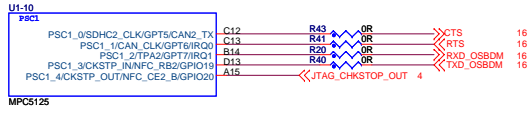


Note:
 1. Place the Voltage Divider and the decap near the Pin
 2. Provide Groundguard to the Vref Line





MPC5125 - ACCEL INTERFACE



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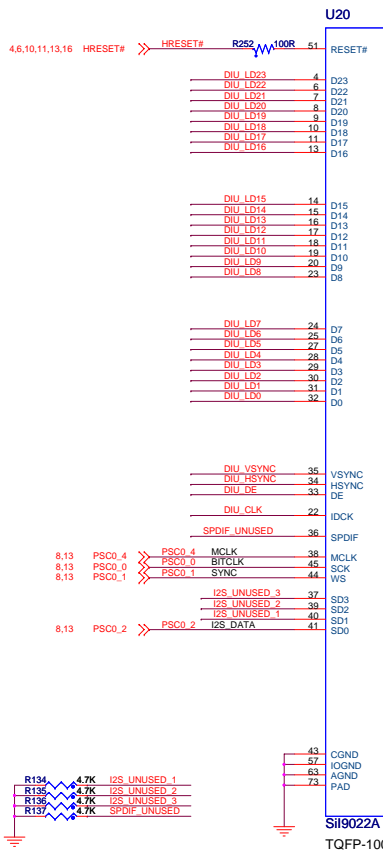
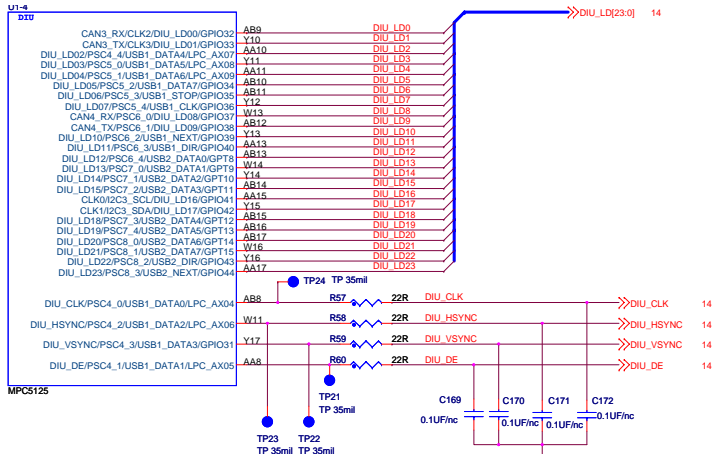
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Size C Document Number: **TWR-MPC5125** Rev: **v2.1**

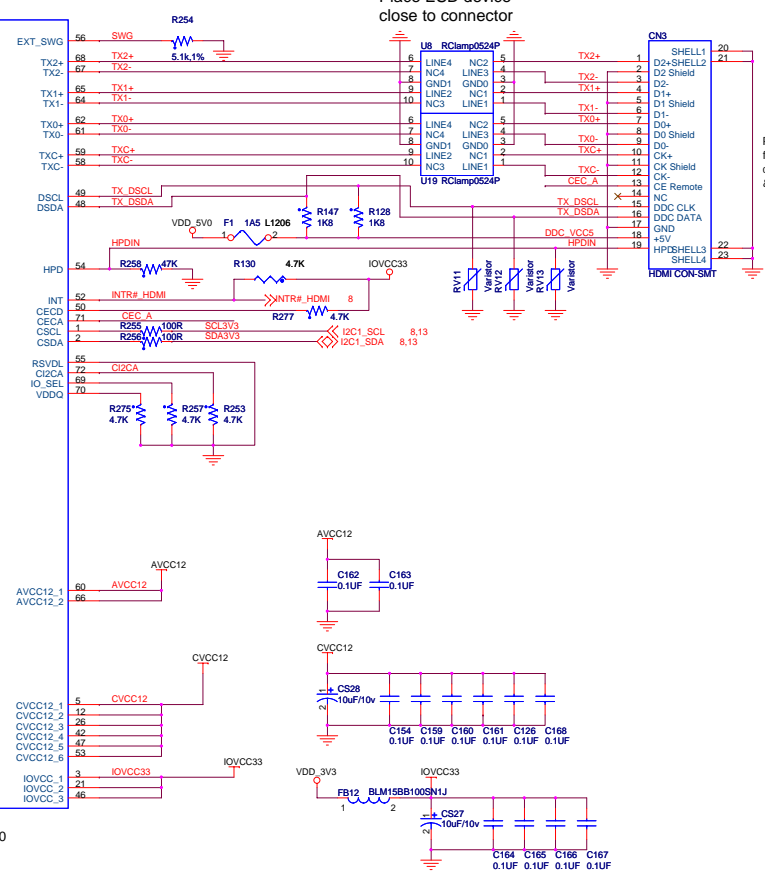
Date: **Monday, March 01, 2010** Sheet: **8** of **17**

MPC5125 - DIU AND HDMI INTERFACE

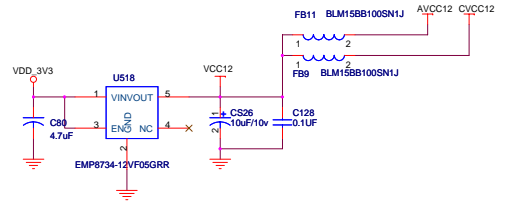


PCB LAYOUT: 100ohm differential impedance for TMD5 traces

PCB LAYOUT: Place ESD device close to connector



PCB LAYOUT: Layout footprint to support connector from JAE & Molex



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MPC5125 - DIU, HDMI INTERFACE

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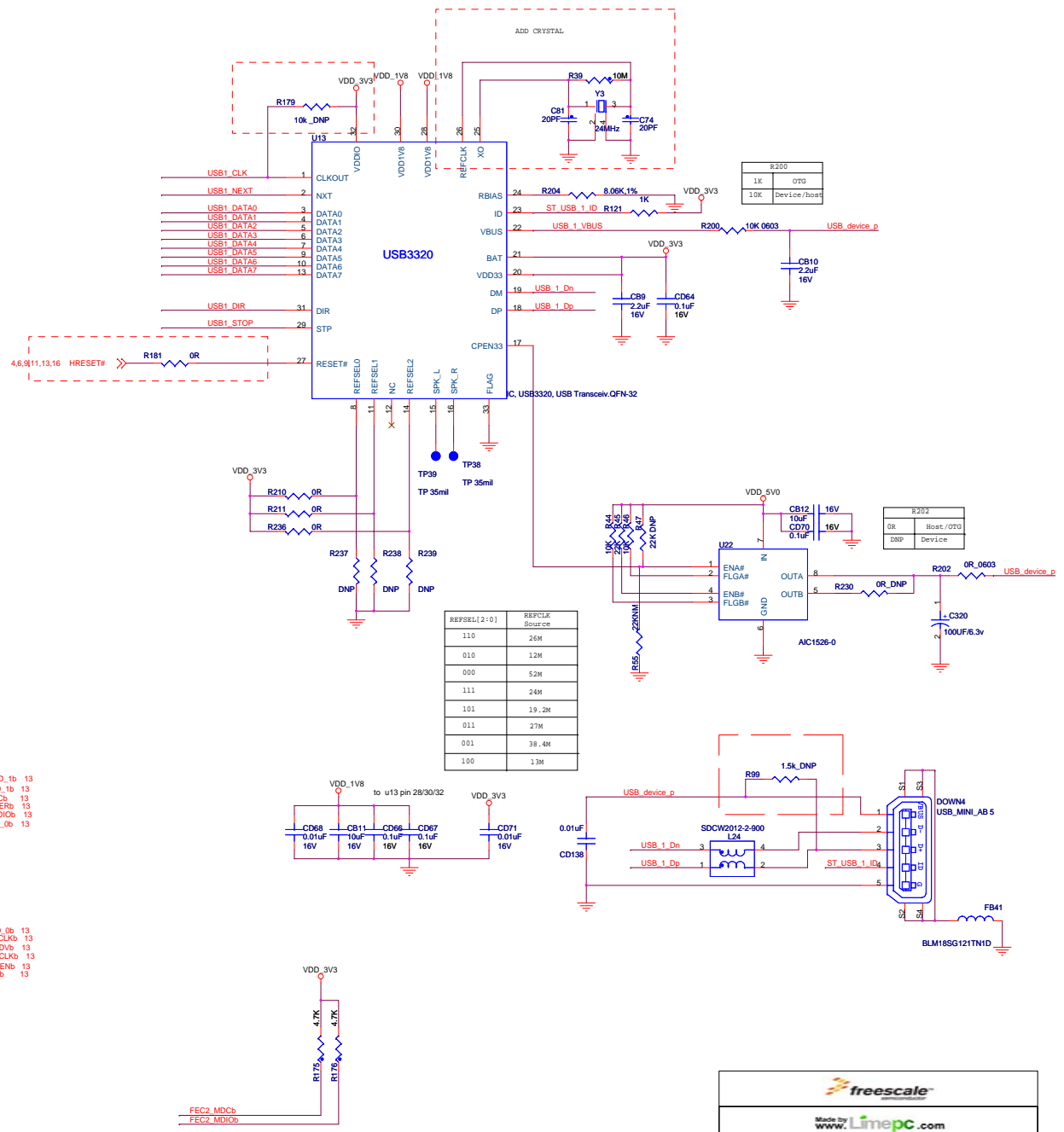


MPC5125 - USB1 AND FEC2 INTERFACE

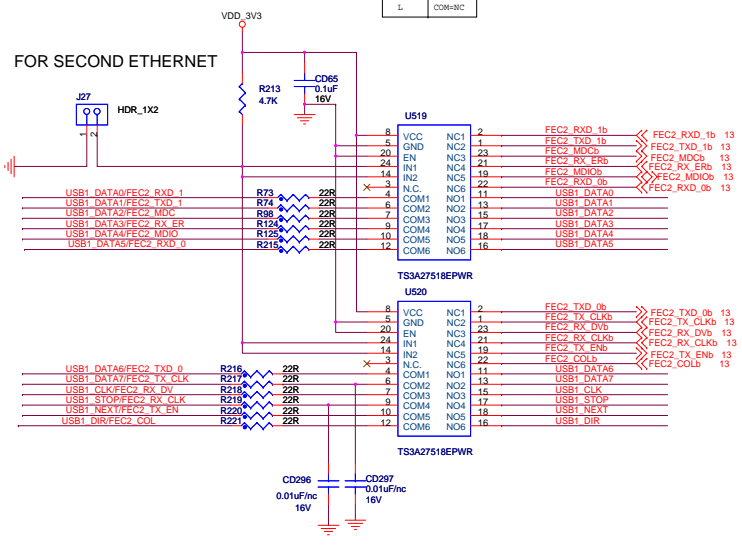
U1-7
USB1

USB1_DATA0PSC1_0FEC2_RXD_1/RMIL_RX1/TPR_AD10	Y3	USB1_DATA0/FEC2_RXD_1
USB1_DATA1PSC1_1FEC2_TXD_1/RMIL_TX1/TPR_AD11	W9	USB1_DATA1/FEC2_TXD_1
USB1_DATA2PSC1_2FEC2_MDC/RMIL_MDC/TPR_AD12	AB7	USB1_DATA2/FEC2_MDC
USB1_DATA3PSC1_3FEC2_RX_ER/RMIL_RX_ER/TPR_AD13	AB6	USB1_DATA3/FEC2_RX_ER
USB1_DATA4PSC1_4FEC2_MDIOR/MIL_MDIOR/TPR_AD14	AA7	USB1_DATA4/FEC2_MDIOR
USB1_DATA5PSC4_0FEC2_RXD_0/RMIL_RX0/TPR_AD15	V7	USB1_DATA5/FEC2_RXD_0
USB1_DATA6PSC4_1FEC2_TXD_0/RMIL_TX0/TPR_AD16	V6	USB1_DATA6/FEC2_TXD_0
USB1_DATA7PSC4_2FEC2_TX_CLK/RMIL_REF_CLK/TPR_AD17	AB5	USB1_DATA7/FEC2_TX_CLK
USB1_CLK/PSC4_4FEC2_RX_DV/RMIL_CRS_DV/TPR_DACK	Y8	USB1_CLK/FEC2_RX_DV
USB1_STOP/PSC4_3FEC2_RX_CLK/TPR_SYNC	W6	USB1_STOP/FEC2_RX_CLK
USB1_NEXT/FEC2_TX_EN/RMIL_TX_EN/GPIO09	AA5	USB1_NEXT/FEC2_TX_EN
USB1_DIR/FEC2_COL/GPIO10	W7	USB1_DIR/FEC2_COL

MPC5125



FOR SECOND ETHERNET



REFSEL[2:0]	REFCLK Source
110	26M
010	12M
000	52M
111	24M
101	19.2M
011	27M
001	38.4M
100	13M

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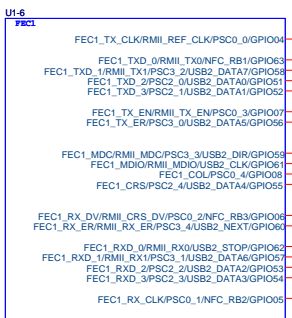
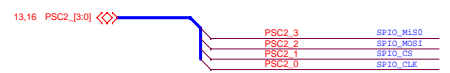
MPC5125 USB1/FEC2

Document Number: TWR-MPC5125
Rev: v2.1

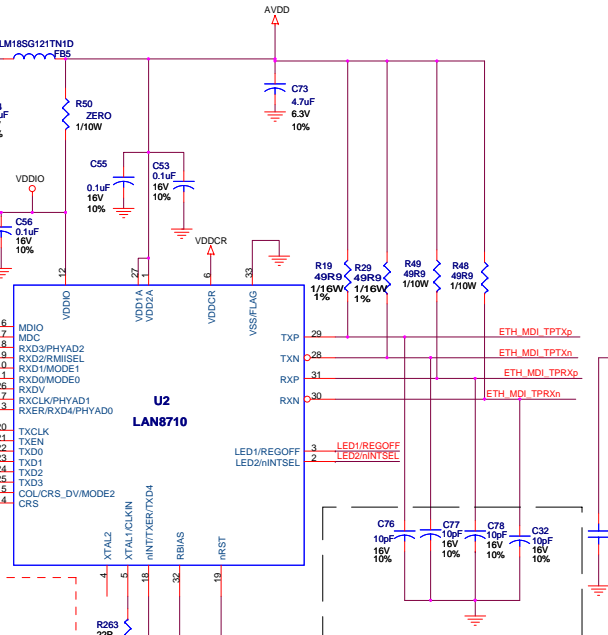
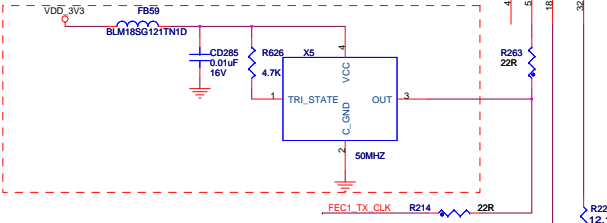
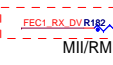
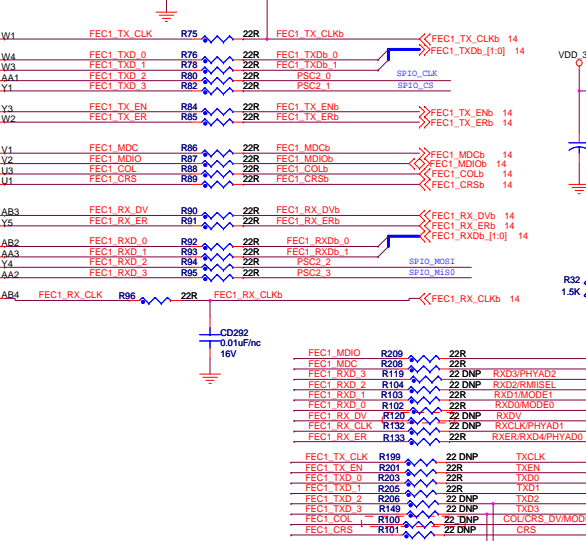
Date: Monday, March 01, 2010 | Sheet: 10 of 17



MPC5125 - MISC. INTERFACES



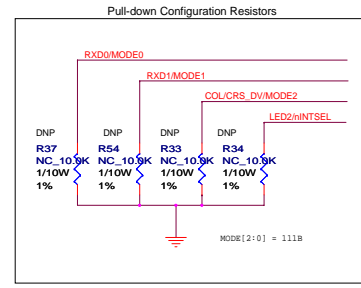
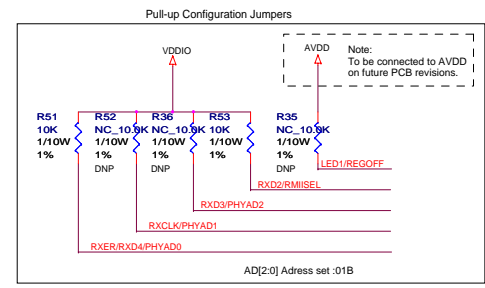
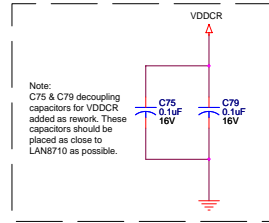
MPC5125



Note: Capacitors C32 through C76 are optional for EMI purposes and are not populated on the LAN8710 evaluation board. These capacitors are required for operation in an EMI constrained environment.

Configuration Resistor Settings

Resistor	POPULATE	EMPTY
R51	PHYAD[0] = 1	PHYAD[0] = 0
R52	PHYAD[1] = 1	PHYAD[1] = 0
R36	PHYAD[2] = 1	PHYAD[2] = 0
R53	RMII mode selected	MI mode selected
R35	Internal 1.2V reg. disabled	Internal 1.2V reg enabled
R37	MODE[0] = 0	MODE[0] = 1
R54	MODE[1] = 0	MODE[1] = 1
R33	MODE[2] = 0	MODE[2] = 1
R34	INTERRUPT FUNCTION DISABLED ON nINT/TXER/TXD4 SIGNAL	INTERRUPT FUNCTION ENABLED ON nINT/TXER/TXD4 SIGNAL



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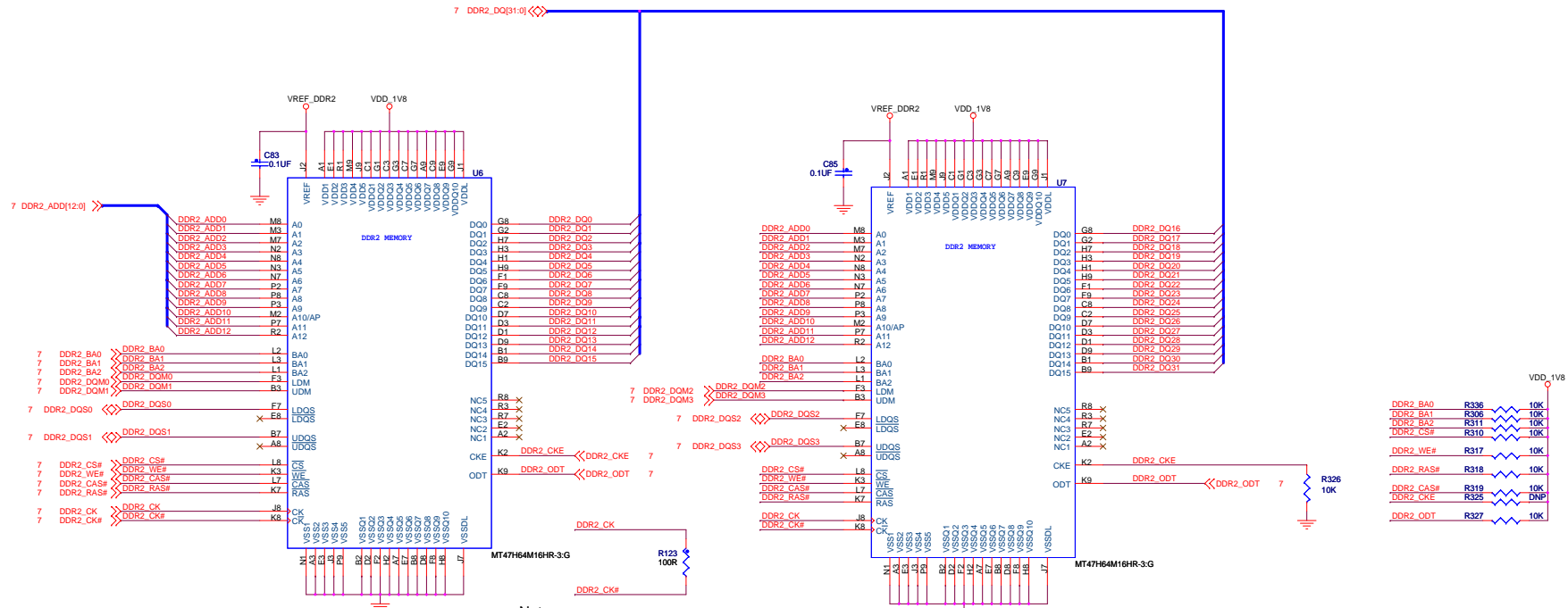
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Size C Document Number: TWR-MPC5125 Rev v2.1

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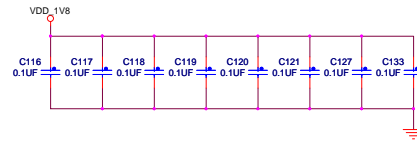
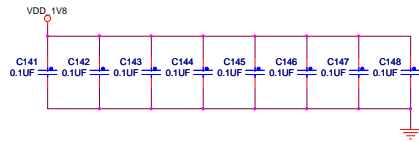
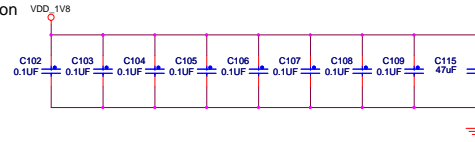
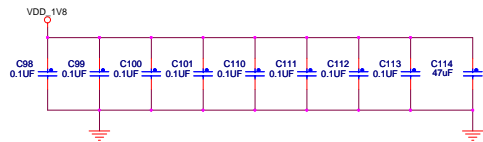


DDR-2 MEMORIES AND TERMINATIONS



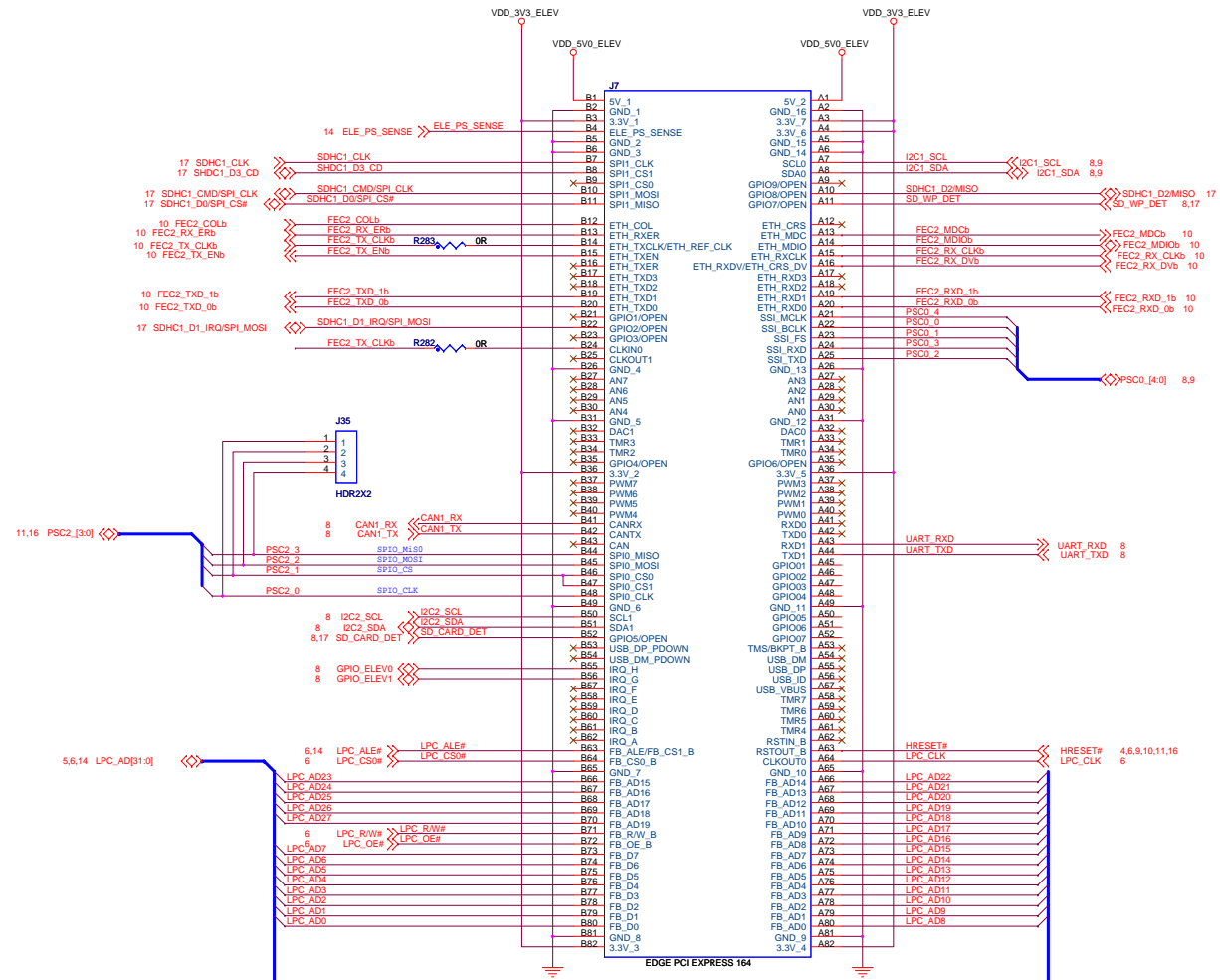
Note:

Place the DDR2 CLK Termination resistor close the Chips





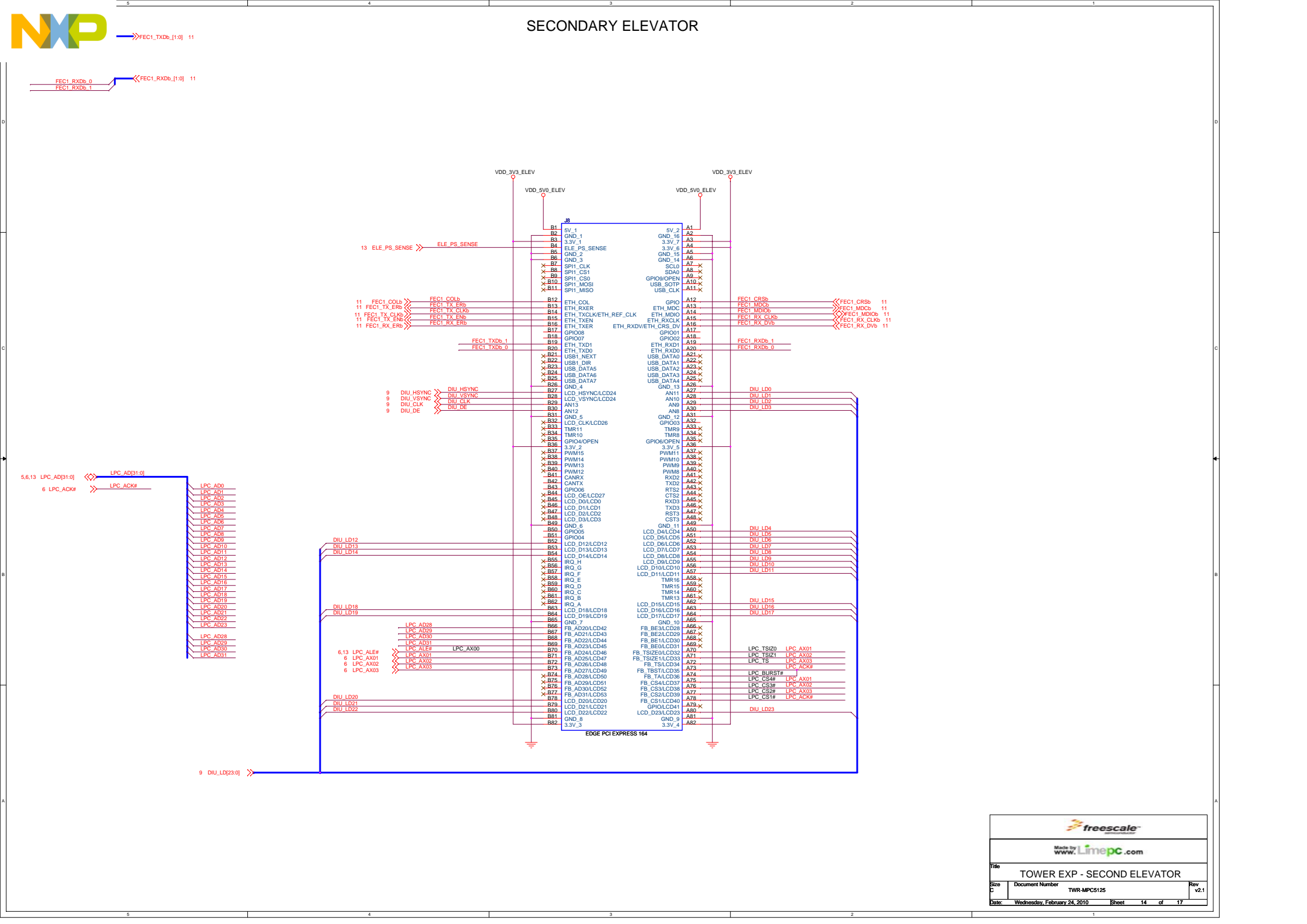
MAIN ELEVATOR



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File: TOWER EXP - MAIN ELEVATOR

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SECONDARY ELEVATOR

NXP → FEC1_TXDb_[1:0] 11

FEC1_RXDb_0
FEC1_RXDb_1 ← FEC1_RXDb_[1:0] 11

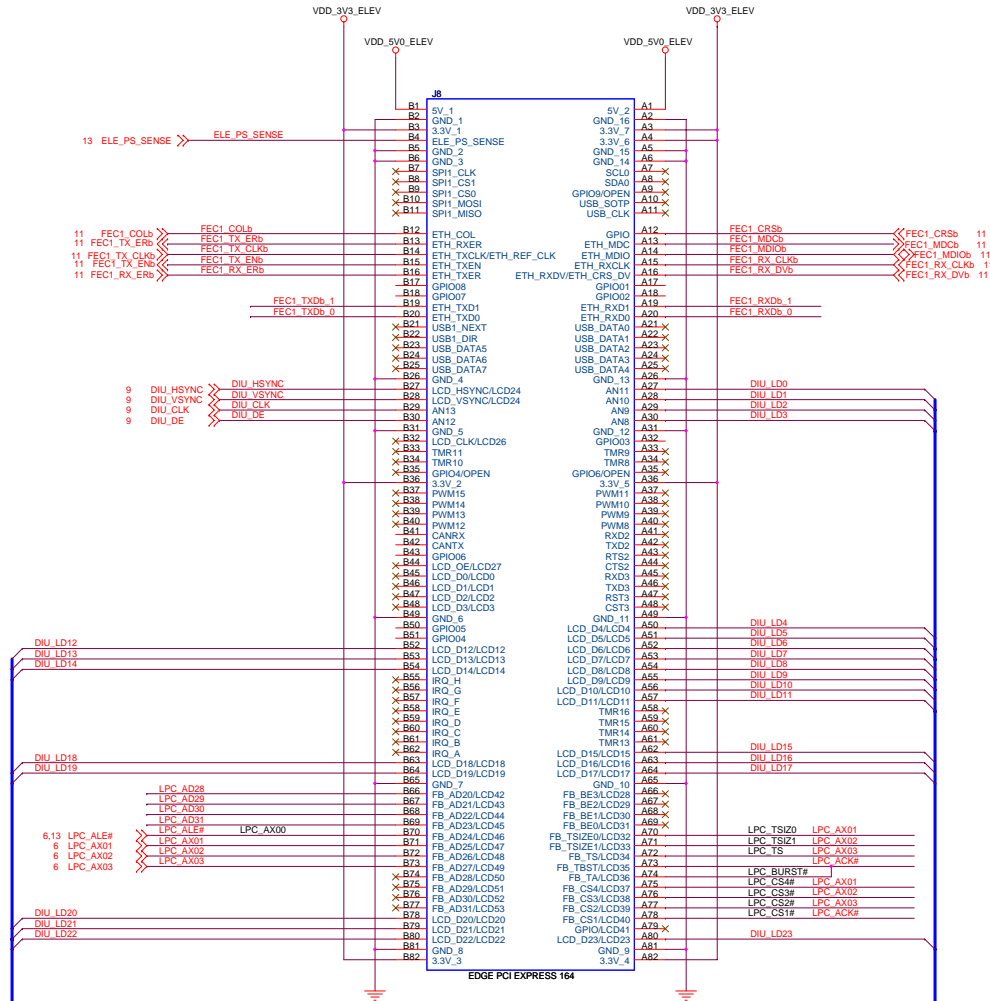
5.6,13 LPC_AD[31:0] → LPC_AD[31:0]
6 LPC_ACK# → LPC_ACK#

LPC AD0
LPC AD1
LPC AD2
LPC AD3
LPC AD4
LPC AD5
LPC AD6
LPC AD7
LPC AD8
LPC AD9
LPC AD10
LPC AD11
LPC AD12
LPC AD13
LPC AD14
LPC AD15
LPC AD16
LPC AD17
LPC AD18
LPC AD19
LPC AD20
LPC AD21
LPC AD22
LPC AD23
LPC AD28
LPC AD29
LPC AD30
LPC AD31

6,13 LPC_ALE# → LPC_ALE#
6 LPC_AX01 → LPC_AX01
6 LPC_AX02 → LPC_AX02
6 LPC_AX03 → LPC_AX03

LPC AX00
LPC AX01
LPC AX02
LPC AX03

9 DIU_LD[23:0] →



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Title: TOWER EXP - SECOND ELEVATOR

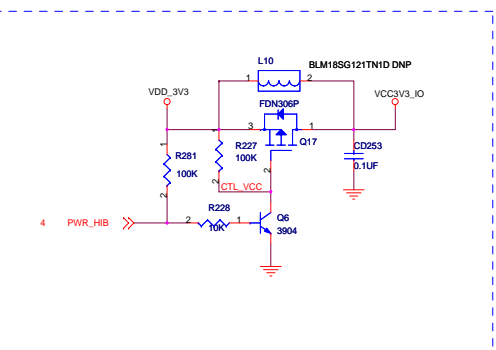
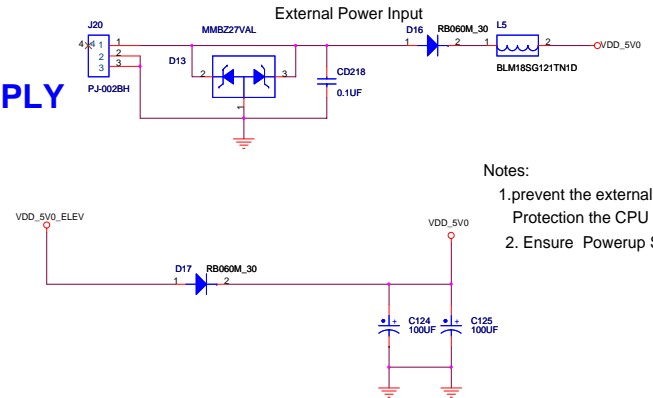
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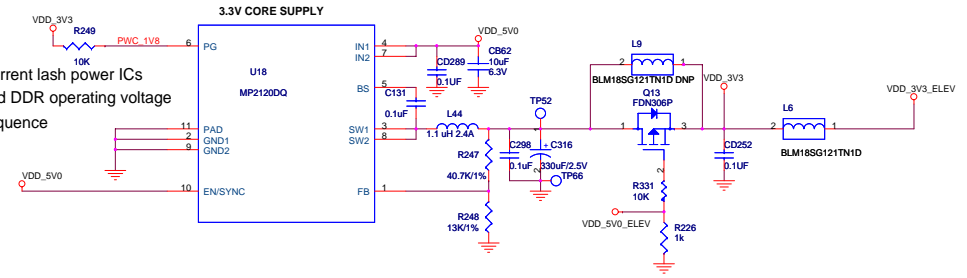
POWER SUPPLY

POWER SUPPLY

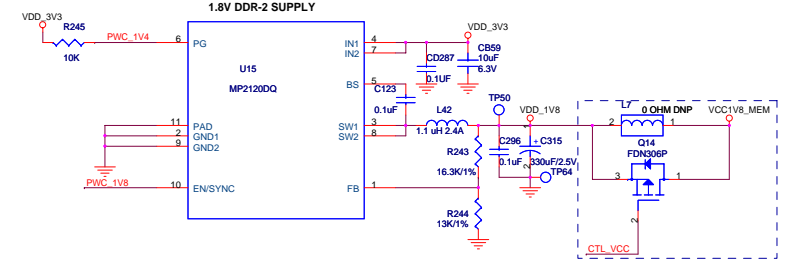


- Notes:
1. prevent the external current lash power ICs Protection the CPU and DDR operating voltage
 2. Ensure Powerup Sequence

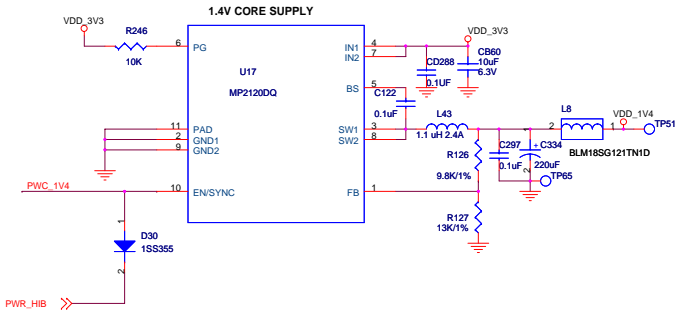
3.3V @ 2.5A POWER SUPPLY



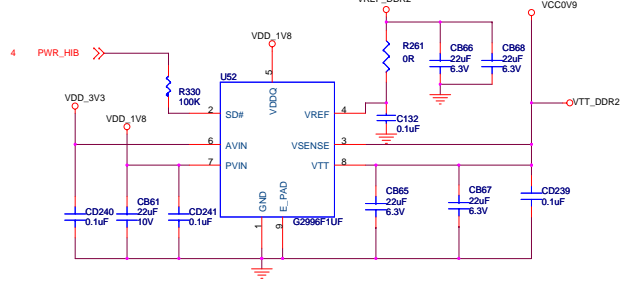
1.8V @ 2.5A POWER SUPPLY



1.4V @ 2.5A POWER SUPPLY

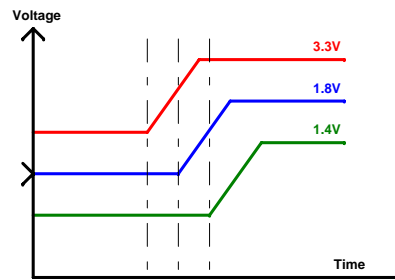


DDR-2 TERMINATION REG



- Note
1. Route VSENSE line as a trace and connect it to the VTT power plane near the DDR-2 memories
 2. Provide Ground Guard to the Vsense line

Powerup Sequence



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POWER SUPPLY			
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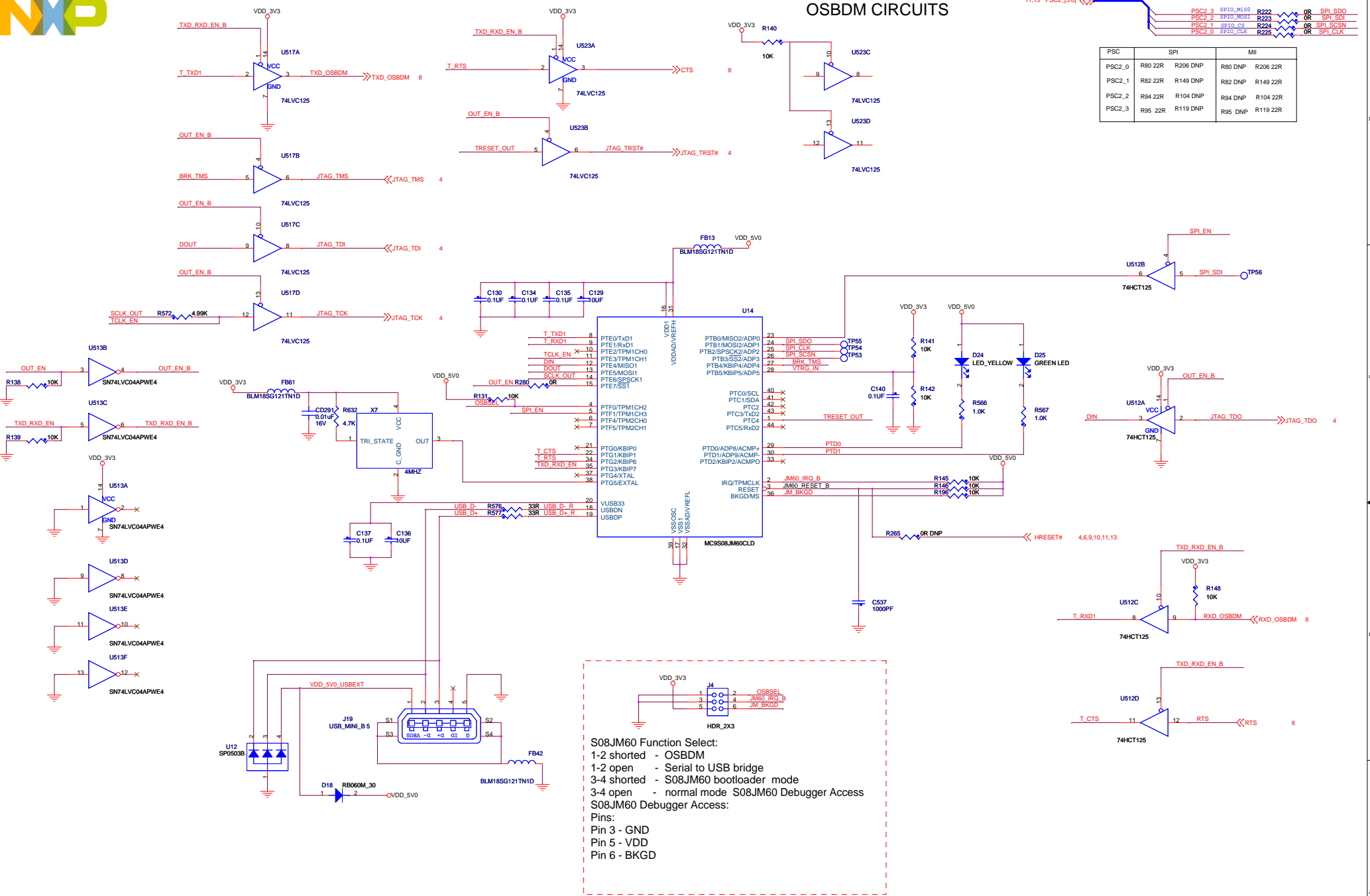


OSBDM CIRCUITS

11.13 PSC2_[3:0]

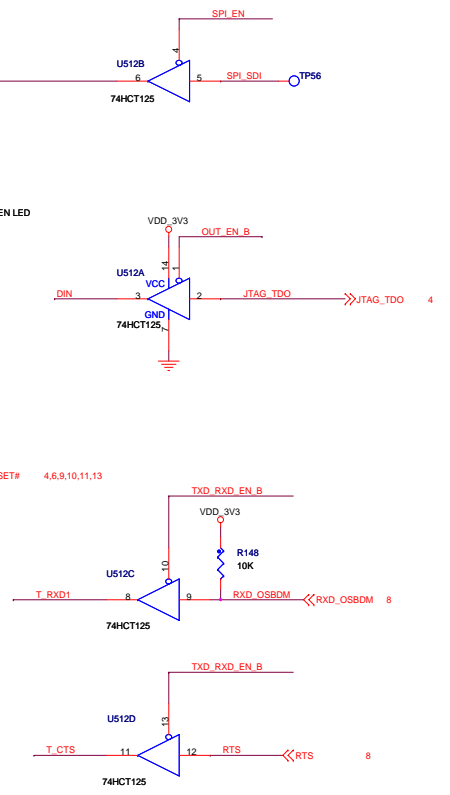
PSC2_3	SP10_MISO	R223	OR	SPI_SDO
PSC2_2	SP10_MOSI	R223	OR	SPI_SDI
PSC2_1	SP10_CS	R224	OR	SPI_SCSN
PSC2_0	SP10_CLK	R225	OR	SPI_CLK

PSC	SPI	MII
PSC2_0	R80 22R R206 DNP	R80 DNP R206 22R
PSC2_1	R82 22R R149 DNP	R82 DNP R149 22R
PSC2_2	R94 22R R104 DNP	R94 DNP R104 22R
PSC2_3	R95 22R R119 DNP	R95 DNP R119 22R



S08JM60 Function Select:
 1-2 shorted - OSBDM
 1-2 open - Serial to USB bridge
 3-4 shorted - S08JM60 bootloader mode
 3-4 open - normal mode S08JM60 Debugger Access

S08JM60 Debugger Access:
 Pins:
 Pin 3 - GND
 Pin 5 - VDD
 Pin 6 - BKGD





AC97 AND SD

