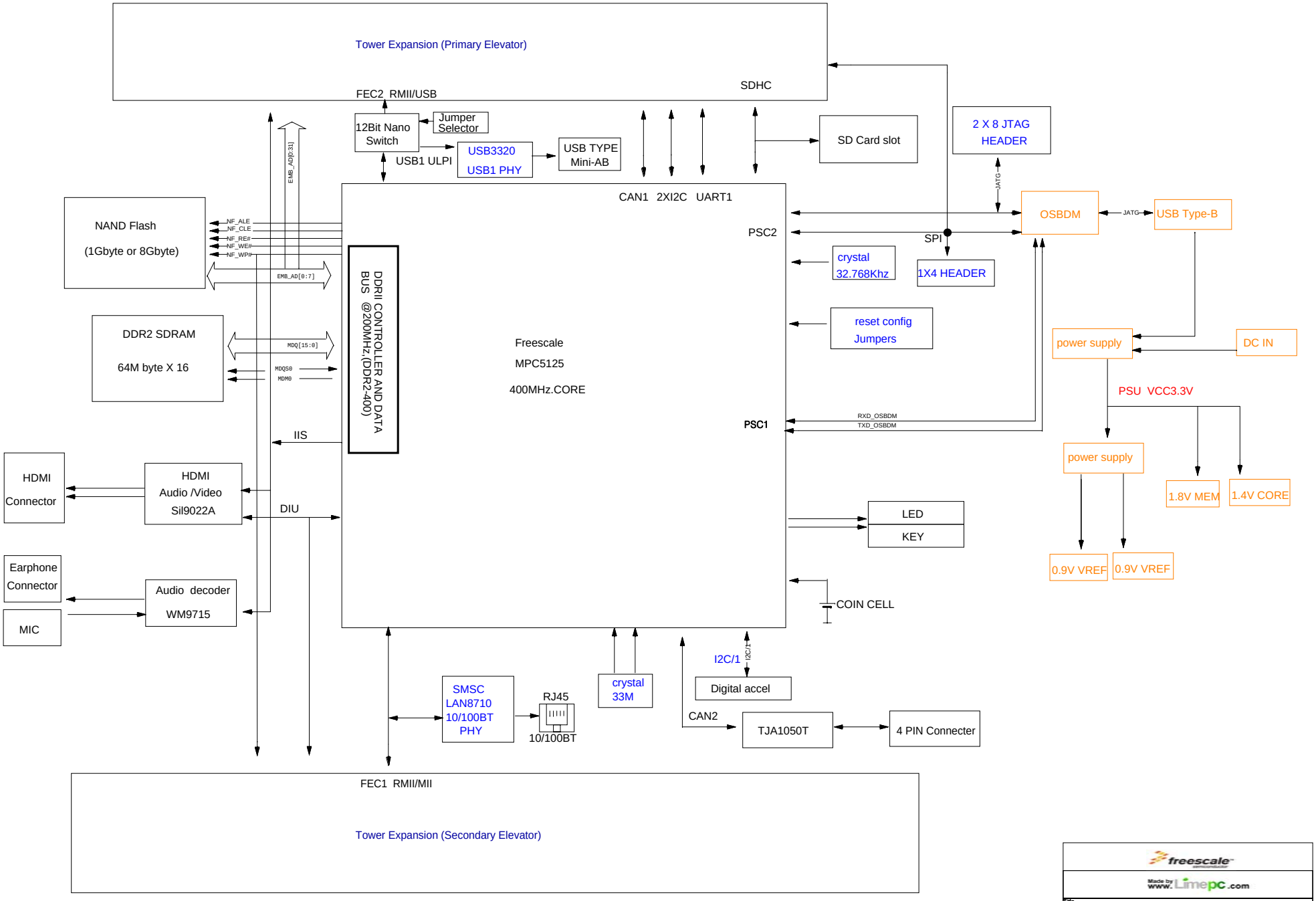
TABLE OF CONTENTS AND REV HISTORY

Title: COVER_PAGE

Size: C | Document Number: TWR-MPC5125 | Rev: v2.1

Date: Wednesday, February 24, 2010 | Sheet 1 of 17

BLOCK DIAGRAM



freescale semiconductor

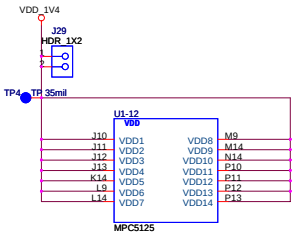
Made by www.Limepc.com

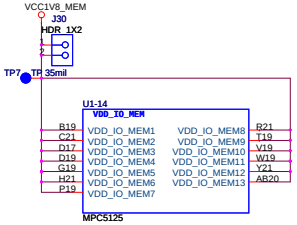
Title: BLOCK DIAGRAM

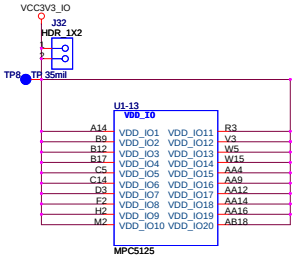
Size	Document Number	Rev
C	TWR-MPC5125	v2.1

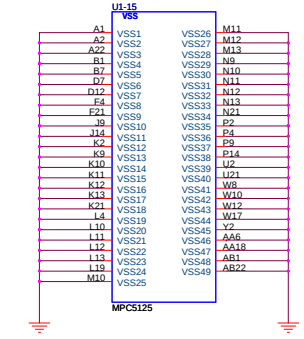
Date: Wednesday, February 24, 2010 Sheet 2 of 17

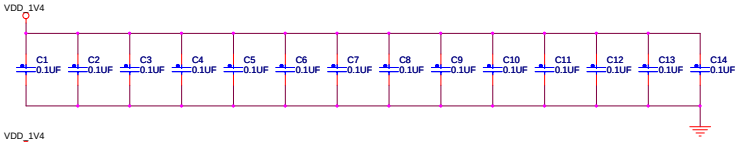
MPC5125 POWER AND DECAPS

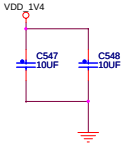


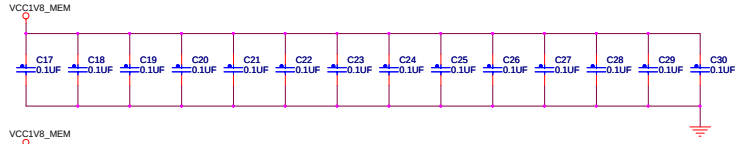


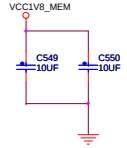


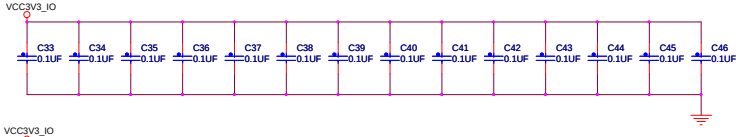


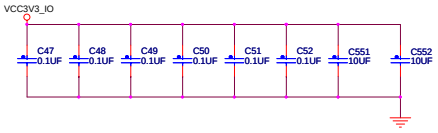






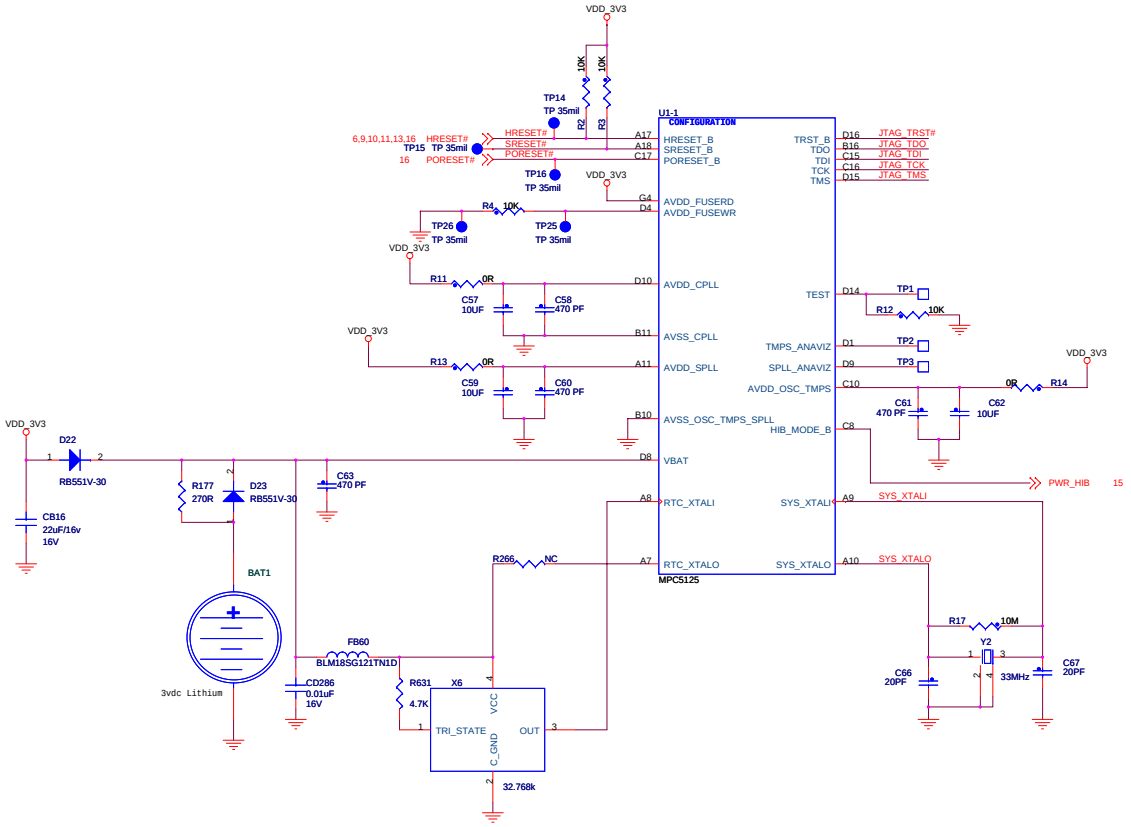




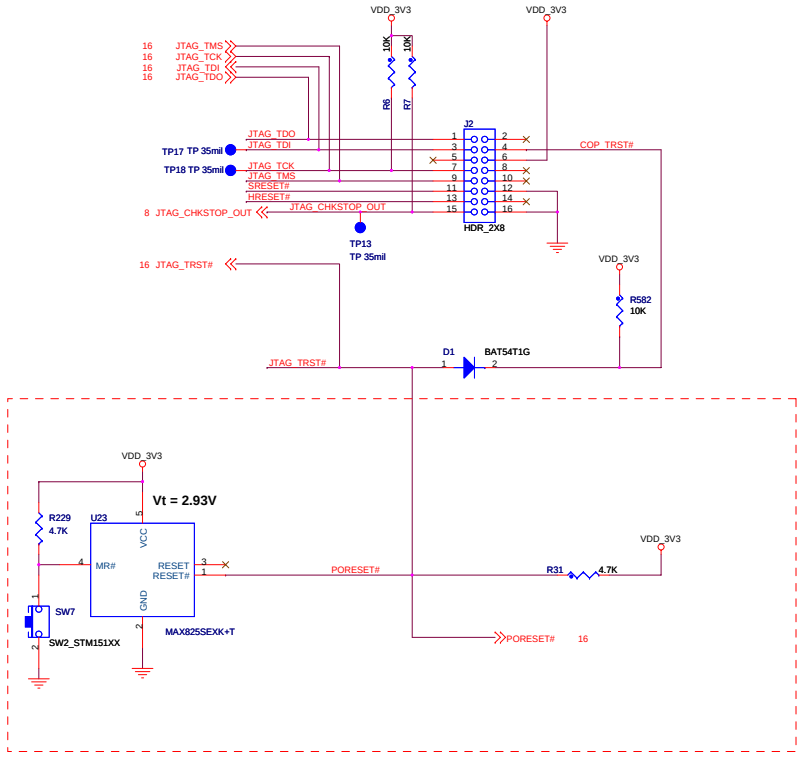


Title	MPC5125 POWER AND DECAPS	
Size C	Document Number TWR-MPC5125	Rev v2.1
Date: Thursday, February 25, 2010	Sheet 3 of 17	

MPC5125 - CONFIGURATION



JTAG Header



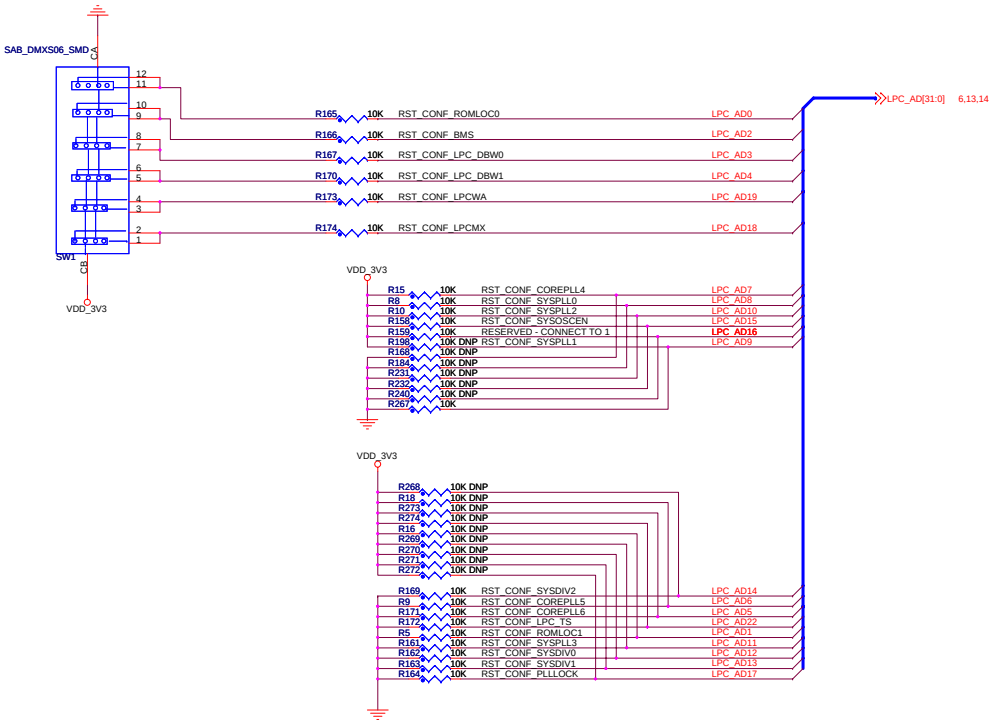
Made by www.Limepc.com		
Title: MPC5125 CONFIGURATION		
Size: C	Document Number: TWR-MPC5125	Rev: v2.1
Date: Wednesday, February 24, 2010	Sheet 4 of 17	

RESET CONFIGURATION JUMPERS

RST FUNCTION	LPC PIN	DESCRIPTION
RST_CONF_LOC	LPC_AD[1:0] Default 01	Selects boot device 00 LPC boot 01 NAND (NFC) boot2 10 Factory Test mode, use TPR port at LPC 11 Factory Test mode, use TPR port at DIU
RST_CONF_BMS	LPC_AD[2] Default 1	Boot mode select: Selects e300 boot vector and configures default value for LPC CS0 or NFC base address.
RST_CONF_LPC_DBW	LPC_AD[4:3] Default 00	LPC Data Port Size 00 8 bit 10 Reserved 01 16 bit 11 32 bit
RST_CONF_COREPLL 2.0 : 1	LPC_AD[7:5] Default 100	Core PLL Multiply factor See clock module for programming options
RST_CONF_SYSPLL 24 : 1	LPC_AD[11:8] Default 0101	System PLL Multiply factor See clock module for programming options
RST_CONF_SYSDIV 2	LPC_AD[14:12] Default 000	System PLL divider ratio See clock module for programming options
RST_CONF_SYSOSCEN	LPC_AD[15] Default 1	Oscillator Bypass Mode 0 System Oscillator bypass mode 1 System Oscillator mode
RST_CONF_LONGFB	LPC_AD[16] Default 1	Reserved (must be tied to logic high)
RST_CONF_PLLLOCK	LPC_AD[17] Default 0	Use PLL lock signal 1 use counter 0 use PLL lock signal
RST_CONF_LPCMX	LPC_AD[18] Default 0	LPC Mux mode configuration 0 Non-multiplexed mode 1 Multiplexed mode
RST_CONF_LPCWA	LPC_AD[19] Default 1	LPC Word/Byte address 1 Address is interpreted as byte address 0 Address is interpreted as word address
RST_CONF_LPC_TS	LPC_AD[22] Default 0	Use LPC_TS, LPC_TSIZE[1:0] if boot from LPC 1 use LPC_TS, LPC_TSIZE[1:0] if boot from LPC 0 set LPC_TS, LPC_TSIZE[1:0] is set to one if boot from LPC

Parameter	BMS=0(Boot low)	BMS=1(Boot high)
e300 Boot Vector	0 X 00000100	0 X FFF00100

Parameter	BMS=0(Boot low)	BMS=1(Boot high)
LPC CSBOOT Start	0 X 00000000	0 X FFF00000
LPC CSBOOT End	0 X 0007FFFF	0 X FFFFFFFF
NFC Base Address	0 X 00000000	0 X FFF00000



freescale

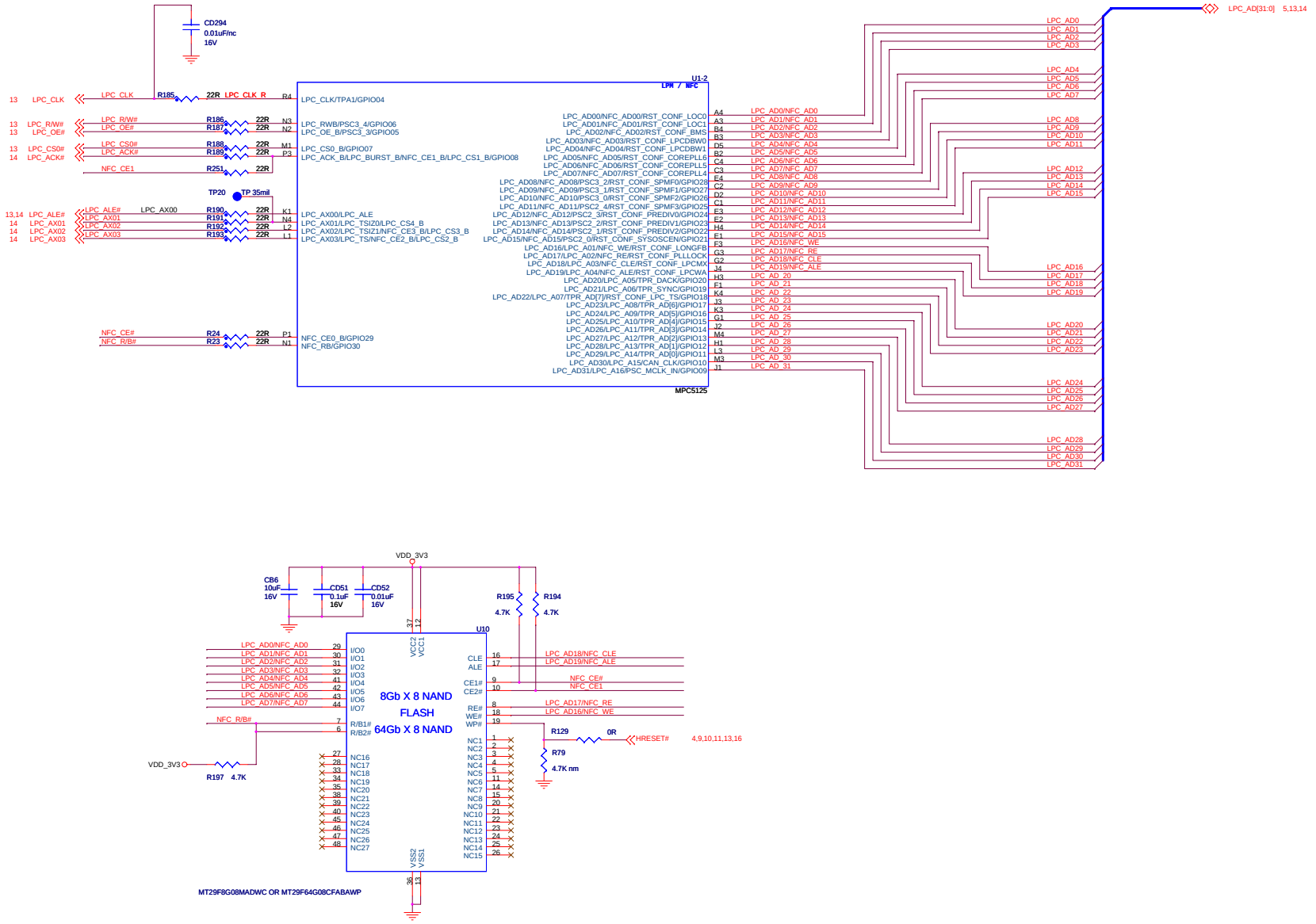
Made by www.Limepc.com

Title: RESET CONFIG JUMPERS

Size	Document Number	Rev
C	TWR-MPC5125	v2.1

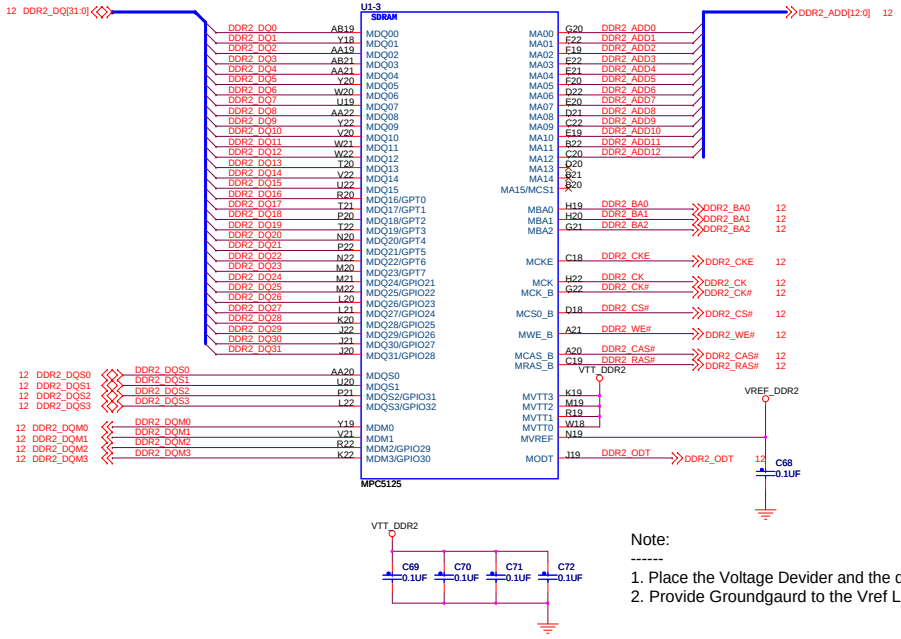
Date: Wednesday, February 24, 2010 Sheet 5 of 17

MPC5125 - LPC AND NFC



Title	MPC5125 LPC AND NFC		
Size C	Document Number TWR-MPC5125		Rev v2.1
Date: Monday, March 01, 2010	Sheet 6 of 17		

MPC5125 - DDR-2 MEMORY INTERFACE



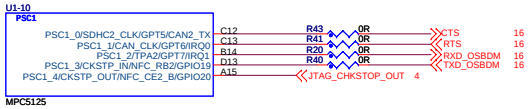
Note:
---
1. Place the Voltage Devider and the decap near the Pin
2. Provide Groundgaurd to the Vref Line

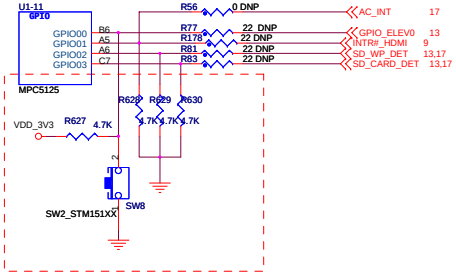
freescale

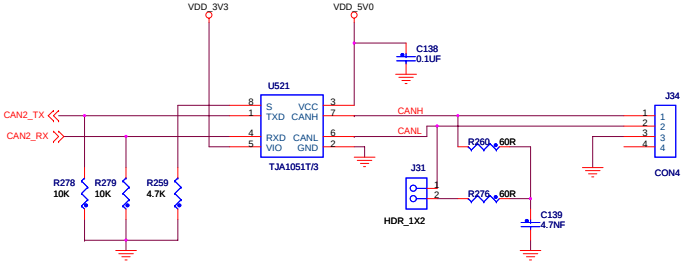
Made by www.Limepc.com

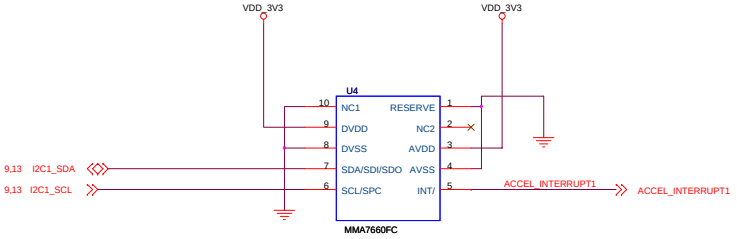
Title	MPC5125 DDR2 INTERFACE	
Size C	Document Number TWR-MPC5125	Rev v2.1
Date: Wednesday, February 24, 2010	Sheet 7 of 17	

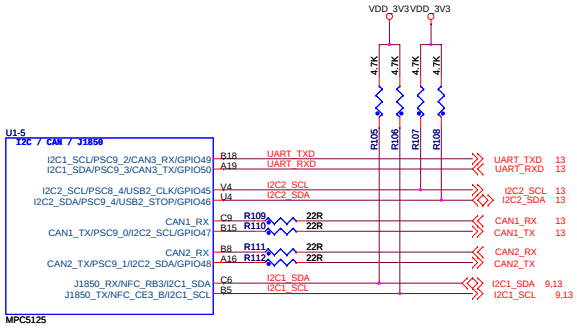
MPC5125 - ACCEL INTERFACE

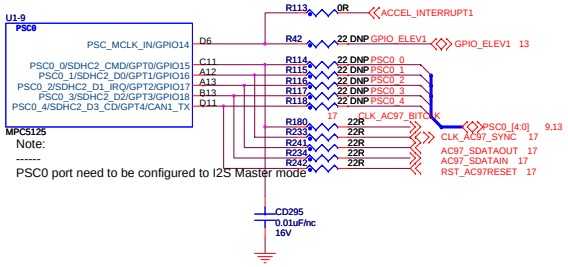










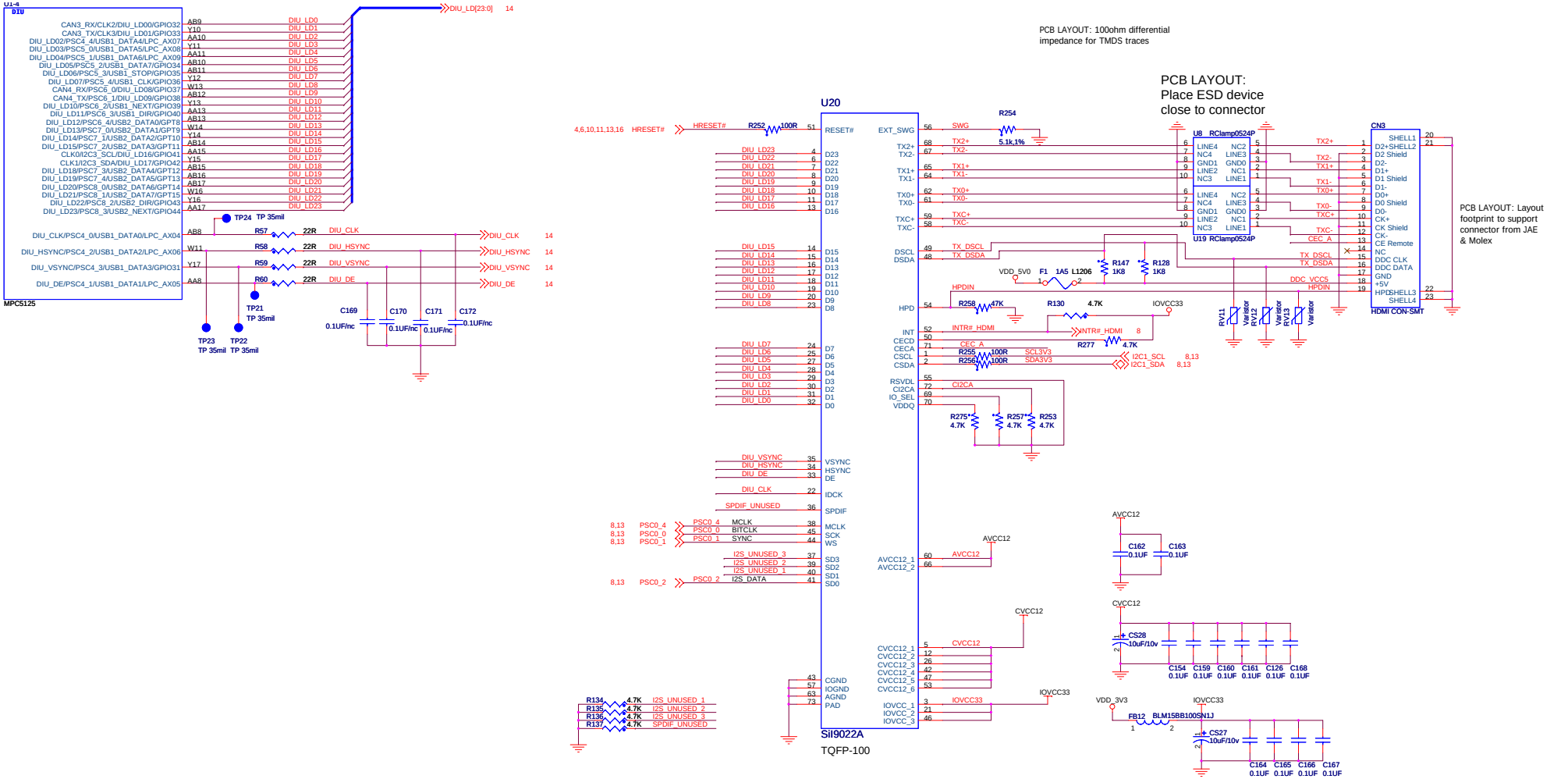


Title
MPC5125 RS232 AND ACCEL

Size	Document Number	Rev
C	TWR-MPC5125	v2.1

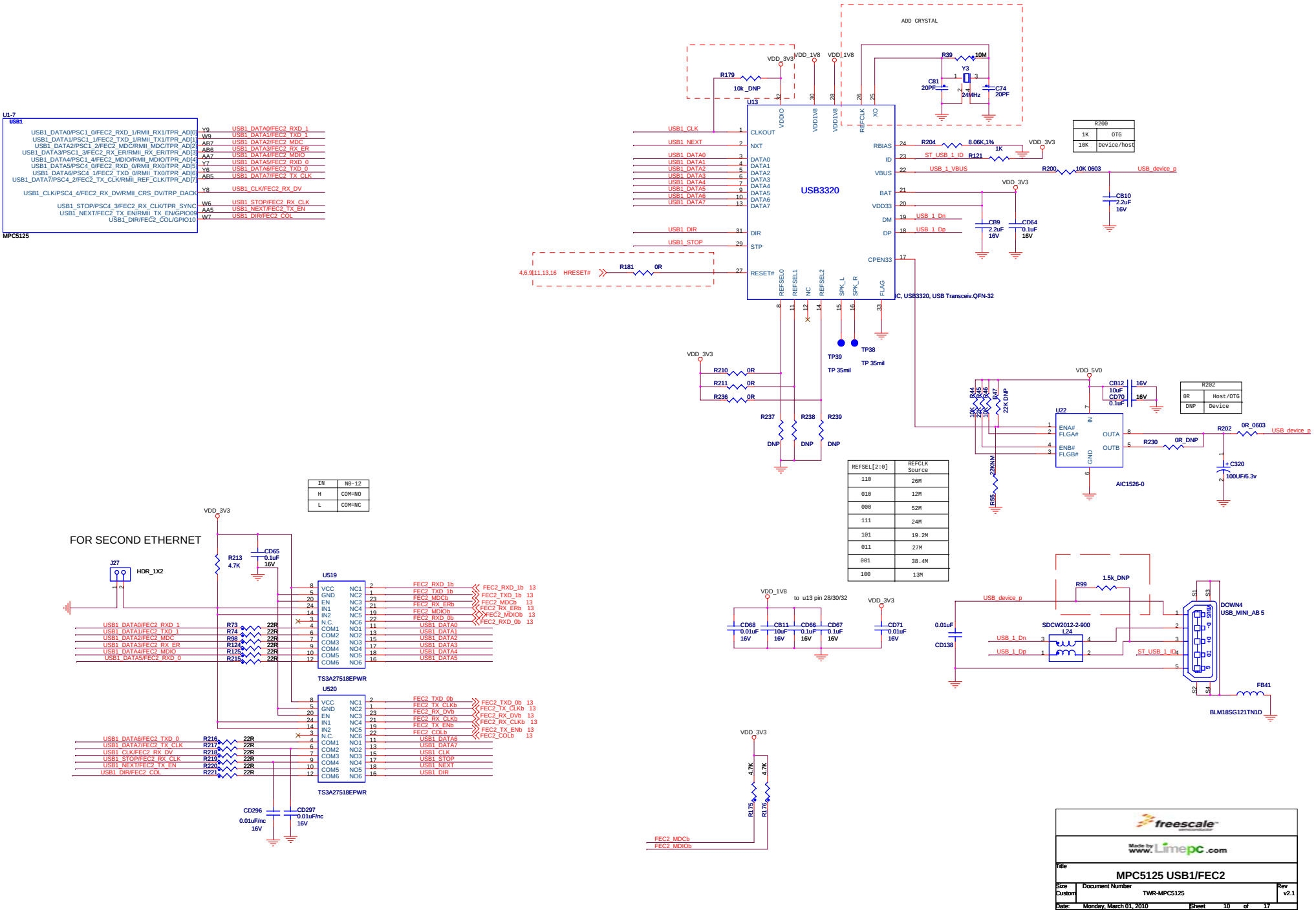
Date: Monday, March 01, 2010 Sheet 8 of 17

MPC5125 - DIU AND HDMI INTERFACE

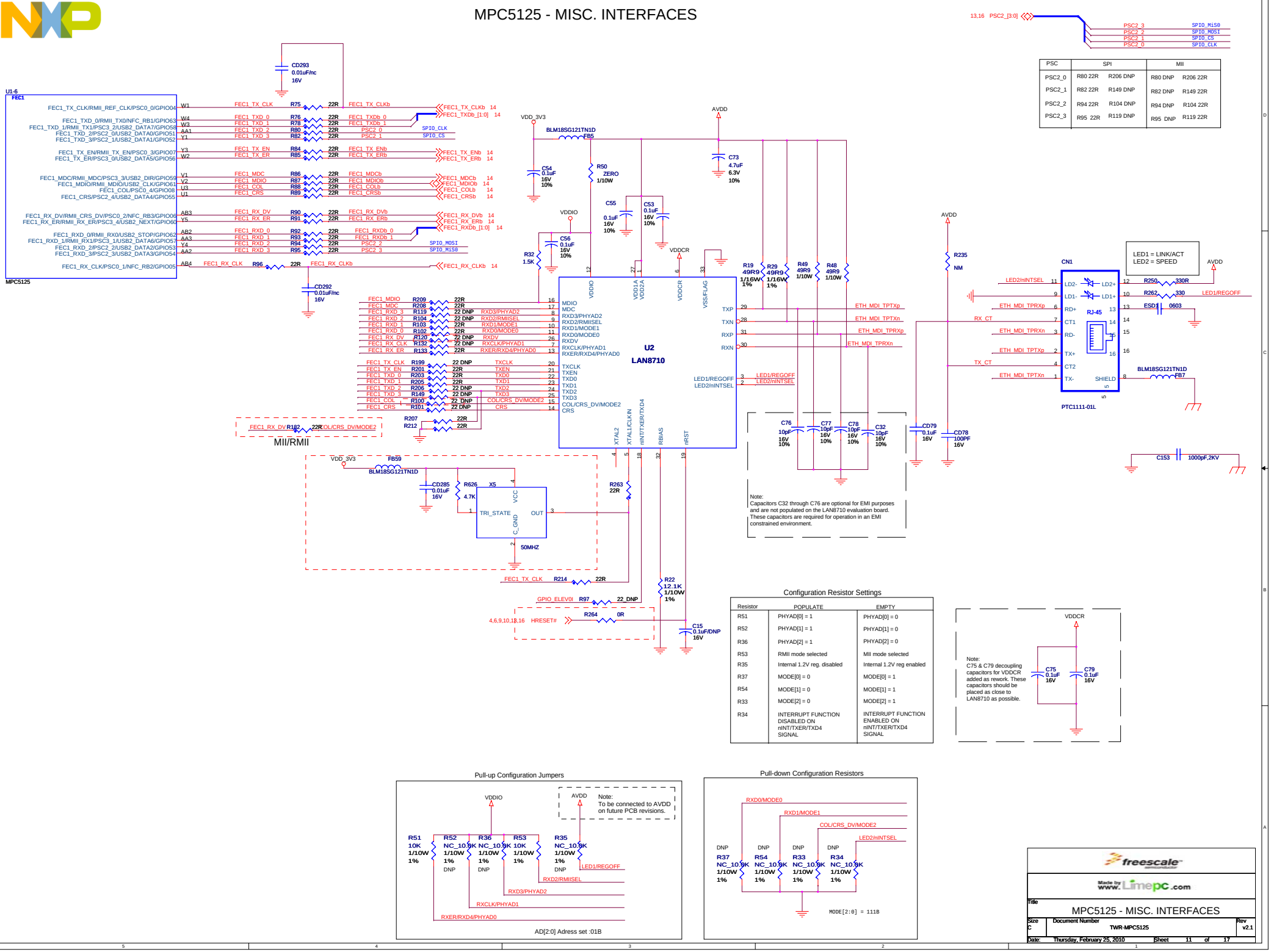


Title	MPC5125 - DIU,HDMI INTERFACE		
Size C	Document Number TWR-MPC5125		Rev v2.1
Date: Monday, March 01, 2010	Sheet 9 of 17		

MPC5125 - USB1 AND FEC2 INTERFACE



MPC5125 - MISC. INTERFACES



PSC	SPI		MII	
PSC2_0	R80 22R	R206 DNP	R80 DNP	R206 22R
PSC2_1	R82 22R	R149 DNP	R82 DNP	R149 22R
PSC2_2	R94 22R	R104 DNP	R94 DNP	R104 22R
PSC2_3	R95 22R	R119 DNP	R95 DNP	R119 22R

Configuration Resistor Settings

Resistor	POPULATE	EMPTY
R51	PHYAD[0] = 1	PHYAD[0] = 0
R52	PHYAD[1] = 1	PHYAD[1] = 0
R36	PHYAD[2] = 1	PHYAD[2] = 0
R53	RMII mode selected	MII mode selected
R35	Internal 1.2V reg. disabled	Internal 1.2V reg enabled
R37	MODE[0] = 0	MODE[0] = 1
R54	MODE[1] = 0	MODE[1] = 1
R33	MODE[2] = 0	MODE[2] = 1
R34	INTERRUPT FUNCTION DISABLED ON nINT/TXER/TXD4 SIGNAL	INTERRUPT FUNCTION ENABLED ON nINT/TXER/TXD4 SIGNAL

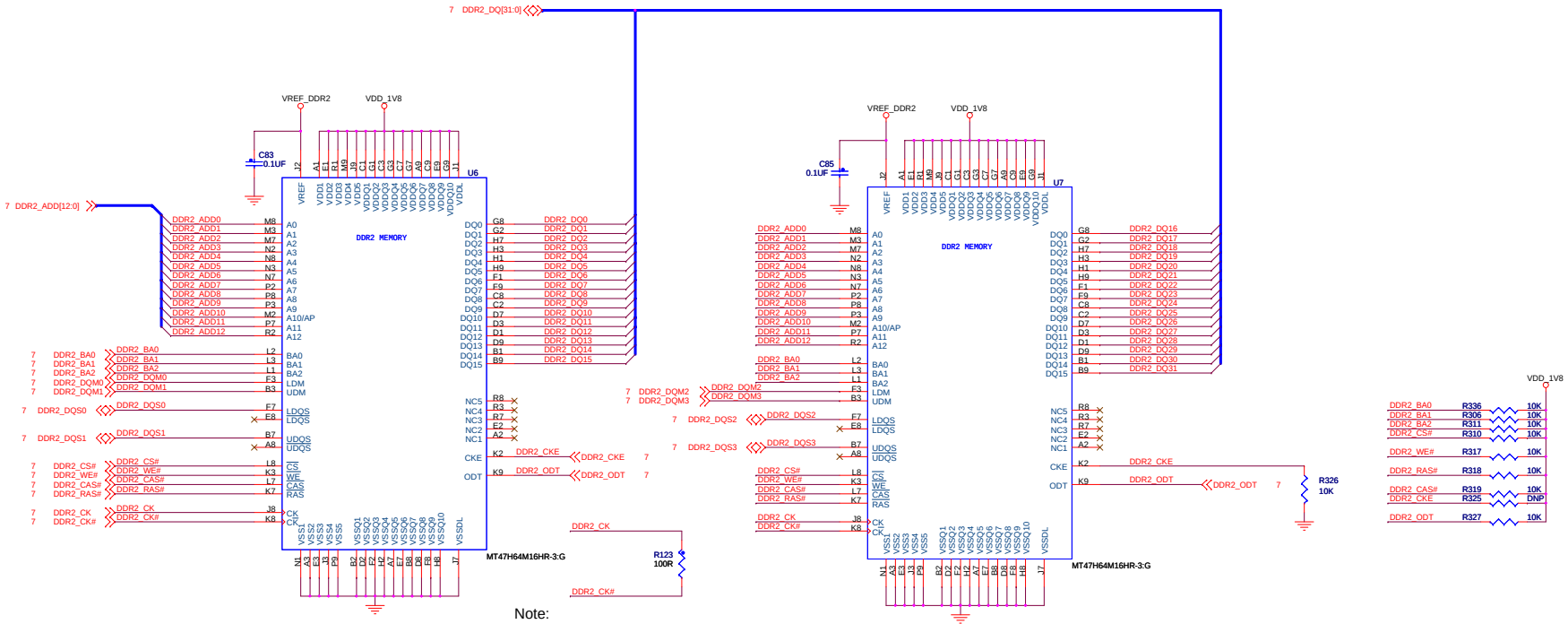
Pull-up Configuration Jumpers

Pull-down Configuration Resistors

Made by www.Limepc.com

Title	MPC5125 - MISC. INTERFACES		
Size C	Document Number TWR-MPC5125		Rev v2.1
Date: Thursday, February 25, 2010	Sheet 11 of 17		

DDR-2 MEMORIES AND TERMINATIONS

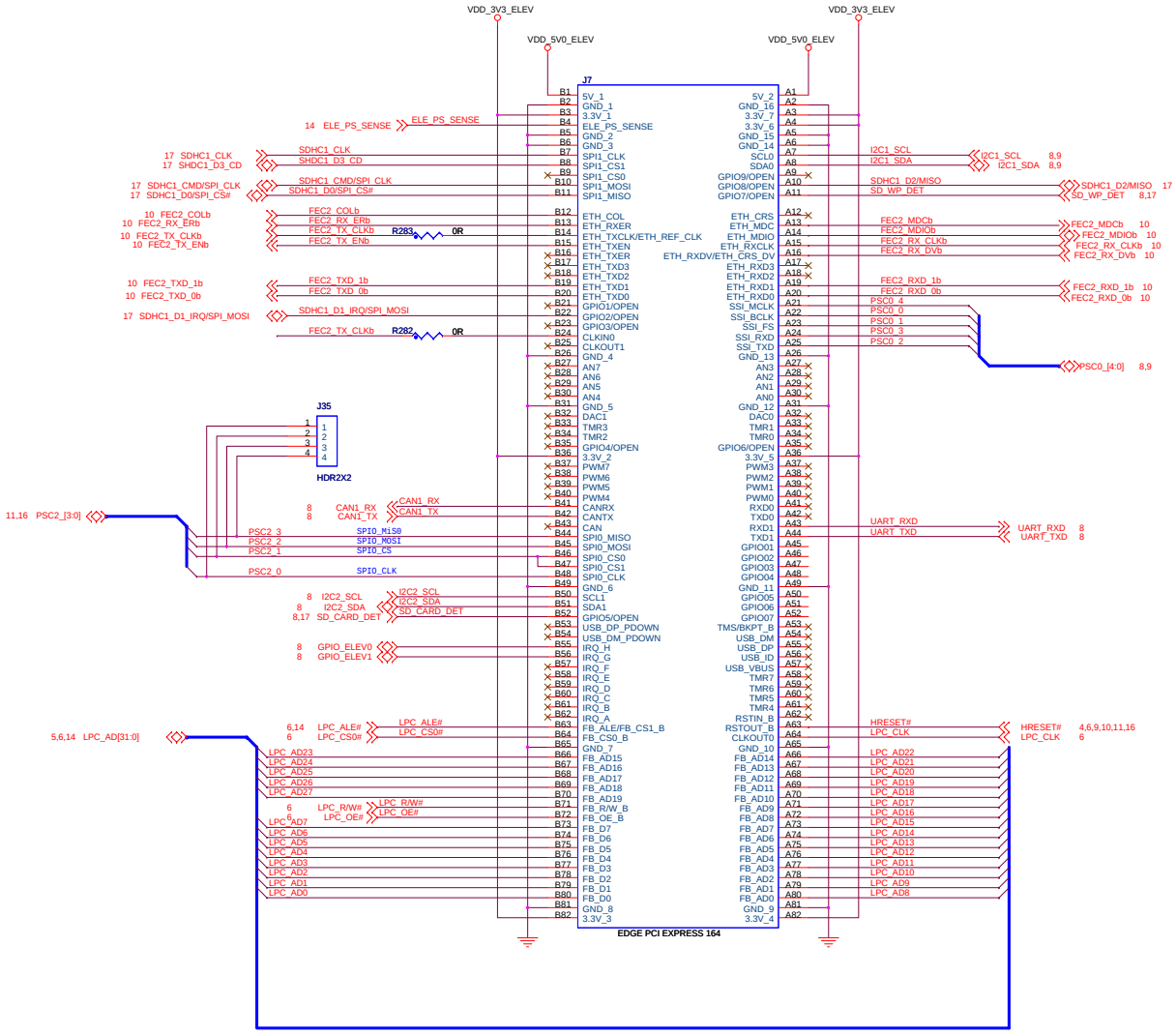


Note:

Place the DDR2 CLK Termination resistor close the Chips

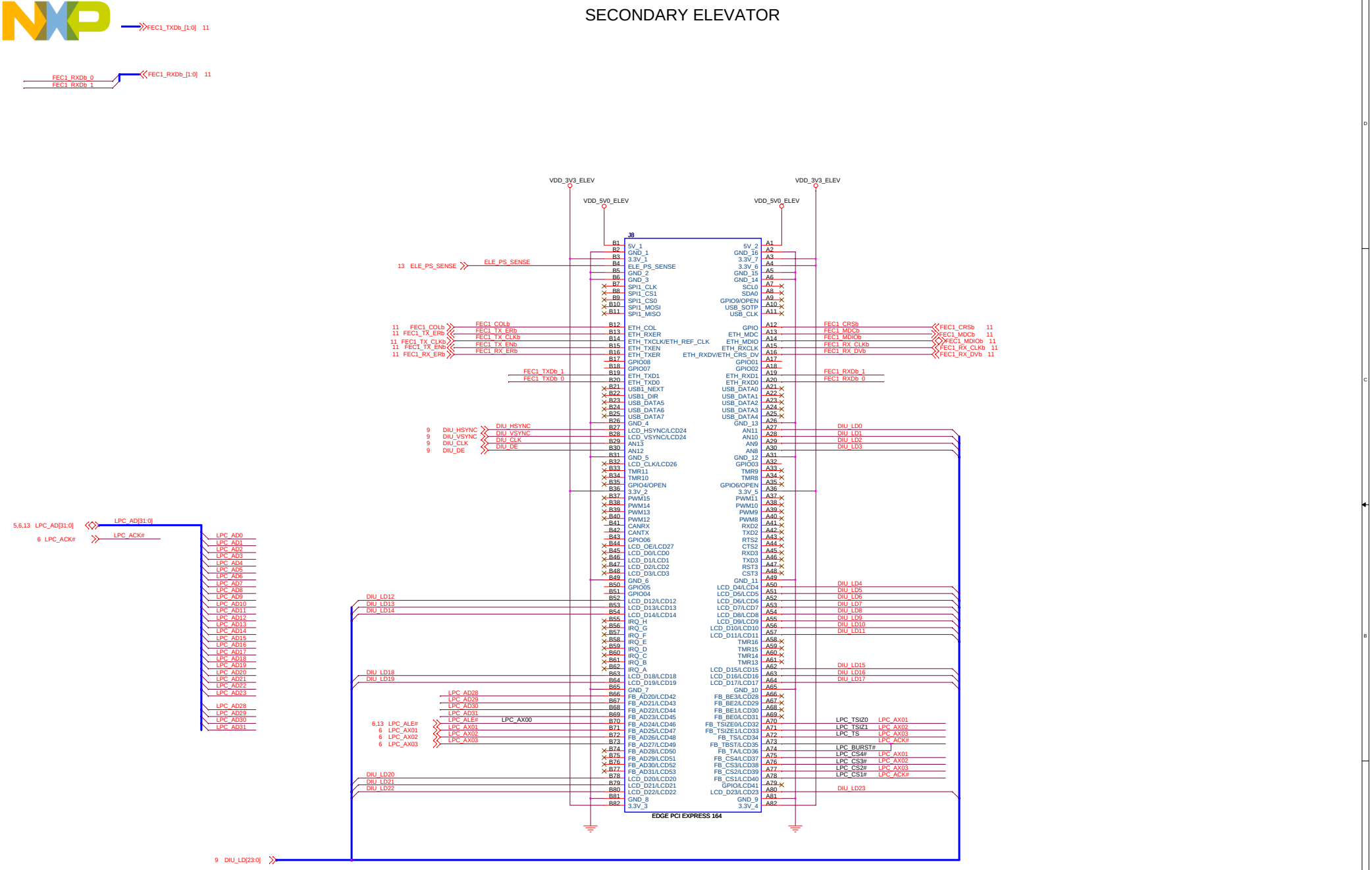
Title	DDR2 MEMORIES_TERMINATIONS	
Size C	Document Number TWR-MPC5125	Rev v2.1
Date: Wednesday, February 24, 2010	Sheet 12 of 17	

MAIN ELEVATOR



Title	TOWER EXP - MAIN ELEVATOR
Size	C
Document Number	TWR-MPC5125
Rev	v2.1
Date:	Friday, February 26, 2010
Sheet	13 of 17

SECONDARY ELEVATOR

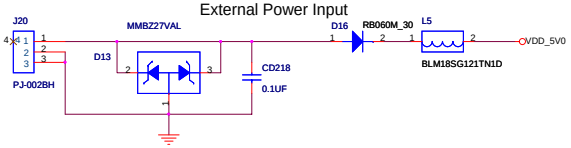


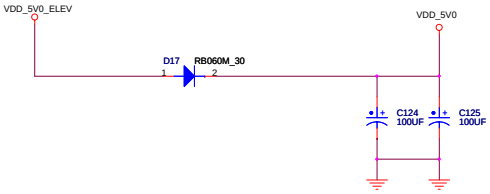
Made by www.Limepc.com

Title	TOWER EXP - SECOND ELEVATOR	
Size C	Document Number TWR-MPC5125	Rev v2.1
Date: Wednesday, February 24, 2010	Sheet 14 of 17	

POWER SUPPLY

External Power Input

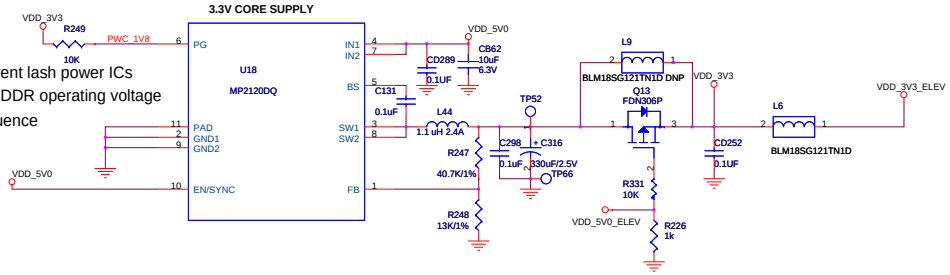


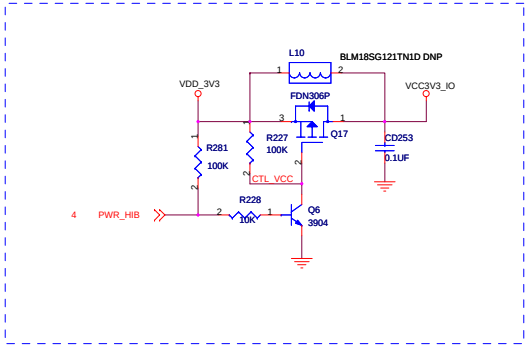


Notes:

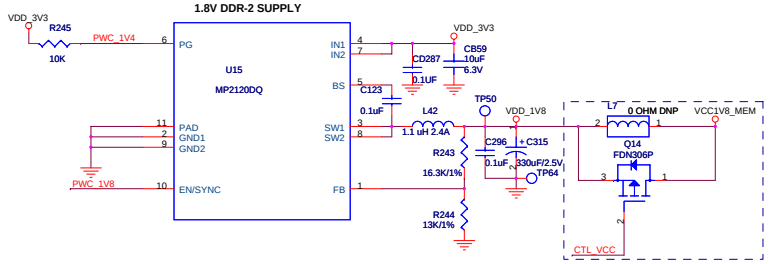
1. prevent the external current lash power ICs
   Protection the CPU and DDR operating voltage
2. Ensure Powerup Sequence

3.3V @ 2.5A POWER SUPPLY

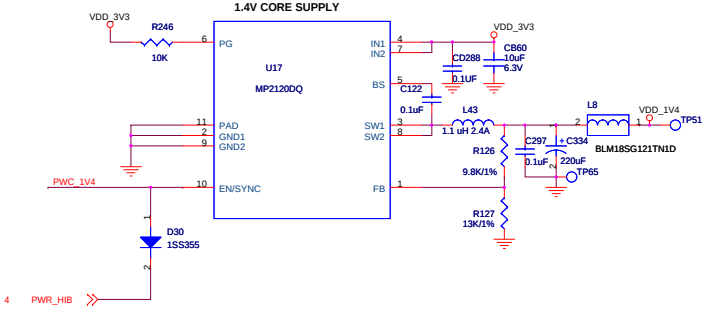




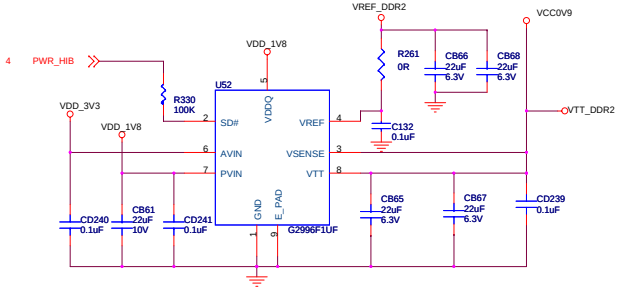
1.8V @ 2.5A POWER SUPPLY



1.4V @ 2.5A POWER SUPPLY

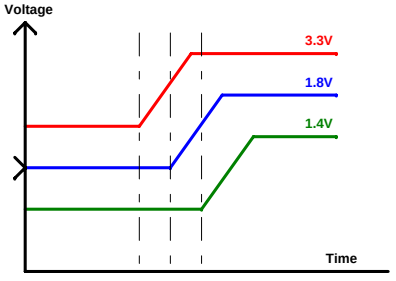


DDR-2 TERMINATION REG



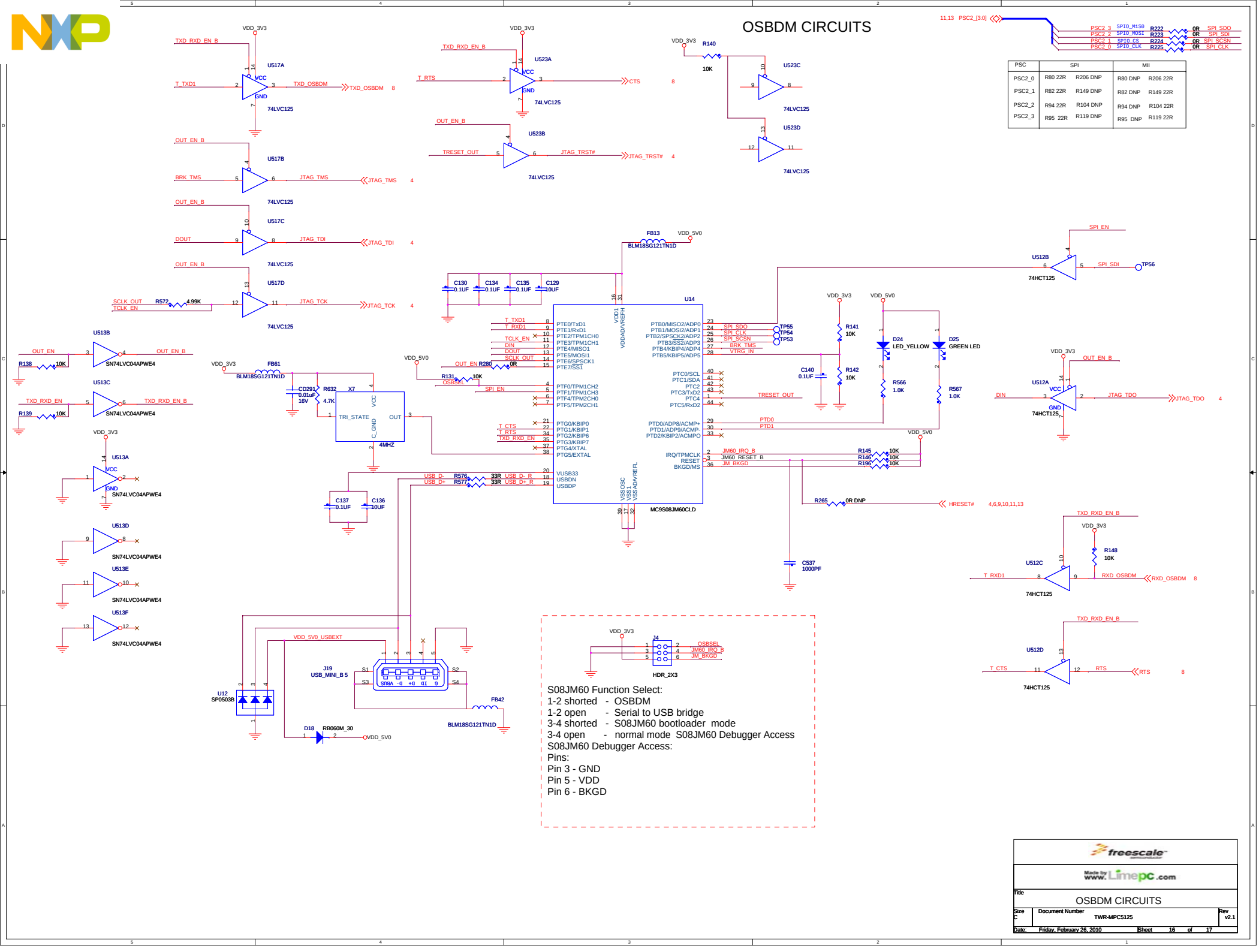
Note
---
1. Route VSENSE line as a trace and connect it to the VTT power plane near the DDR-2 memories
2. Provide Ground Gaurd to the Vsense line

Powerup Sequence



Title	POWER SUPPLY	
Size C	Document Number TWR-MPC5125	Rev v2.1
Date: Wednesday, February 24, 2010	Sheet 15 of 17	

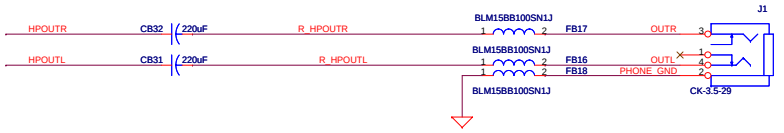
OSBDM CIRCUITS

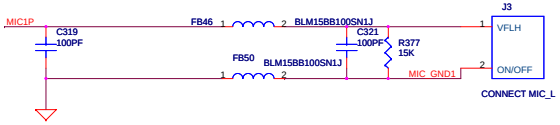


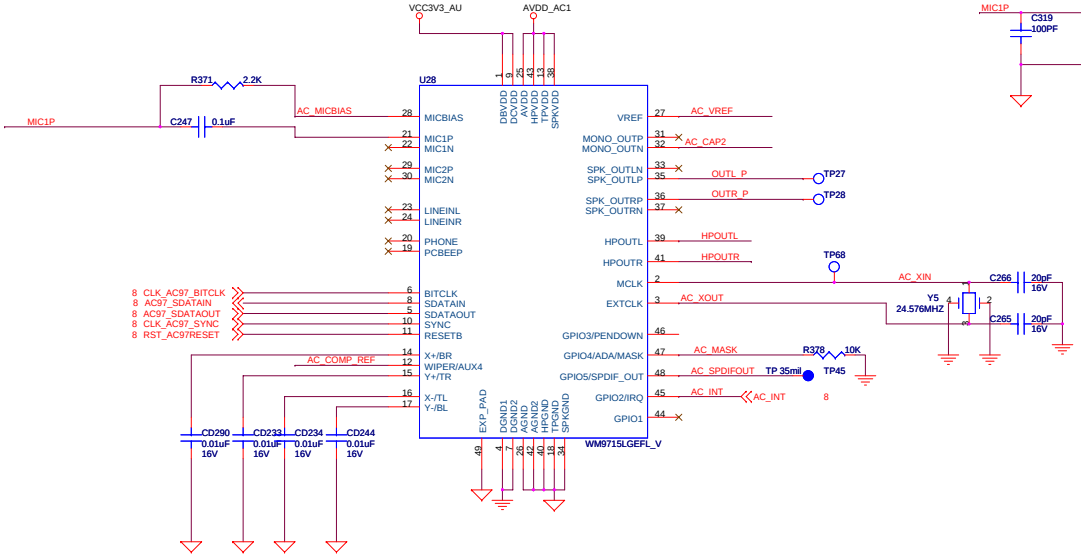
S08JM60 Function Select:
1-2 shorted - OSBDM
1-2 open - Serial to USB bridge
3-4 shorted - S08JM60 bootloader mode
3-4 open - normal mode S08JM60 Debugger Access
S08JM60 Debugger Access:
Pins:
Pin 3 - GND
Pin 5 - VDD
Pin 6 - BKGD

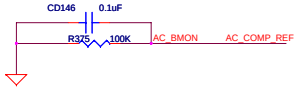
Title	OSBDM CIRCUITS
Size C	Document Number TWR-MPC5125
Rev	v2.1
Date:	Friday, February 26, 2010
Sheet	16 of 17

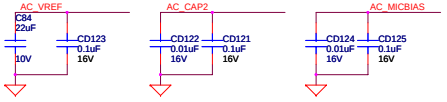
AC97 AND SD

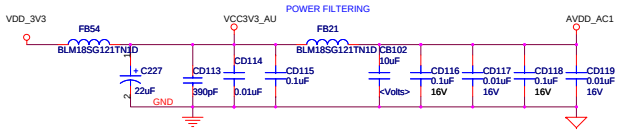


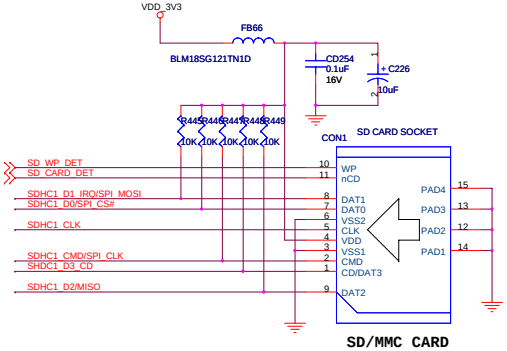












Layout Note: Connect the GND and AGND1 underneath CODEC (U11) with multiple Vias.

freescale semiconductor

Made by www.Limepc.com

Title	OSBDM CIRCUITS	
Size: C	Document Number: TWR-MPC5125	Rev: v2.1
Date: Wednesday, February 24, 2010	Sheet 17 of 17	