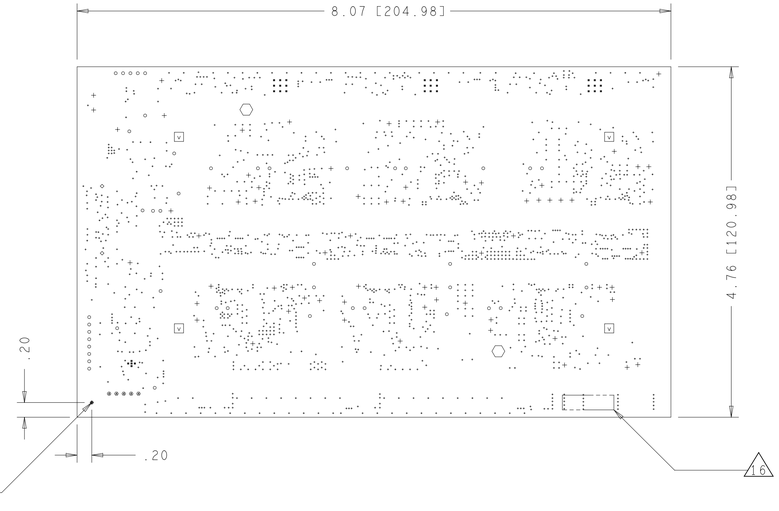
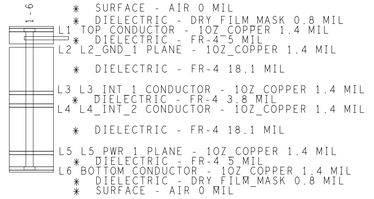
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	ORIGINAL RELEASE	03-27-19	D.N.
	D	ENGINEERING CHANGES	02-19-20	J.S.
	D1	ADDED RoHS/REACH NOTE	06-09-21	D.A.

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - NONE
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.005"
7. PLATING FINISH: A. BOTH SIDES GOLD: 2-15 MICROINCHES OF GOLD OVER 100-350 MICROINCHES NICKEL.
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
   GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DFM CHECK MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. TWO SOLDER SAMPLES TO BE PROVIDED.
16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (e4)
18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.
20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
21. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS, KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.
22. THIS BOARD USES VIA-IN-PAD:
    A. VIA-IN-PAD TO BE FILLED WITH NON-CONDUCTIVE VIA FILL. LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.
    B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.
    C. DIMPLE OR PROTRUSION ON VIA-IN-PADS MUST BE NO GREATER THAN .001".



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
+	10.0	+0.0/-10.0	PLATED	1716
VIA	10.1	+0.0/-10.1	PLATED	32
○	40.0	+3.0/-3.0	PLATED	48
⊕	43.0	+3.0/-3.0	PLATED	5
+	63.0	+3.0/-3.0	PLATED	67
◇	47.0	+2.0/-2.0	NON-PLATED	2
▽	150.0	+2.0/-2.0	NON-PLATED	4
○	250.0	+2.0/-2.0	NON-PLATED	2



DESIGN CROSS SECTION CHART
TOTAL THICKNESS 60 MIL

BOARD THICKNESS TOLERANCE +/-10%

DETAIL A
LAYER STACKUP
SCALE: NONE

___ COMPANY PUBLIC
_X_ COMPANY INTERNAL
___ COMPANY CONFIDENTIAL

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL MEET THE RoHS COMMISSION DELEGATED DIRECTIVE (EU) 2015/863 OF 31 MARCH 2015 AMENDING ANNEX II TO DIRECTIVE 2011/65/EU. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL NOT CONTAIN ANY OF THE SUBSTANCES OF VERY HIGH CONCERN (SVHC) ABOVE THE THRESHOLD VALUE PER THE CURRENT ECHA LIST OF SVHC'S AND WITH ANNEX XIV AND ANNEX XVII OF REACH DIRECTIVE 1907/2006. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±0-30'
.XXX ±.005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN	
DARRELL SLUPEK	02-27-19
CHECKED	
DANIEL NEDELEA	02-27-19
DESIGN ENGINEER	
CATALIN BUNDA	02-27-19

PART NO. 170-38863

NXP SEMICONDUCTORS

6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
RDGD3100I3PH5EVB

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-38863	FAB-38863	D1

SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 2

NOTES (UNLESS OTHERWISE SPECIFIED):

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	ORIGINAL RELEASE	03-27-19	D.N.
	D	ENGINEERING CHANGES	02-19-20	J.S.
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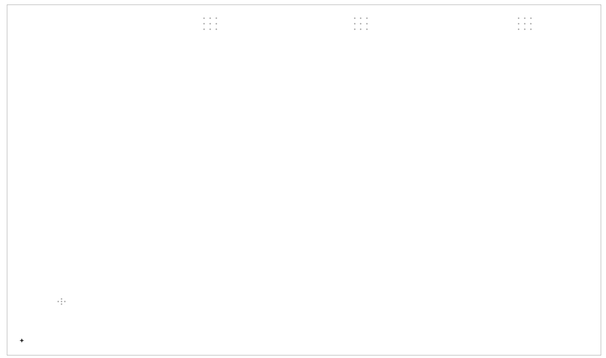

22 THIS FAB_VIAFILL.ART SHOWS LOCATIONS OF VIA-IN-PAD TO BE FILLED.

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL MEET THE RoHS COMMISSION DELEGATED DIRECTIVE (EU) 2015/863 OF 31 MARCH, 2015 AMENDING ANNEX II TO DIRECTIVE 2011/65/EU. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL NOT CONTAIN ANY OF THE SUBSTANCES OF VERY HIGH CONCERN (SVHC) ABOVE THE THRESHOLD VALUE PER THE CURRENT ECHA LIST OF SVHC'S AND THE ANNEX XVII CANDIDATE LIST OF REACH REGULATION. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

___ COMPANY PUBLIC
X COMPANY INTERNAL
___ COMPANY CONFIDENTIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±0-30'
.XXX ±.005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

PART NO. 170-38863

APPROVALS	DATE
DRAWN: DARRELL SLUPEK	02-27-19
CHECKED: DANIEL NEDELEA	02-27-19
DESIGN ENGINEER: CATALIN BUNDA	02-27-19

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
RDGD3100I3PH5EVB

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-38863	FAB-38863	D1

SCALE DO NOT SCALE DRAWING SHEET 2 OF 2