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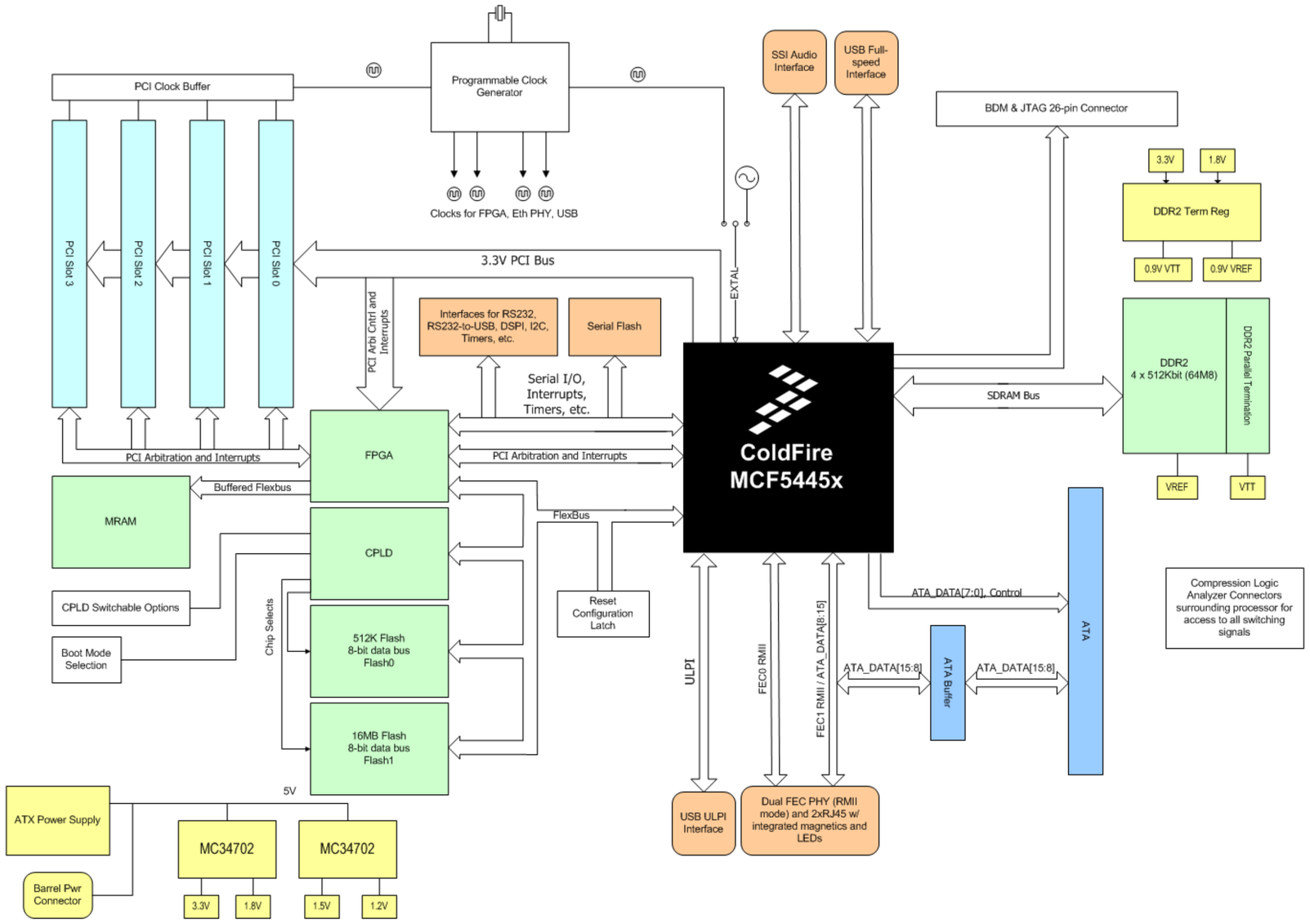
Revisions

Rev	Description	Date	Approved
X1	Original Draft	11/08/06	J.W.
X2	Fixed Flash1, serial port interfaces, etc.	07/03/07	M.N.



freescale semiconductor

Transportation & Standard Products Group
6501 William Cannon Drive West
Austin, TX 78735-8598

Designer: M.Norman & J.Smith	Drawing Title: **M54455EVB**	
Drawn by: DEVTECH CAD - RO	Page Title: **TITLE PAGE**	
Approved: JOHN WEIL	Size C	Document Number PDF: SPF-22131 SOURCE: SCH-22131 — Rev B
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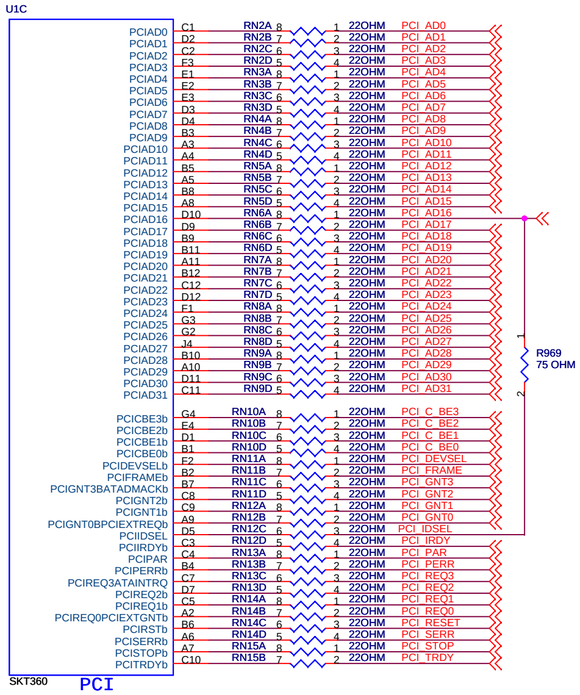
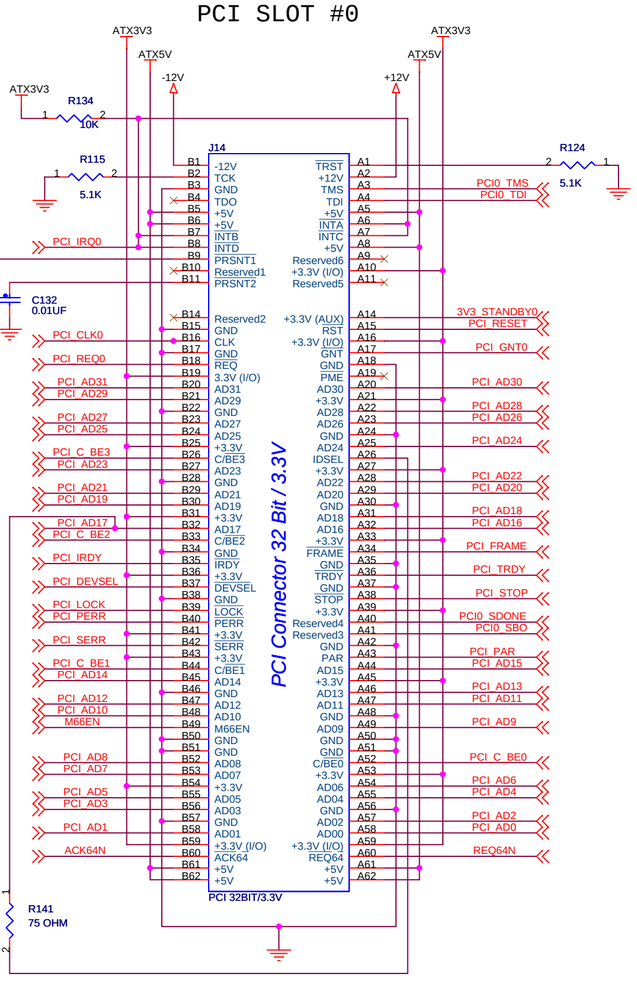
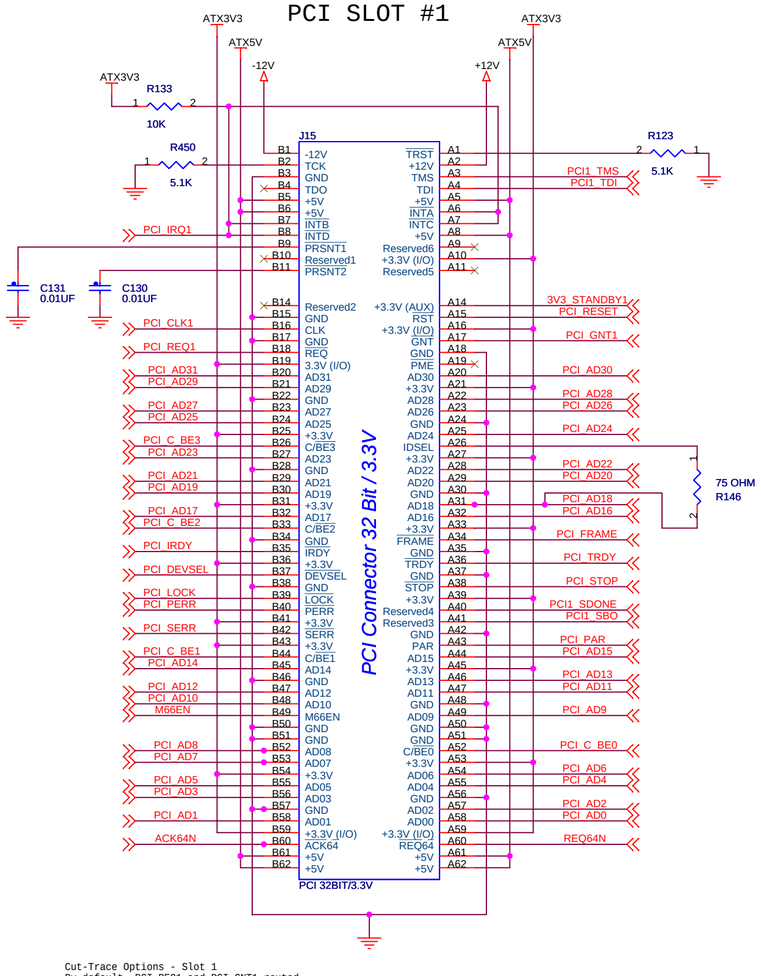
PCI SLOT #0



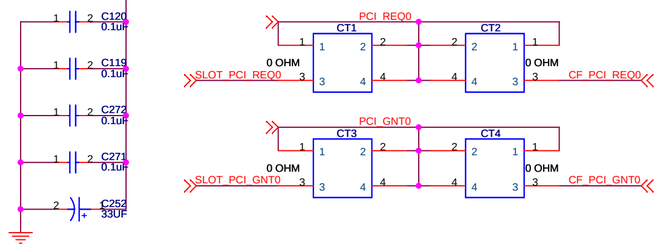
Cut-Trace Options - Slot 0
By default, PCI_REQ0 and PCI_GNT0 routed directly to PCI Slot 0.
To route through FPGA, cut trace between 1 and 2 on CT1 and solder 1 to 3. Then, cut trace between 1 and 2 on CT2 and solder 1 to 3. Repeat this process for CT3 and CT4.

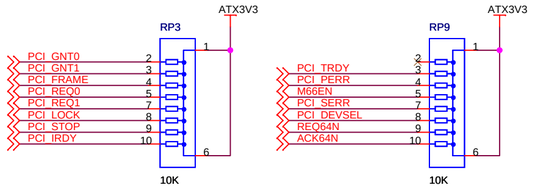


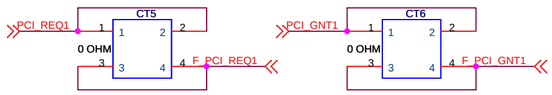
PCI SLOT #1

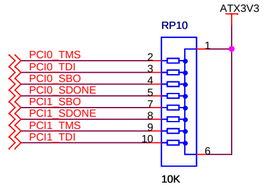


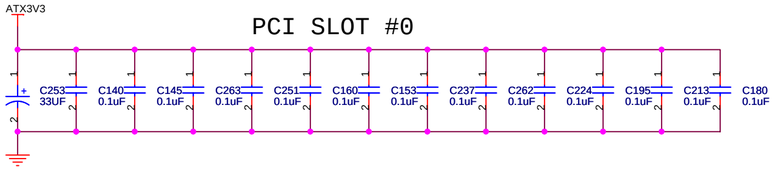
Cut-Trace Options - Slot 1
By default, PCI_REQ1 and PCI_GNT1 routed directly to PCI Slot 1 from U1.
To route through FPGA, cut trace between 1 and 2 on CT5 and solder 1 to 3. Then, cut trace between 1 and 2 on CT6 and solder 1 to 3.

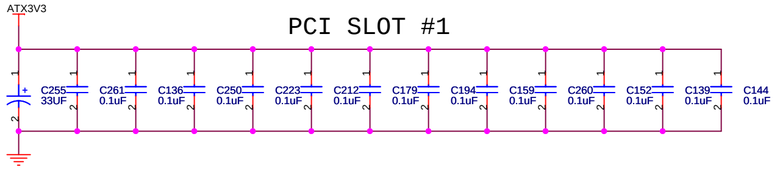


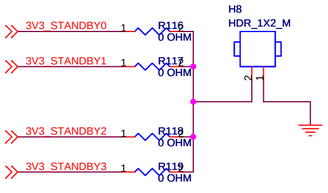


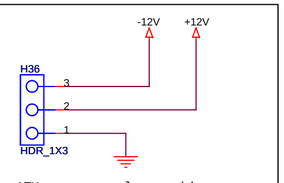








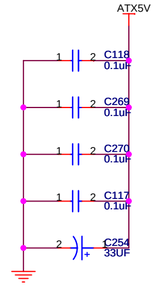




The ATX power supply provides +/- 12V power to the connectors. This header can be used to monitor the supply.

PCI Notes:

1. CF_PCI_GNTn and CF_PCI_REQn signals connect to the FPGA. PCI_GNTn and PCI_REQn signals are connected from the FPGA to the PCI slots.
2. PCI Slot #0 uses PCI_REQ0 and PCI_GNT0
   PCI Slot #1 uses PCI_REQ1 and PCI_GNT1
   PCI Slot #2 uses PCI_REQ2 and PCI_GNT2
   PCI Slot #3 uses PCI_REQ3 and PCI_GNT3
3. MCF5445x IDSEL connected to PCI_AD16
   PCI Slot #0 IDSEL connected to PCI_AD17
   PCI Slot #1 IDSEL connected to PCI_AD18
   PCI Slot #2 IDSEL connected to PCI_AD19
   PCI Slot #3 IDSEL connected to PCI_AD20
4. The FPGA gathers interrupts from the PCI slots.
5. JTAG is unusable on PCI connectors



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Drawing Title: M54455EVB

Page Title: PCI SLOT #0 AND #1

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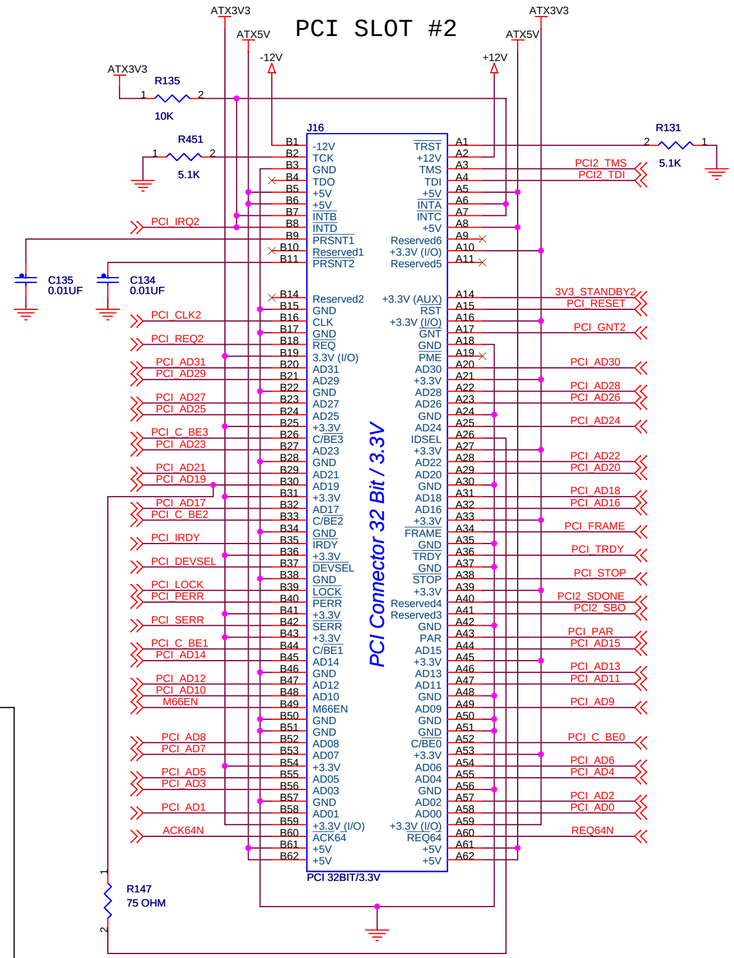
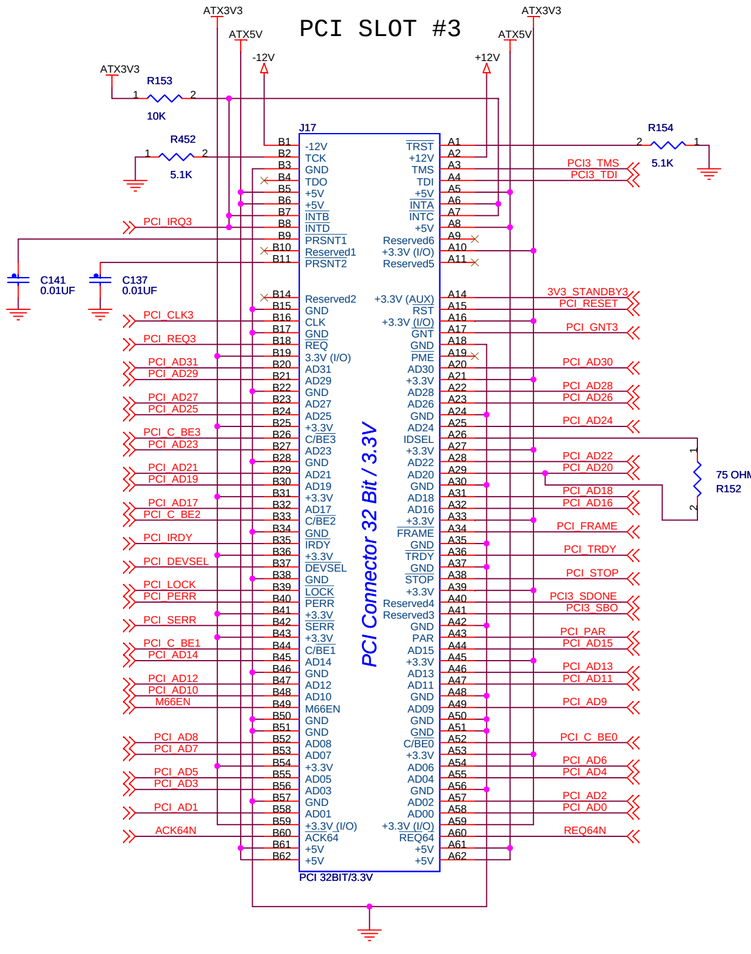


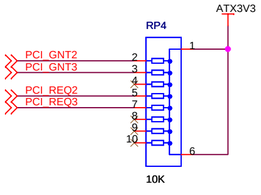


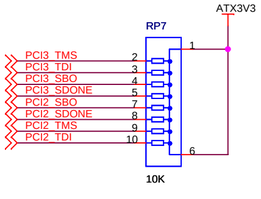
PCI Notes:

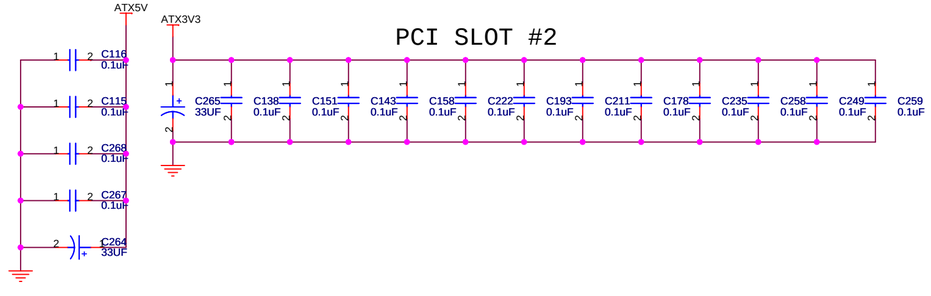
1. CF_PCI_GNTn and CF_PCI_REQn signals connect to the FPGA. PCI_GNTn and PCI_REQn signals are connected from the FPGA to the PCI slots.
2. PCI Slot #0 uses PCI_REQ0 and PCI_GNT0
   PCI Slot #1 uses PCI_REQ1 and PCI_GNT1
   PCI Slot #2 uses PCI_REQ2 and PCI_GNT2
   PCI Slot #3 uses PCI_REQ3 and PCI_GNT3
3. MCF5445x IDSEL connected to PCI_AD16
   PCI Slot #0 IDSEL connected to PCI_AD17
   PCI Slot #1 IDSEL connected to PCI_AD18
   PCI Slot #2 IDSEL connected to PCI_AD19
   PCI Slot #3 IDSEL connected to PCI_AD20
4. The FPGA gathers interrupts from the PCI slots.
5. JTAG is unusable on PCI connectors

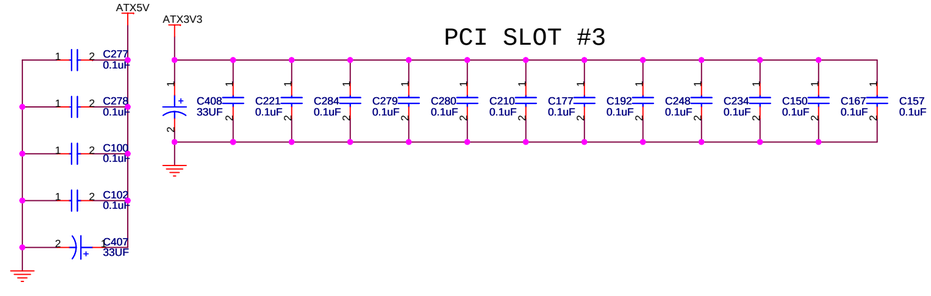
Cut-Trace Options - Slot 2
By default, PCI_REQ2 and PCI_GNT2 routed directly to PCI Slot 2 from U1.
To route through FPGA, cut trace between 1 and 2 on CT7 and solder 1 to 3. Then, cut trace between 1 and 2 on CT8 and solder 1 to 3.

Cut-Trace Options - Slot 3
By default, PCI_REQ3 and PCI_GNT3 routed directly to PCI Slot 3 from U1.
To route through FPGA, cut trace between 1 and 2 on CT9 and solder 1 to 3. Then, cut trace between 1 and 2 on CT10 and solder 1 to 3.









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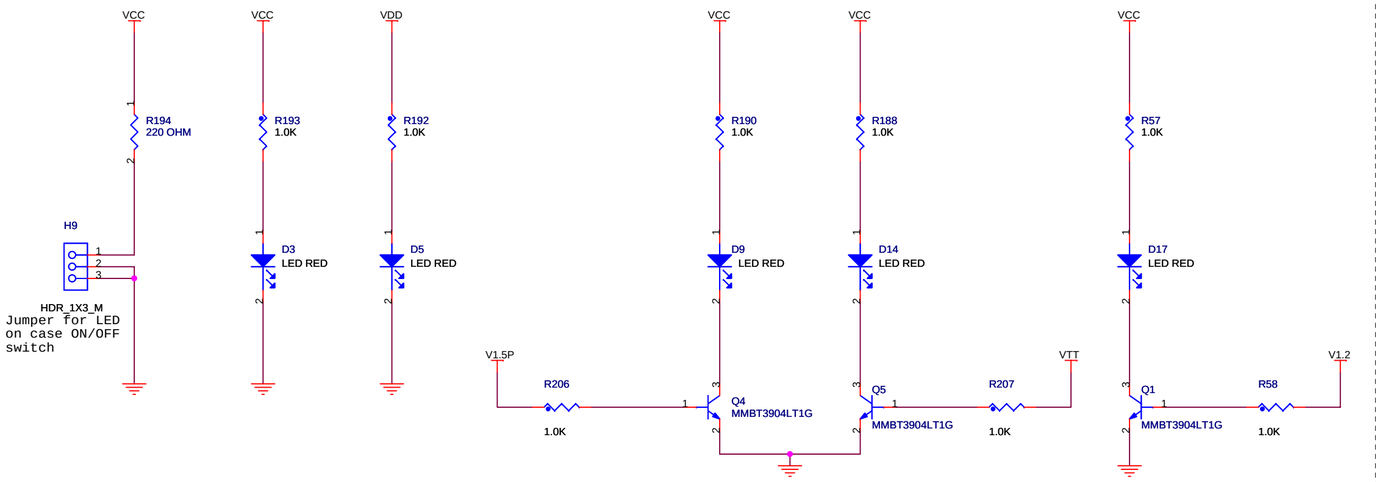
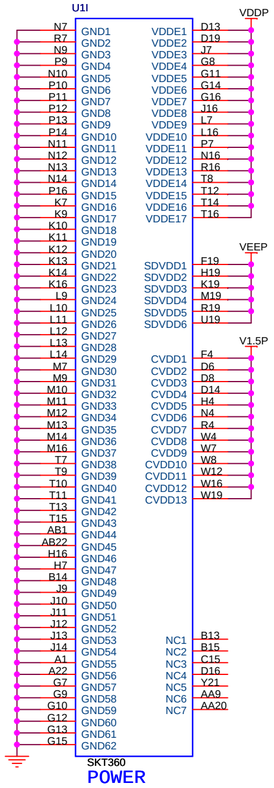
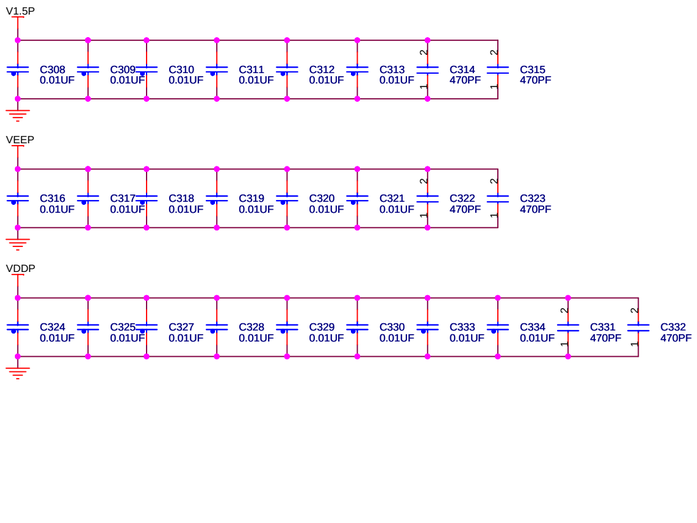
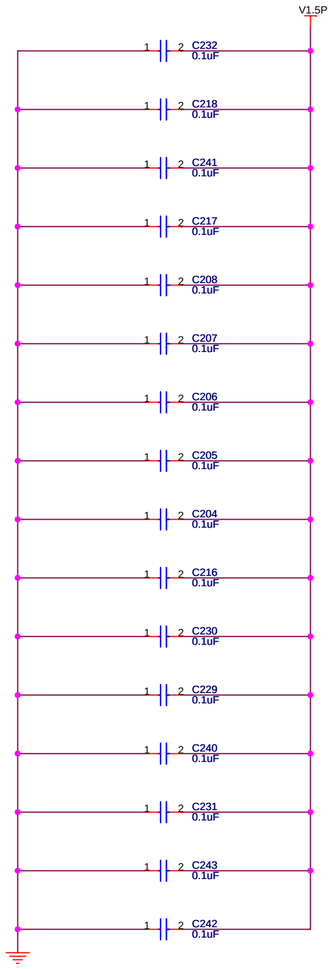
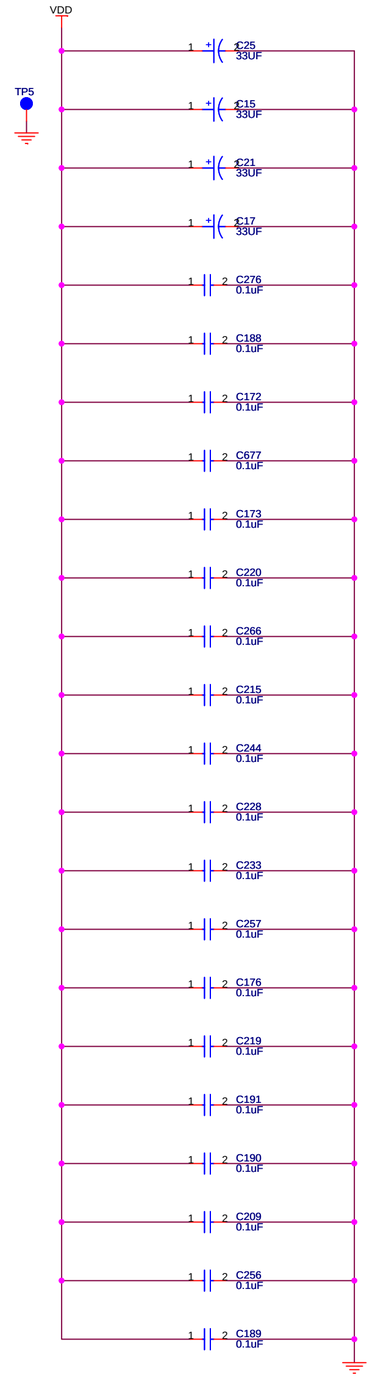
Power Indicators

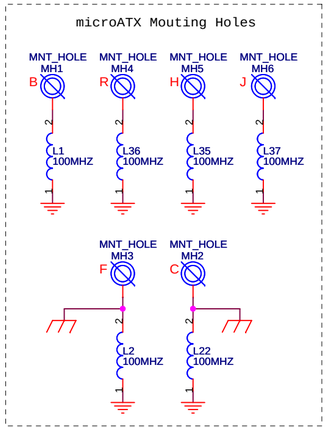












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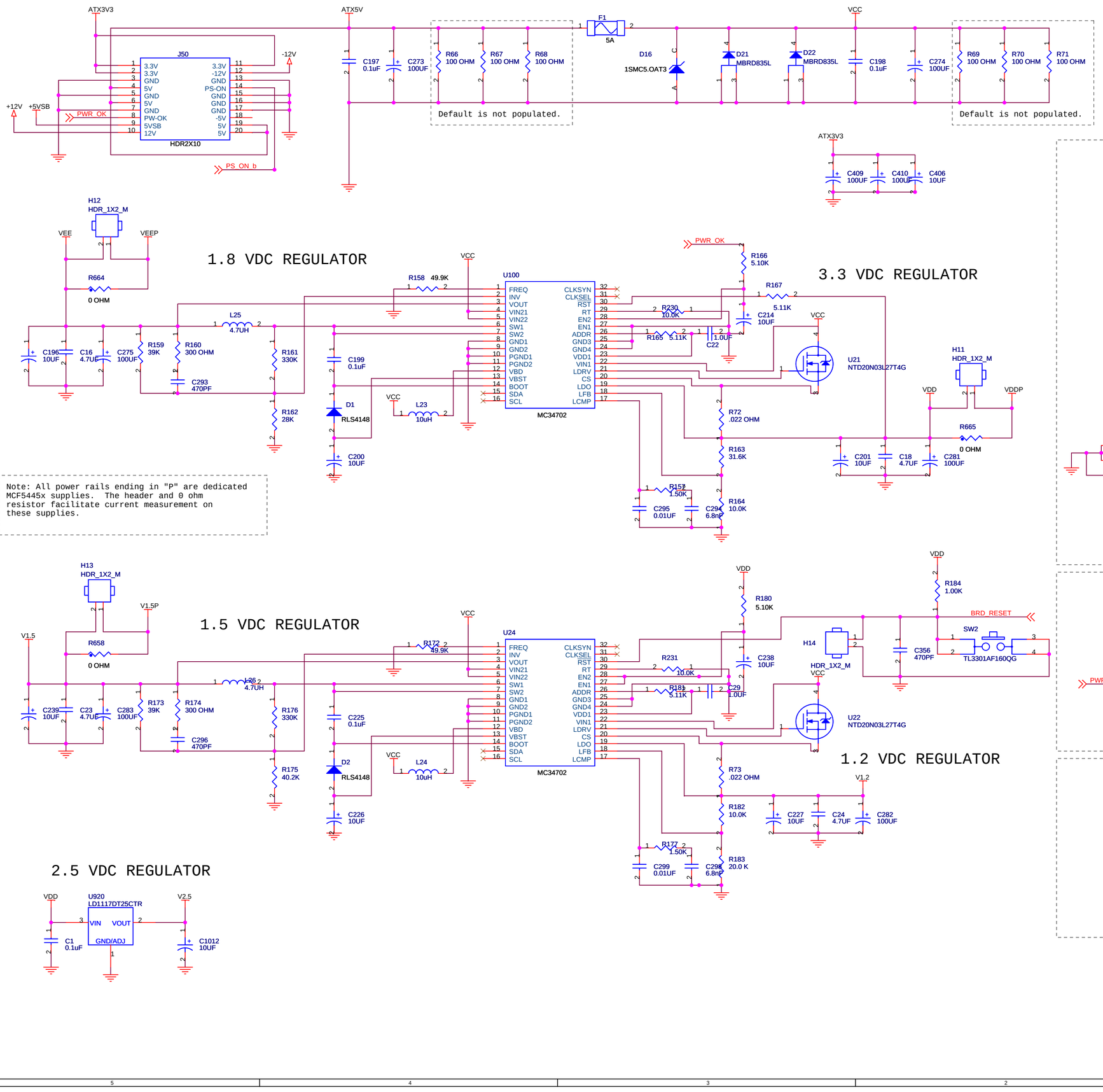

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To ATA Interface

FEC1_RMII_TXD1
FEC1_RMII_TXD0
FEC1_RMII_TXEN
FEC1_RMII_RXD1
FEC1_RMII_RXD0
FEC1_RMII_RXER
FEC1_RMII_CRS_DV
FEC1_RMII_REF_CLK
RMIICLK2

U1Q
FEC1TXCLKFEC1RMIIREFCLKATADATA11 AB19 FEC1_RMII_REF_CLK
FEC1TXENFEC1RMIITXENATADATA8 AA21 FEC1_RMII_TXEN
FEC1TXD0FEC1RMIITXD0ATADATA9 Y20 FEC1_RMII_TXD0
FEC1TXD1FEC1RMIITXD1ATADATA10 AA19 FEC1_RMII_TXD1
FEC1RXDVFEC1RMIICRSDVATADATA15 AB15 FEC1_RMII_CRS_DV
FEC1RXERFEC1RMIIRXERATADATA12 W17 FEC1_RMII_RXER
FEC1RXD0FEC1RMIIRXD0ATADATA13 Y17 FEC1_RMII_RXD0
FEC1RXD1FEC1RMIIRXD1ATADATA14 AA17 FEC1_RMII_RXD1
SKT360
FEC1_RMII

U1B
FEC0MDC AB8 FEC0_MDC
FEC0MDIO Y7 FEC0_MDIO
FEC0RXDVFEC0RMIICRSDV Y8 FEC0_RMII_CRS_DV
FEC0RXD0FEC0RMIIRXD0 AB10 FEC_RMII_RXD0
FEC0RXD1FEC0RMIIRXD1 W9 FEC0_RMII_RXD1
FEC0RXERFEC0RMIIRXER AA10 FEC_RMII_RXER
FEC0TXCLKFEC0RMIIREFCLK Y10
FEC0TXD0FEC0RMIITXD0 Y11 FEC_RMII_TXD0
FEC0TXD1FEC0RMIITXD1 AA11 FEC_RMII_TXD1
FEC0TXENFEC0RMIITXEN W11 FEC0_RMII_TXEN
SKT360
FECO/RMII

RMIICLK1
RMIICLK0
CPU_RSTOUT

R944 4.7K
R946 4.7K
R945 4.7K
R947 4.7K
R948 4.7K
R949 4.87K

U901
DP83849

MDIO 66
MDC 67
TXD3_B/SNI_MODE_B 45
TXD2_B 46
TXD1_B 47
TXD0_B 48
TX_EN_B 49
TX_CLK_B 50
RXD3_B/ED_EN_B 53
RXD2_B/EXTENDER_EN 56
RXD1_B/PHYAD4 57
RXD0_B/PHAD3 58
COL_B/FX_EN_B 59
RX_ER_B/MDIX_EN_B 60
CRS_B/CRS_DV_B/LED_CFG_B 61
RX_DV_B/MII_MODE_B 62
RX_CLK_B 63
RX_CLK_A 79
RX_DV_A/MII_MODE_A 80
CRS_A/CRS_DV_A/LED_CFG_A 1
RX_ER_A/MDIX_EN_A 2
COL_A/FX_EN_A 3
RXD0_A/PHYAD1 4
RXD1_A/PHYAD2 5
RXD2_A/CLK2MAC_DIS 8
RXD3_A/ED_EN_A 9
TX_CLK_A 12
TX_EN_A 13
TXD0_A 14
TXD1_A 15
TXD2_A 16
TXD3_A/SNI_MODE_A 17
X2 69
X1 70
RESET_N 71
ANA33V/DD 30
IOVDD1 11
IOVDD2 55
IOVDD3 65
IOVDD4 78
PFBOUT 31
PFBN2 28
PFBN3 34
PFBN1 7
PFBN4 54
ANAGND1 22
ANAGND2 29
ANAGND3 33
ANAGND4 40
IOGND1 10
IOGND2 52
IOGND3 64
IOGND4 77
CDGND1 25
CDGND2 37
COREGND1 6
COREGND2 55
CLK2MAC 68
PWRDOWN_INT_B 44 PHY1_PWRDN
PWRDOWN_INT_A 18 PHY0_PWRDN
LED_LINK_B/AN0_B 43
LED_SPEED_B/FXSD_B/AN1_B 42
LED_ACT/COL_B/AN_EN_B 41
TPTDM_B/FXRDM_B 39
TPTDP_B/FXRDP_B 38
TPTDM_B/FXTDM_B 36
TPTDP_B/FXTDP_B 35
TPTDP_A/FXTDP_A 27
TPTDM_A/FXTDM_A 26
TPRDP_A/FXRDP_A 24
TPRDM_A/FXRDM_A 23
LED_ACT/COL_A/AN_EN_A 21
LED_SPEED_A/FXSD_A/AN1_A 20
LED_LINK_A/AN0_A 19
TDI 76
TRSTN 75
TMS 74
TDO 73
TCK 72
RBIAS 32

R951 49.9 OHM
R765 49.9 OHM
C950 0.1uF
R952 49.9 OHM
R953 49.9 OHM
C766 0.1uF
R950 220 OHM
C952 0.1uF
C765 0.1uF

P5B Upper Port
ETH1_TXD- 13 TRD1- RJ1 TRP1+
ETH1_TXD_CT 7 TRCT1
ETH1_TXD+ 6 TRD1+ RJ2 TRP1-
ETH1_RXD- 5 TRD2- RJ3 TRP2+
ETH1_RXD_CT 12 TRCT2
ETH1_RXD+ 11 TRD2+ RJ6 TRP2-
10 TRD3- RJ4 TRP3+
4 TRCT3
3 TRD3+ RJ5 TRP3-
2 TRD4- RJ7 TRP4+
9 TRCT4
8 TRD4+ RJ8 TRP4-
1 GND2
ETH1_LED_LINK- 31 LED3_C
ETH1_LED_LINK+ 32 LED3_A
R587 220 OHM
ETH1_LED_SC- 33 LED4_GC
ETH1_LED_SC+ 34 LED4_GA
Chassis_GND
Chassis_GND
S3
S4
0845-2R1T-E4

Ethernet Channel 1

LED1 indicates a LINK and blinks for activity.

LED2 indicates Speed (10/100 Mbps) and Collision (when in 10 Mbps mode). LED2 is GREEN for 100Mbps mode, OFF for 10Mbps, and blinking ORANGE for Collisions.

R955 49.9 OHM
R956 49.9 OHM
C957 0.1uF
R958 49.9 OHM
R957 49.9 OHM
C954 0.1uF
R959 220 OHM
C955 0.1uF
C956 0.1uF

P5A Lower Port
ETH0_TXD- 21 TRD1- RJ1 TRP1+
ETH0_TXD_CT 14 TRCT1
ETH0_TXD+ 15 TRD1+ RJ2 TRP1-
ETH0_RXD- 16 TRD2- RJ3 TRP2+
ETH0_RXD_CT 22 TRCT2
ETH0_RXD+ 23 TRD2+ RJ6 TRP2-
24 TRD3- RJ4 TRP3+
17 TRCT3
18 TRD3+ RJ5 TRP3-
19 TRD4- RJ7 TRP4+
25 TRCT4
26 TRD4+ RJ8 TRP4-
20 GND1
ETH0_LED_LINK- 27 LED1_C
ETH0_LED_LINK+ 28 LED1_A
R954 220 OHM
ETH0_LED_SC- 29 LED2_GC
ETH0_LED_SC+ 30 LED2_GA
Chassis_GND
Chassis_GND
S1
S2
0845-2R1T-E4

Ethernet Channel 0

LED1 indicates a LINK and blinks for activity.

LED2 indicates Speed (10/100 Mbps) and Collision (when in 10 Mbps mode). LED2 is GREEN for 100Mbps mode, OFF for 10Mbps, and blinking ORANGE for Collisions.

C11 0.1uF
C12 0.1uF
C14 0.1uF
C31 0.1uF
C2 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C3 10UF
C4 0.1uF

Both ports of the Ethernet PHY are placed into RMII mode. The MII management channel is connected to the FEC0 MDC/MDIO interface only (e.g. all MII management communications must go through FEC0). The default PHY addresses of 0x0 (FEC0) and 0x1 (FEC1) are used.

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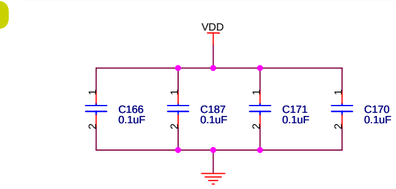

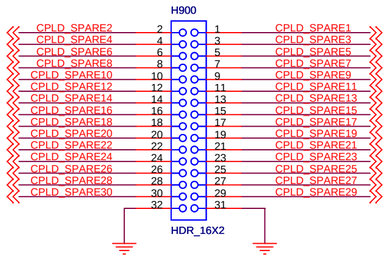

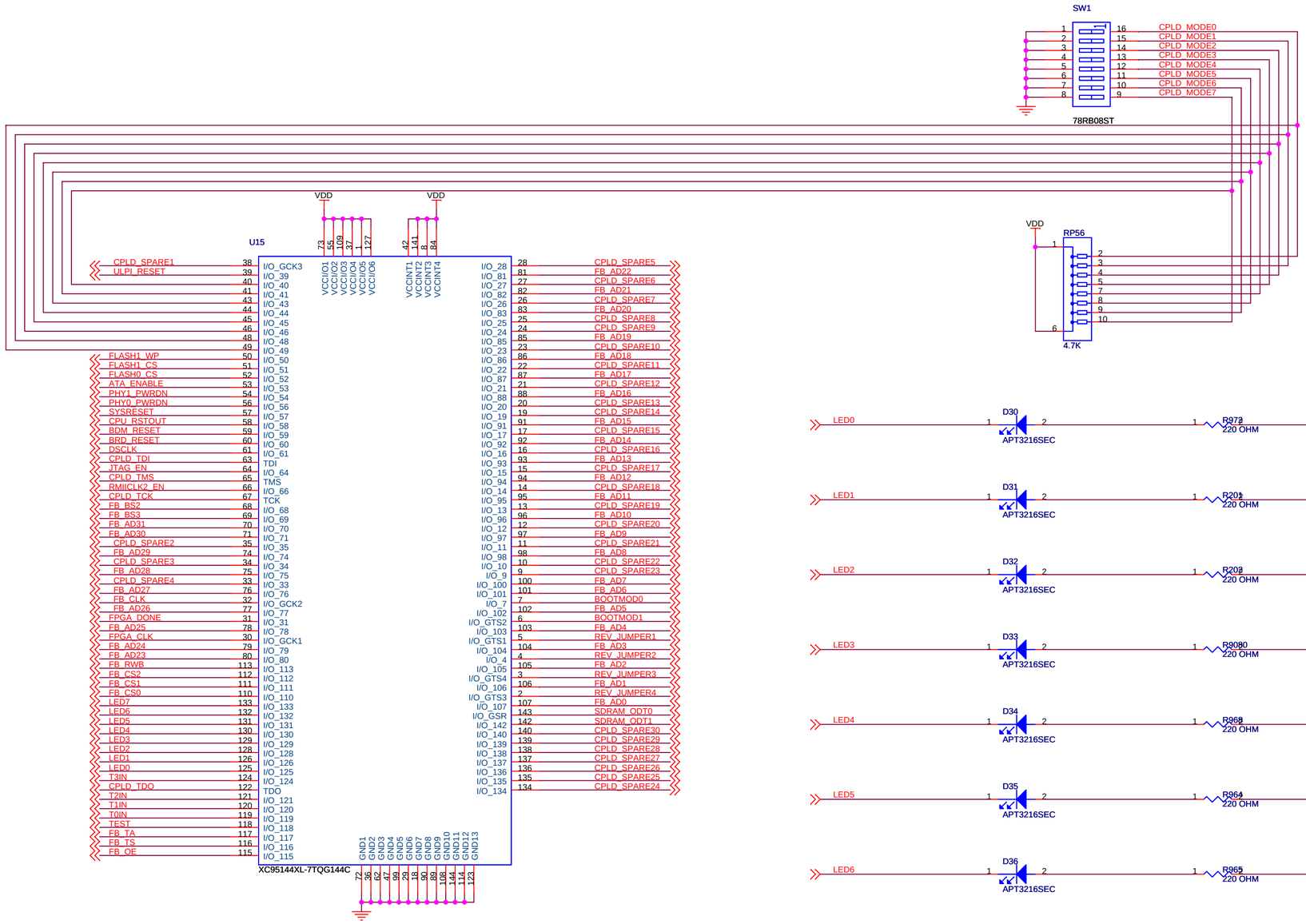

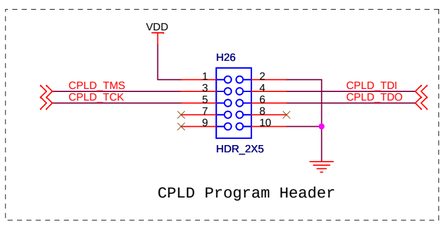

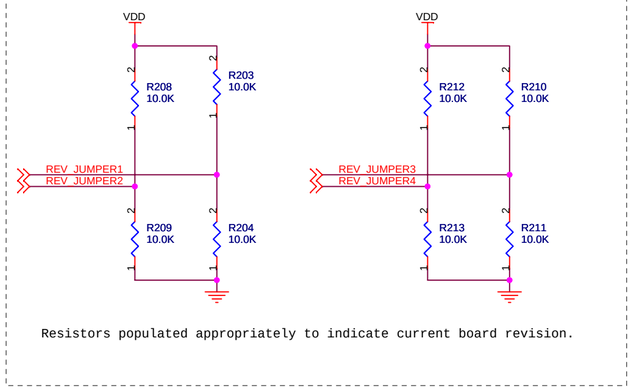

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SERIAL BOOT FLASH

PARALLEL BOOT CONFIGURATION

SW3
78RB08ST
RN16
4.7K
U902
74LV541/SO
FB_AD0
FB_AD1
FB_AD2
FB_AD3
FB_AD4
FB_AD5
FB_AD6
FB_AD7

DSPI/SBF

U1E
SKT360
DSPISCKSBFCK
DSPISINSBFDI
DSPISOUTSBFDO
DSPIPCS0DSPISSb
DSPIPCS1SCFCSb
DSPIPCS2
DSPIPCS5DSPIPCSSb
DSPI_SCK
DSPI_SOUT
DSPI_SIN
DSPI_PCS0
DSPI_PCS1
DSPI_PCS2
DSPI_PCS5
R971 4.7K
R970 4.7K
U905
M25P16-SO16
DSPI_PCS1
DSPI_SIN
DSPI_SCK
DSPI_SOUT

U906
M25P16-VMW6G
ALTERNATIVE PART, DNP

CPU_RSTOUT

RESET/BOOT MODE

U1D
SKT360
RESETb
RSTOUTb
BOOTMOD0
BOOTMOD1
TEST
TEST
BOOTMOD1
BOOTMOD0
SYSRESET

J24
HDR_2X13
CPU_RSTOUT
BDM_RESET
PSTDDATA6
PSTDDATA4
PSTDDATA2
PSTDDATA0
BKPT
DSCLK
TCLK
EXTERNAL_DSI
DSO
PSTDDATA7
PSTDDATA5
PSTDDATA3
PSTDDATA1
PSTCLK
FB_TA
DSI
EXTERNAL_DSI

R9084 100 OHM
Default is DNP

BDM/JTAG

U1F
SKT360
PSTDDATA7
PSTDDATA6
PSTDDATA5
PSTDDATA4
PSTDDATA3
PSTDDATA2
PSTDDATA1
PSTDDATA0
JTAGEN
TCLKPSTCLK
TDIDSI
TDODSO
TMSBKPTb
TRSTBDSCLK
DSCLK
TCLK_PSTCLK
JP904
HDR_1X3
R9083
22 OHM
TP1
R979 10K

BDM

RN17
4.7K
FB_TA
HDR_1X3
JP903
JTAG_EN
R976 4.7K
R977 4.7K

BKPT
DSO
PSTDDATA0
PSTDDATA1
PSTDDATA2
PSTDDATA3
TCLK_PSTCLK

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Drawing Title:	M54455EVB
Page Title:	BOOT, SBF & BDM
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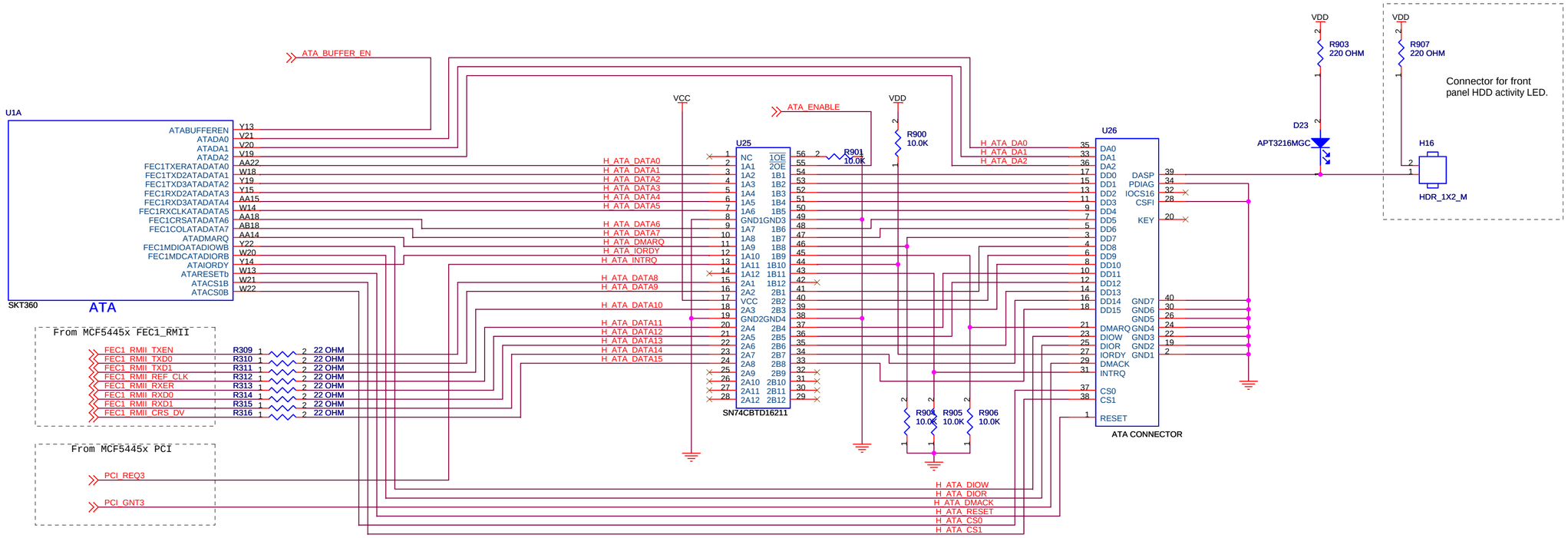

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Drawing Title:	M54455EVB	
Page Title:	ATA	
Size: C	Document Number: 870012704-100	Rev: B
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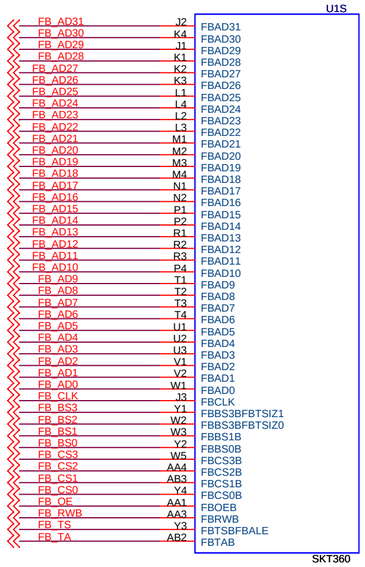
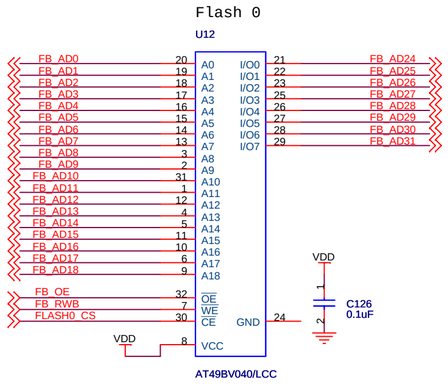
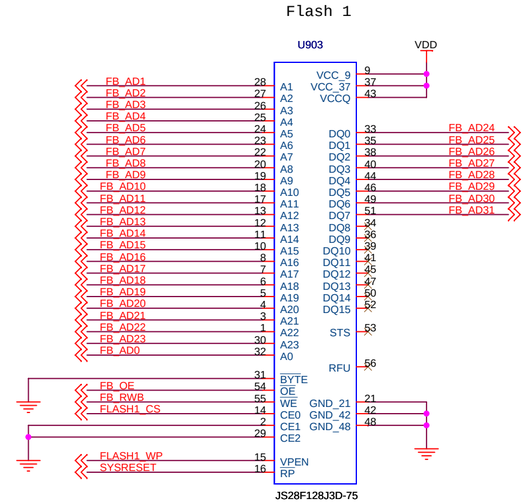
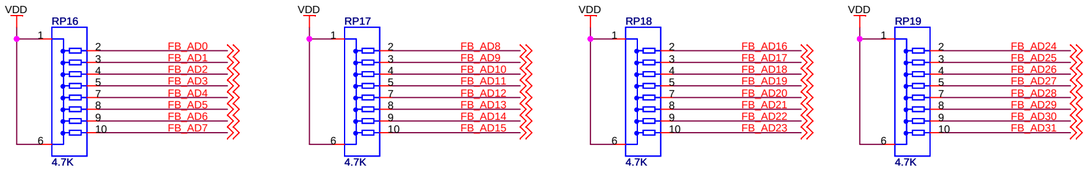
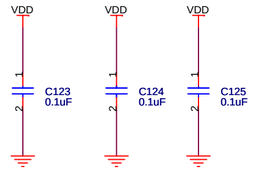






The CPLD_MODE[2] setting determines which flash device gets which chip-select (FB_CS0 or FB_CS1). The device connected to FB_CS0 is the boot device.





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Drawing Title:	M54455EVB	
Page Title:	FLASH	
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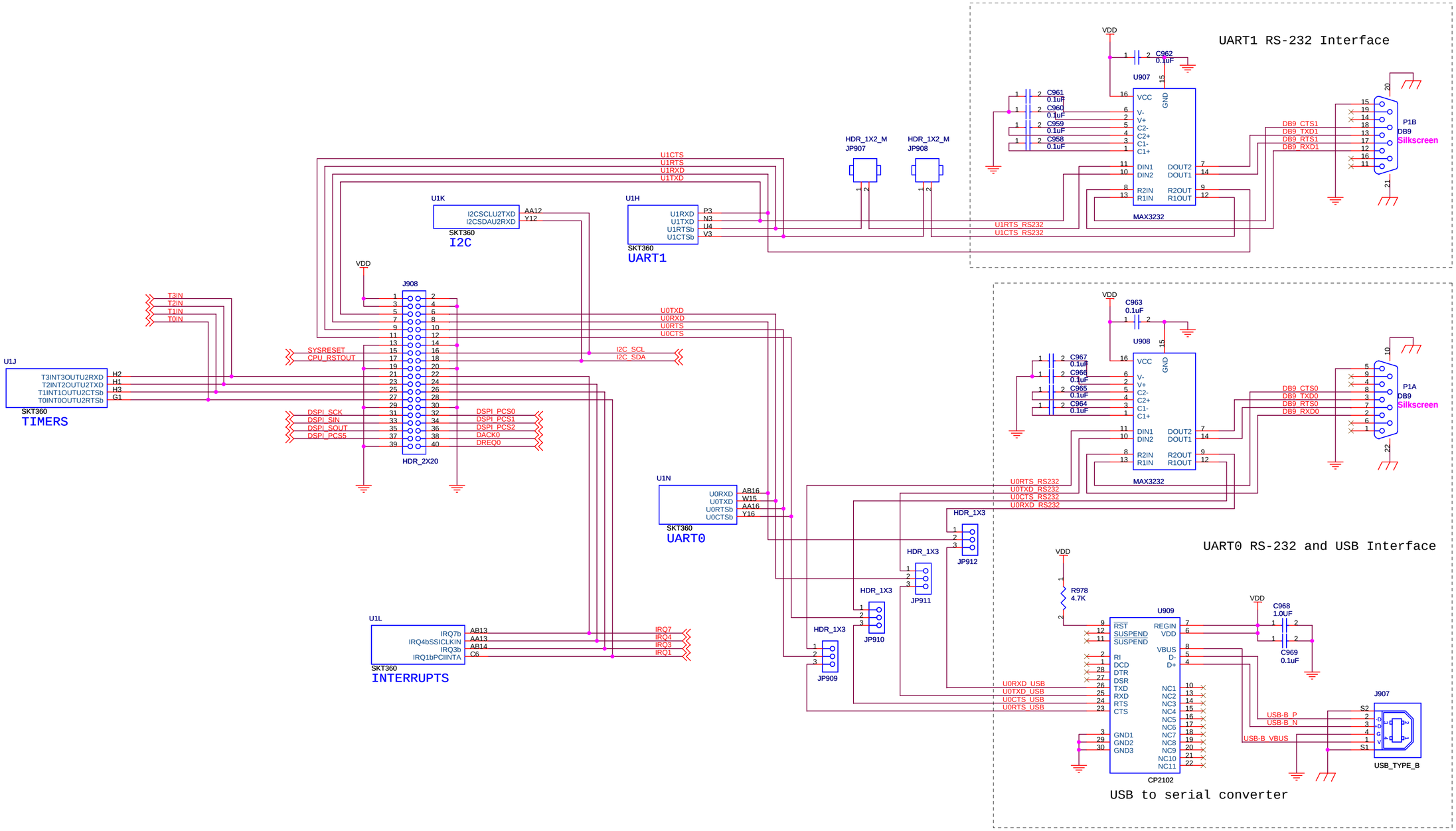

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Drawing Title:	M54455EVB	
Page Title:	SERIAL	
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CLOCKING

U1G
SKT360
XTAL32K
EXTAL32K
EXTAL
XTAL
VDDOSC
VDDRTC
VDDAPLL
VSSOSC
PLLTEST
A12 XTAL32K
A13 EXTAL32K
A16 EXTAL
A17 XTAL
B16 VDD_OSC
C13 VDD_RTC
C14 VDD_A_PLL
C16 VSS_OSC
D15

CT11
EXTAL
CPUCLK
EXTAL_OSC
0 OHM

R136 1.0M
X1 25.0 MHZ
C975 33PF
C974 33PF

R137 18M
X2 32.768MHz
C1011 15PF
C1010 15PF

VDD
R138 10 OHM
C555 1.0UF
C556 0.1uF
L27 2 100MHZ

V1.5P
R139 10 OHM
C557 1.0UF
C559 0.1uF

V1.5P
R140 10 OHM
C558 1.0UF
C560 0.1uF

H4
HDR 2X2

CLK_GEN_S2
I2C_SCL
I2C_SDA

U8
CY22393
SDAT/S0
SCLK/S1
S2/SUSPEND
SHUTDOWN/OE
VDD
AVDD
AGND
GND
XTALIN
XTALOUT
CLKA
CLKB
CLKC
CLKD
CLKE
XBUF

X3 25.0 MHZ
C127 0.1uF
C326 0.1uF

R128 22 OHM CPUCLK
R318 22 OHM
R35 22 OHM USBCLK_60
R126 22 OHM USBCLK_24
R317 22 OHM

U3
CY2309ZXC-1H
VDD CLKOUT
VDD CLKA1
CLKA2
REF CLKA3
CLKA4
S2
S1
CLKB1
CLKB2
GND CLKB3
GND CLKB4

C128 0.1uF
C335 0.1uF

22OHM RN59A RMIICLK0
22OHM RN59B RMIICLK1
22OHM RN59C RMIICLK2
22OHM RN59D

RMIICLK2_EN

RP78
4.7K

U2
CY2309ZXC-1H
RN57A PCI_CLK0
RN57B PCI_CLK1
RN57C PCI_CLK2
RN57D PCI_CLK3
RN58A PCI_CLK4
RN58B FPGA_CLK
RN58C PCI_CLK5
RN58D
22OHM

C84 0.1uF
C96 0.1uF
C85 47PF

J10 SMA
R122 0 OHM CPUCLK
R142 51 OHM

J11 SMA
R125 0 OHM
R143 51 OHM

TP4
J12 SMA
R127 0 OHM USBCLK_24
R144 51 OHM

J13 SMA
R129 0 OHM USBCLK_60
R145 51 OHM

TP3
J18 SMA
R130 0 OHM
R149 51 OHM

PCI CLOCK BUFFER

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DDR2 Parallel Termination - place near DDR2 devices

T1	SD_D17	RN101A 51OHM	VTT	T13	SD_A7	RN104A 51OHM	VTT	T25	SD_A11	RN107A 51OHM	VTT	T37	SD_D31	RN110A 51OHM	VTT
T2	SD_D16	RN101B 51OHM	VTT	T14	SD_A3	RN104B 51OHM	VTT	T26	SD_CKE	RN107B 51OHM	VTT	T38	SD_D30	RN110B 51OHM	VTT
T3	SD_DQS2	RN101C 51OHM	VTT	T15	SD_A10	RN104C 51OHM	VTT	T27	SD_A2	RN107C 51OHM	VTT	T39	SD_DM3	RN110C 51OHM	VTT
T4	SD_DM2	RN101D 51OHM	VTT	T16	SD_CAS	RN104D 51OHM	VTT	T28	SD_A0	RN107D 51OHM	VTT	T40	SD_DQS3	RN110D 51OHM	VTT
T5	SD_D22	RN102A 51OHM	VTT	T17	SD_BA0	RN105A 51OHM	VTT	T29	SD_A4	RN108A 51OHM	VTT	T41	SD_D24	RN111A 51OHM	VTT
T6	SD_D23	RN102B 51OHM	VTT	T18	SD_A6	RN105B 51OHM	VTT	T30	SD_A8	RN108B 51OHM	VTT	T42	SD_D25	RN111B 51OHM	VTT
T7	SD_D20	RN102C 51OHM	VTT	T19	SD_WE	RN105C 51OHM	VTT	T31	SD_A13	RN108C 51OHM	VTT	T43	SD_CLK_N		
T8	SD_D18	RN102D 51OHM	VTT	T20	SD_A9	RN105D 51OHM	VTT	T32	SD_CS1	RN108D 51OHM	VTT	T44	SD_CLK_P		
T9	SD_D21	RN103A 51OHM	VTT	T21	SD_A1	RN106A 51OHM	VTT	T33	SD_D27	RN109A 51OHM	VTT				
T10	SD_D19	RN103B 51OHM	VTT	T22	SD_BA1	RN106B 51OHM	VTT	T34	SD_D29	RN109B 51OHM	VTT				
T11	SD_CS0	RN103C 51OHM	VTT	T23	SD_A5	RN106C 51OHM	VTT	T35	SD_D26	RN109C 51OHM	VTT				
T12	SD_A12	RN103D 51OHM	VTT	T24	SD_RAS	RN106D 51OHM	VTT	T36	SD_D28	RN109D 51OHM	VTT				

DDR2 SDRAMs

U911 / U912 / U913 / U914 — MT47H64M8

VEE, VREF, C5 / C10 / C13 / C19 0.1uF

SDRAM_ODT0 → R555 4.7K, R556 4.7K

SDRAM_ODT1 → R557 4.7K, R558 4.7K

SDRAM_ODTn signals are controlled by the CPLD and are for test purposes only. The MCF5445x does not provide control signals for DDR2 on-die termination. Discrete parallel terminators are used in this design.

Place series termination resistors as close to U1 as possible

U1O — SKT360

SDD31	L21	RN91A 8	1	22OHM SD_D31
SDD30	K22	RN90B 7	2	22OHM SD_D30
SDD29	K21	RN90A 8	1	22OHM SD_D29
SDD28	K20	RN91B 7	2	22OHM SD_D28
SDD27	J20	RN91D 5	4	22OHM SD_D27
SDD26	J19	RN91C 6	3	22OHM SD_D26
SDD25	J21	RN90C 6	3	22OHM SD_D25
SDD24	J22	RN90D 5	4	22OHM SD_D24
SDD23	H20	RN92A 8	1	22OHM SD_D23
SDD22	G22	RN94C 6	3	22OHM SD_D22
SDD21	G21	RN94D 5	4	22OHM SD_D21
SDD20	G20	RN92B 7	2	22OHM SD_D20
SDD19	G19	RN92C 6	3	22OHM SD_D19
SDD18	F22	RN93A 8	1	22OHM SD_D18
SDD17	F21	RN93B 7	2	22OHM SD_D17
SDD16	F20	RN92D 5	4	22OHM SD_D16
SDDM3	H21	RN94B 7	2	22OHM SD_DM3
SDDM2	E21	RN93D 5	4	22OHM SD_DM2
SDDQS3	H22	RN94A 8	1	22OHM SD_DQS3
SDDQS2	E22	RN93C 6	3	22OHM SD_DQS2
SDRASb	N21	RN100C 6	3	22OHM SD_RAS
SDCASb	L19	RN100D 5	4	22OHM SD_CAS
SDWEb	N20	RN100A 8	1	22OHM SD_WE
SDCS0b	M20	RN95C 6	3	22OHM SD_CS0
SDCS1b	L20	RN95D 5	4	22OHM SD_CS1
SDA13	V22	RN96A 8	1	22OHM SD_A13
SDA12	U20	RN97D 5	4	22OHM SD_A12
SDA11	U21	RN96B 7	2	22OHM SD_A11
SDA10	U22	RN96C 6	3	22OHM SD_A10
SDA9	T19	RN97C 6	3	22OHM SD_A9
SDA8	T20	RN99A 8	1	22OHM SD_A8
SDA7	T21	RN96D 5	4	22OHM SD_A7
SDA6	T22	RN98A 8	1	22OHM SD_A6
SDA5	R20	RN99B 7	2	22OHM SD_A5
SDA4	R21	RN98B 7	2	22OHM SD_A4
SDA3	R22	RN98C 6	3	22OHM SD_A3
SDA1	P20	RN99C 6	3	22OHM SD_A1
SDA2	N19	RN95B 7	2	22OHM SD_A2
SDA0	P21	RN98D 5	4	22OHM SD_A0
SDBA0	P19	RN95A 8	1	22OHM SD_BA0
SDBA1	P22	RN99D 5	4	22OHM SD_BA1
SDCKE	N22	RN100B 7	2	22OHM SD_CKE
SDCLK	L22	R148 1	2	22 OHM SD_CLK_P
SDCLKb	M22	R150 1	2	22 OHM SD_CLK_N
SDVREF	M21	VREF RN97B 7	2	22OHM
		RN97A 8	1	22OHM

R687 100 OHM

Place R687 close to the DDR2 devices

VEE: C976 100PF, C981 1000PF, C983 0.1uF, C984 0.1uF, C985 1000PF, C982 1000PF, C977 100PF, C986 100PF, C988 1000PF, C989 0.1uF, C987 100PF, C990 1000PF, C991 0.1uF, C979 10UF

VTT: C980 100PF, C1003 1000PF, C993 0.1uF, C994 0.1uF, C995 1000PF, C992 1000PF, C978 100PF, C996 100PF, C1004 0.1uF, C999 0.1uF, C1005 1000PF, C1000 1000PF, C997 100PF, C998 100PF, C1001 1000PF, C1006 0.1uF, C1007 100PF, C1008 1000PF, C1009 0.1uF, C1002 10UF

DDR2 termination and reference voltage regulator.

J906 HDR_1X2_M

VDD, R922 4.7K

Vsense should be connected to the center of the Vtt termination bus.

U900 LP2997: SD, AVin, Vddq, PVin, GND1, GND2, Vref, Vsense, Vtt

VEE: C922 47UF

VTT: C921 220UF

VREF: C920 0.01UF

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FPGA Platform Flash

U917 — XCF02SVOG20C

Pin	Net
3 CLK	FPGA_CCLK
4 TDI	XPF_TDI
17 TDO	XPF_TDO
5 TMS	XPF_TMS
6 TCK	XPF_TCK
8 OE/RESET	FPGA_INIT_b
13 CEO	XPF_D0
1 D0	XPF_CF_b
7 CF	FPGA_DONE
10 CE	
18 VCCINT, 19 VCCO, 20 VCCJ	VDD
11 GND	
2, 9, 12, 14, 15, 16 NC1–NC6	

FPGA Program Header

H20 — HDR_2X5

XPF_TMS	3	4	XPF_TDI
XPF_TCK	5	6	FPGA_TDO
	9	10	

VDD

FPGA_M2	R673	0 OHM
FPGA_M1	R674	0 OHM
FPGA_M0	R675	0 OHM

RN114 — 4.7K

1	VDD
2	XPF_TDO
3	XPF_TMS
4	XPF_TCK
5	XPF_CF_b
7	FPGA_INIT_b
8	FPGA_DONE
9	FPGA_CCLK
6	
10	

VDD

FPGA_LED0	D958	R444	220 OHM
FPGA_LED1	D957	R445	220 OHM
FPGA_LED2	D956	R446	220 OHM

APT3216MGC

H21 — TSW-104-07-S-D

I2C_SCL	1	2	XPF_TCK
I2C_SDA	3	4	XPF_TMS
ATA_BUFFER_EN	5	6	XPF_TDI
DSPI_PCS2	7	8	FPGA_TDO

These jumpers provide connections from GPIO signals on the MCF5445x to the JTAG interface of the FPGA platform flash.

U919 — XC3S400-4FTG256C

Pin	Net
T16	GND1
T15	CCLK
T14	IO1
T13	IO_L01P_4/VRN_4
T12	IO2
T11	VCCAUX1
T10	IO/VREF_41
T9	IO_L32P_4/GCLK0
T8	IO/VREF_5
T7	IO_L31N_5/D4
T6	VCCAUX2
T5	IO3
T4	IO_L10N_5/VRP_5
T3	IO_L01N_5/RDWR_B
T2	M1
T1	GND2
R16	IO_L01P_3/VRN_3
R15	GND3
R14	DONE
R13	IO_L01N_4/VRP_4
R12	IO_L25P_4
R11	IO_L28P_4
R10	IO_L30P_4/D3
R9	IO_L32N_4/GCLK1
R8	GND4
R7	IO_L31P_5/D5
R6	IO_L29N_5
R5	IO_L27N_5/VREF_5
R4	IO_L10P_5/VRN_5
R3	IO_L01P_5/CS_B
R2	GND5
R1	IO_L01N_6/VRP_6
P16	IO_L01N_3/VRP_3
P15	IO_L16N_3
P14	IO_L16P_3
P13	IO/VREF_42
P12	IO_L25N_4
P11	IO_L28N_4
P10	IO_L30N_4/D2
P9	IO_L31P_4/DOUT/BUSY
P8	IO_L32N_5/GCLK3
P7	IO4
P6	IO_L29P_5/VREF_5
P5	IO_L27P_5
P4	M2
P3	MO
P2	IO_L16N_6
P1	IO_L01P_6/VRN_6
N16	IO_L17N_3
N15	IO_L17P_3/VREF_3
N14	IO_L19P_3
N13	VCCINT7
N12	IO/VREF_43
N11	IO_L27P_4/D1
N10	IO_L29P_4
N9	IO_L31N_4/INIT_B
N8	IO_L32P_5/GCLK2
N7	IO_L30N_5
N6	IO_L28N_5/D6
N5	IO5
N4	VCCINT8
N3	IO_L16P_62
N2	IO_L17N_6
N1	IO_L17P_6/VREF_6
M16	IO_L20N_3
M15	IO_L20P_3
M14	IO_L19N_3
M13	IO_L21P_3
M12	VCCINT1
M11	IO_L27N_4/DIN/D0
M10	IO_L29N_4
M9	VCCO_4
M8	VCCO_5
M7	IO_L30P_5
M6	IO_L28P_5/D7
M4	IO_L19N_6
M3	IO_L19P_6
M2	IO_L20N_6
M1	IO_L20P_6
M5	VCCINT2
L16	VCCAUX3
L15	IO_L22N_3
L14	IO_L22P_3
L13	IO_L21N_3
L12	IO_L23P_3/VREF_3
L11	GND6
L10	VCCO_4
L9	VCCO_4
L8	VCCO_5
L7	VCCO_5
L6	GND7
L5	IO_L21N_6
L4	IO_L21P_6
L3	IO_L22N_6
L2	IO_L22P_6
L1	VCCAUX4
A1	GND8
A2	TDI
A3	IO/VREF_01
A4	IO_L01P_0/VRN_0
A5	IO6
A6	VCCAUX5
A7	IO7
A8	IO_L32P_0/GCLK6
A9	IO8
A10	IO_L31N_1/VREF_1
A11	VCCAUX6
A12	IO9
A13	IO_L10N_1/VREF_1
A14	IO_L01N_1/VRP_1
A15	TDO
A16	GND9
B1	IO_L01P_7/VRN_7
B2	GND10
B3	PROG_B
B4	IO_L01N_0/VRP_0
B5	IO_L25P_0
B6	IO_L28P_0
B7	IO_L30P_0
B8	IO_L32N_0/GCLK7
B9	GND11
B10	IO_L31P_1
B11	IO_L29N_1
B12	IO_L27N_1
B13	IO_L10P_1
B14	IO_L01P_1/VRN_1
B15	GND12
B16	IO_L01N_2/VRP_2
E16	VCCAUX7
E15	IO_L22P_2
E14	IO_L22N_2
E13	IO_L21P_2
E12	IO_L21N_2
E11	GND31
E10	VCCO_1
F9	VCCO_1
F8	VCCO_0
F7	VCCO_0
F6	GND32
F5	IO_L23P_7
F4	IO_L10N_7/VRP_5
F3	IO_L22P_7
F2	IO_L22N_7
F1	VCCAUX8
G16	IO13
G15	IO_L24P_2
G14	IO_L24N_2
G13	IO_L23P_2
G12	IO_L23N_2/VREF_2
G11	VCCO_2
G10	GND27
G9	GND28
G8	GND29
G7	GND30
G6	VCCO_7
G5	IO_L23N_7
G4	IO_L24P_7
G3	IO_L24N_7
G2	IO14
G1	IO_L40P_7
H16	IO_L40P_2/VREF_2
H15	IO_L40N_2
H14	IO_L39P_2
H13	IO_L39N_2
H12	VCCO_2
H11	VCCO_2
H10	GND22
H9	GND23
H8	GND24
H7	GND25
H6	VCCO_7
H5	VCCO_7
H4	IO_L39P_7
H3	IO_L39N_7
H2	GND26
H1	IO_L40N_7/VREF_7
J16	IO_L40N_3/VREF_3
J15	GND17
J14	IO_L39N_3
J13	IO_L39P_3
J12	VCCO_3
J11	VCCO_3
J10	GND18
J9	GND19
J8	GND20
J7	GND21
J6	VCCO_6
J5	VCCO_6
J4	IO_L39N_6
J3	IO_L39P_6
J2	IO_L40N_6
J1	IO_L40P_6/VREF_6
K16	IO_L40P_3
K15	IO11
K14	IO_L24N_3
K13	IO_L24P_3
K12	IO_L23N_3
K11	VCCO_3
K10	GND13
K9	GND14
K8	GND15
K7	GND16
K6	VCCO_6
K5	IO_L23N_6
K4	IO_L23P_6
K3	IO_L24N_6/VREF_6
K2	IO_L24P_6
K1	IO12
E16	IO_L20P_2
E15	IO_L20N_2
E14	IO_L19P_2
E13	IO_L19N_2
E12	VCCINT5
E11	IO_L28P_1
E10	IO_L30P_1
E9	VCCO_1
E8	VCCO_0
E7	IO_L29N_0
E6	IO_L27N_0
E5	VCCINT6
E4	IO_L21P_7
E3	IO_L19N_7/VREF_7
E2	IO_L20P_7
E1	IO_L20N_7
D16	IO_L17P_2/VREF_2
D15	IO_L17N_2
D14	IO_L16P_2
D13	VCCINT3
D12	IO/VREF_1
D11	IO_L28N_1
D10	IO_L30N_1
D9	IO_L32P_1/GCLK4
D8	IO_L31N_0
D7	IO_L29P_0
D6	IO_L27P_0
D5	IO/VREF_02
D4	VCCINT4
D3	IO_L19P_7
D2	IO_L17P_7
D1	IO_L17N_7
C16	IO_L01P_2/VRN_2
C15	IO_L16N_2
C14	TCK
C13	TMS
C12	IO_L27P_1
C11	IO_L29P_1
C10	IO10
C9	IO_L32N_1/GCLK5
C8	IO_L31P_0/VREF_0
C7	IO_L30N_0
C6	IO_L28N_0
C5	IO_L25N_0
C4	HSWAP_EN
C3	IO_L16P_7/VREF_7
C2	IO_L16N_7
C1	IO_L01N_7/VRP_7

FPGA_CCLK			
MEM_ADDR4			
MEM_ADDR8			
MEM_ADDR12			
FPGA_CFG2			
PCI_CLK4			
FPGA_SPARE0			
FPGA_SPARE1			
FB_AD19			
FB_AD11			
FB_AD7			
FPGA_M1			
MEM_DATA29			
FPGA_DONE	R2	56 OHM	MEM_ADDR16
MEM_BE1_b			
FPGA_CFG3			
FPGA_CFG1			
CF_PCI_REQ0			
FB_AD27			
FB_AD23			
FB_AD15			
FB_AD3			
M66EN			
MEM_DATA25			
CLK_GEN_S2			
BRD_RESET			
MEM_DATA18			
MEM_DATA22			
MEM_DATA30			
FPGA_CFG0			
FPGA_CLK			
PCI_IRQ0			
FB_CS3			
FB_AD31			
FPGA_M2			
FPGA_M0			
DREQ0			
MEM_DATA17			
MEM_RW			
MEM_DATA26			
FPGA_INIT_b			
PCI_IRQ1			
FB_TS			
FB_BS3			
LED2_SEG7			
DACK0			
FB_AD30			
MEM_BE0_b			
MEM_DATA21			
FPGA_UDTR			
XPF_D0			
PCI_IRQ2			
PCI_IRQ3			
CF_PCI_GNT0			
LED2_SEG6			
LED2_SEG5			
FB_AD26			
FB_AD10			
MEM_ADDR15			
FPGA_UTXD			
FPGA_UDSR			
FPGA_UCLK			
LED2_SEG4			
LED2_SEG3			
FB_TA			
FB_AD22			
XPF_TDO	R3	56 OHM	FPGA_TDI
FB_AD8			
FB_AD4			
FB_AD0			
PCI_FRAME			
FPGA_LED1			
FPGA_LED2			
MEM_ADDR17			
MEM_ADDR9			
MEM_ADDR1			
FPGA_TDO			
FB_AD1			
XPF_CF_b	R1	56 OHM	FPGA_PROG_b
FB_AD16			
FB_AD12			
FB_AD28			
SLOT_PCI_GNT0			
FB_CLK			
FPGA_LED0			
MEM_DATA27			
MEM_CS_b			
MEM_ADDR13			
MEM_ADDR5			
MEM_ADDR2			
MEM_DATA24			
LED1_SEG2			
LED1_SEG1			
LED1_SEG0			
IRQ4			
MEM_DATA28			
LED1_SEG5			
LED1_SEG4			
LED1_SEG3			
IRQ7			
IRQ3			
MEM_OE_b			
LED1_SEG7			
LED1_SEG6			
IRQ1			
MEM_ADDR3			
FPGA_URTS			
FPGA_UCTS			
LED2_SEG0			
FB_BS2			
FB_AD14			
FB_AD2			
MEM_ADDR7			
MEM_ADDR11			
FPGA_URXD			
FPGA_UDCD			
FPGA_URI			
LED2_SEG2			
LED2_SEG1			
FB_CS2			
FB_AD18			
FB_AD6			
PCI_RESET			
SLOT_PCI_REQ0			
FB_OE			
FB_RWB			
FB_CS1			
FB_AD29			
FB_AD21			
MEM_ADDR14			
MEM_DATA16			
MEM_DATA23			
F_PCI_REQ2			
F_PCI_REQ3			
PCI_IRDY			
F_PCI_GNT3			
FB_CS0			
FB_AD24			
FB_BS1			
FB_AD17			
FB_AD9			
MEM_ADDR6			
MEM_ADDR10			
XPF_TCK	R4	56 OHM	
XPF_TMS	R5	56 OHM	
MEM_DATA19			
MEM_DATA31			
F_PCI_REQ1			
F_PCI_GNT2			
F_PCI_GNT1			
FB_BS0			
FB_AD20			
HSWAP_EN			
FB_AD25			
FB_AD13			
FB_AD5			

SW6, SW7 — TL3301AF160QG

MEM_DATA28	SW6	1	3
		2	4
MEM_DATA24	SW7	1	3
		2	4

These spare test points should be placed in a row. Preferably 0.1 inch spacing.

TP6 FPGA_SPARE0, TP7 FPGA_SPARE1

MRAM

U915 — mr2a16a — 256k x 16 bit 3.3V

Pin	Net
1 A0	MEM_ADDR1
2 A1	MEM_ADDR2
3 A2	MEM_ADDR3
4 A3	MEM_ADDR4
5 A4	MEM_ADDR5
18 A5	MEM_ADDR6
19 A6	MEM_ADDR7
20 A7	MEM_ADDR8
21 A8	MEM_ADDR9
22 A9	MEM_ADDR10
23 A10	MEM_ADDR11
24 A11	MEM_ADDR12
25 A12	MEM_ADDR13
26 A13	MEM_ADDR14
27 A14	MEM_ADDR15
42 A15	MEM_ADDR16
43 A16	MEM_ADDR17
44 A17	MEM_ADDR18
6 E	MEM_CS_b
41 G	MEM_OE_b
17 W	MEM_RW
40 UB	MEM_BE0_b
39 LB	MEM_BE1_b
7 DQL0	MEM_DATA16
8 DQL1	MEM_DATA17
9 DQL2	MEM_DATA18
10 DQL3	MEM_DATA19
13 DQL4	MEM_DATA20
14 DQL5	MEM_DATA21
15 DQL6	MEM_DATA22
16 DQL7	MEM_DATA23
29 DQU8	MEM_DATA24
30 DQU9	MEM_DATA25
31 DQU10	MEM_DATA26
32 DQU11	MEM_DATA27
35 DQU12	MEM_DATA28
36 DQU13	MEM_DATA29
37 DQU14	MEM_DATA30
38 DQU15	MEM_DATA31
28 NC	
11 VDD1, 33 VDD2	VDD
12, 34 VSS1, VSS2	

FPGA RS-232 Interface

U916 — MAX3243CDB

FPGA_UDTR	14 DIN1	9 DOUT1	DB9_UDTR
FPGA_URTS	13 DIN2	10 DOUT2	DB9_URTS
FPGA_UTXD	12 DIN3	11 DOUT3	DB9_UTXD
DB9_URXD	4 R1IN	19 R1OUT	FPGA_URXD
DB9_UDSR	5 R2IN	18 R2OUT	FPGA_UDSR
DB9_UDCD	6 R3IN	17 R3OUT	FPGA_UDCD
DB9_UCTS	7 R4IN	16 R4OUT	FPGA_UCTS
DB9_URI	8 R5IN	15 R5OUT	FPGA_URI
	28 C1+	20 R2OUTB	
	24 C1-	21 INVALID	
	1 C2+		
	2 C2-		
	27 V+		
	3 V-		
	23 FORCEON		
	22 FORCEOFF		
	26 VCC	25 GND	

C883 0.1uF, C880 0.1uF, C881 0.1uF, C884 0.1uF, C882 0.1uF

R809 4.7K, R808 4.7K

U918 — 18.432MHZ

4 VDD	VDD
1 OE	R655 10K
3 OUT	FPGA_UCLK
2 GND	

P3 DB9_M Silkscreen

5	DB9_URI
9	DB9_UDTR
4	DB9_UCTS
8	DB9_UTXD
3	DB9_URTS
7	DB9_URXD
2	DB9_UDSR
6	DB9_UDCD
1	

SW5 — SW_DIP-4_SM

1	8	FPGA_CFG0
2	7	FPGA_CFG1
3	6	FPGA_CFG2
4	5	FPGA_CFG3

RP97 — 4.7K

1	VDD
2	
3	
4	
5	
7	
8	
9	
10	
6	

U28 — 30mA — 7-segment Display

LED1_SEG0	RP93A	1	8
LED1_SEG1	RP93B	2	7
LED1_SEG2	RP93C	3	6
LED1_SEG3	RP93D	4	5
	470OHM		
LED1_SEG4	RP94A	1	8
LED1_SEG5	RP94B	2	7
LED1_SEG6	RP94C	3	6
LED1_SEG7	RP94D	4	5
	470OHM		

14	COM1_D1	COM_2	13
16	A1	A2	11
15	B1	B2	10
3	C1	C2	8
2	D1	D2	6
1	E1	E2	5
18	F1	F2	12
17	G1	G2	7
4	DP1	DP2	9

LED2_SEG0	RP95A	1	8
LED2_SEG1	RP95B	2	7
LED2_SEG2	RP95C	3	6
LED2_SEG3	RP95D	4	5
	470OHM		
LED2_SEG4	RP96A	1	8
LED2_SEG5	RP96B	2	7
LED2_SEG6	RP96C	3	6
LED2_SEG7	RP96D	4	5
	470OHM		

JP906 HDR_1X2_M, TP2, R810 4.7K

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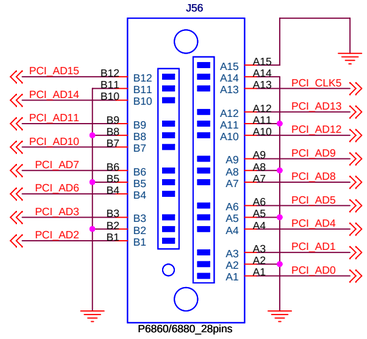
Probe 1



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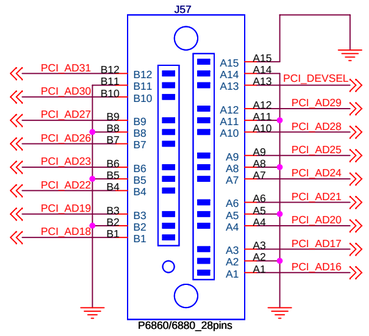
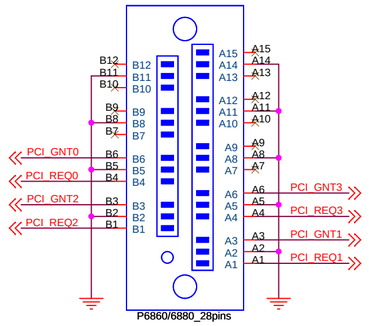


Probe 3



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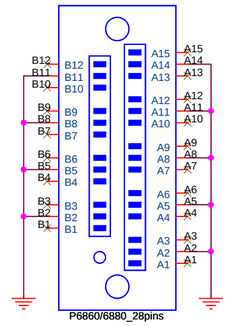
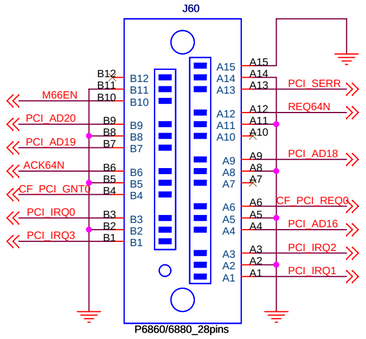


Probe 5



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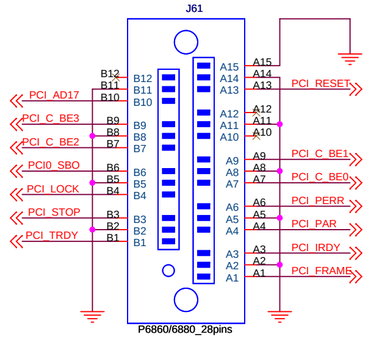

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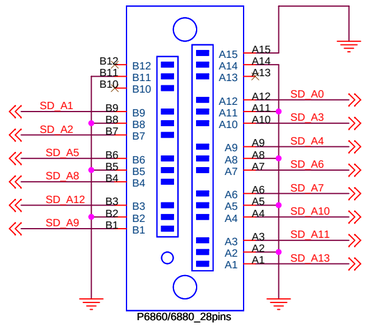

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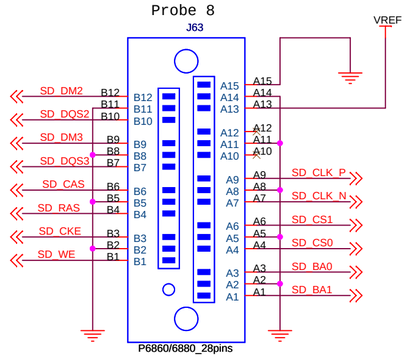

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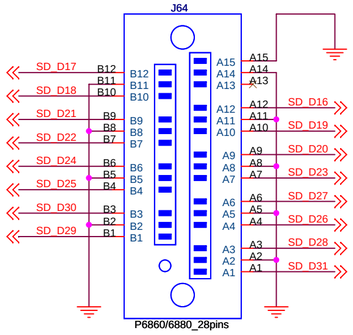

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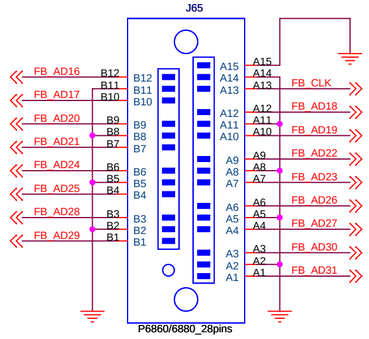

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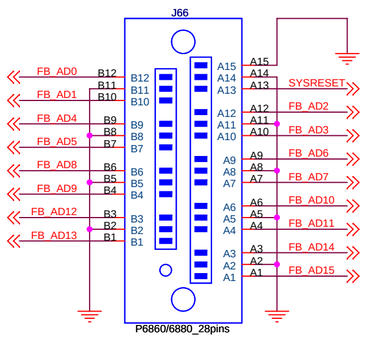

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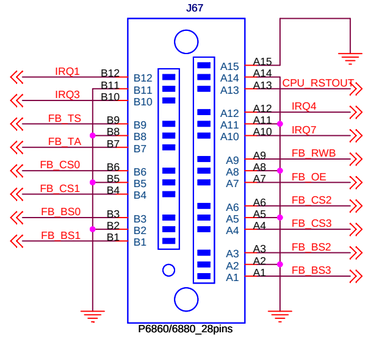

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Page Title: **PROBES**

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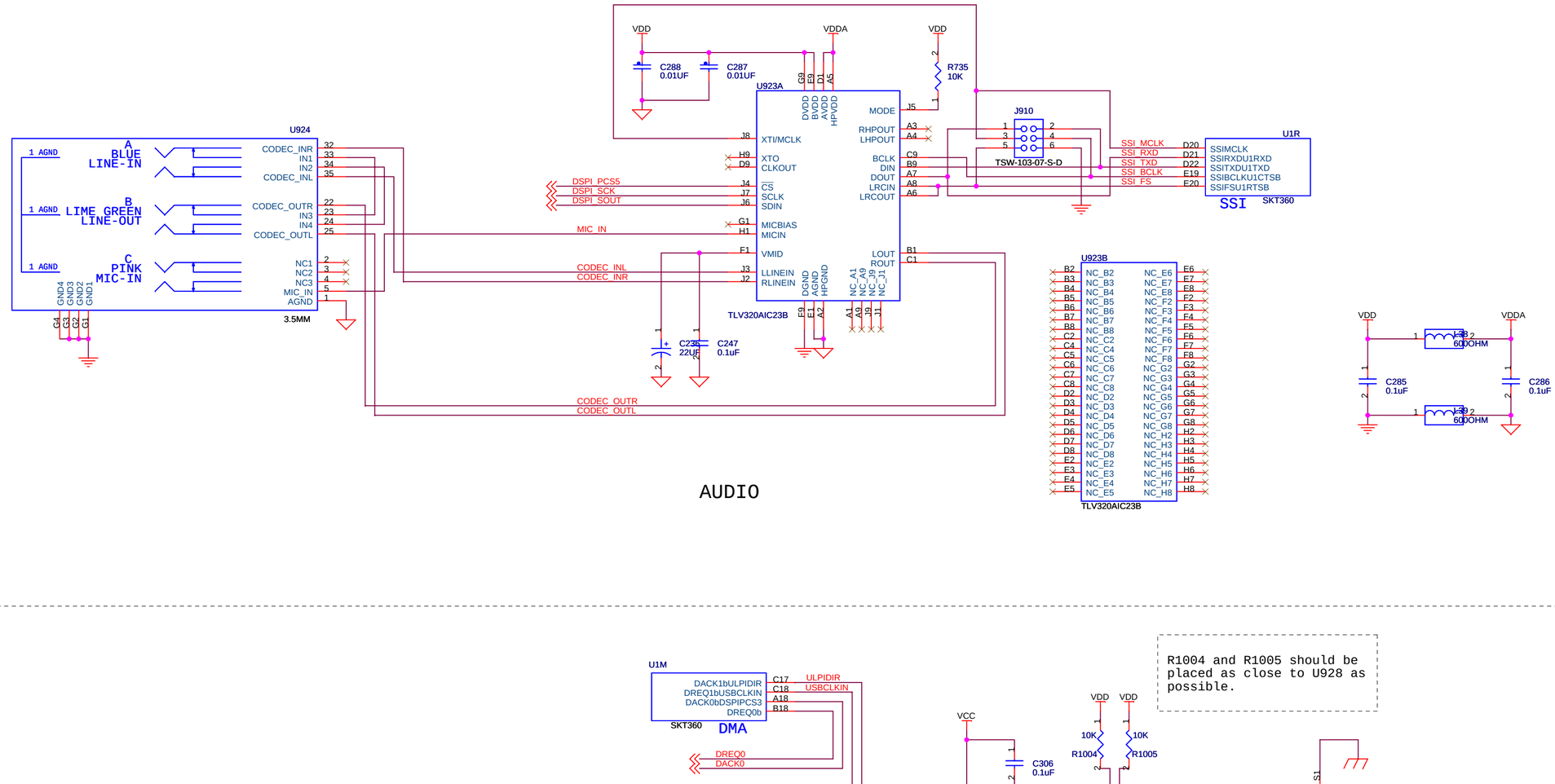
U924
A
BLUE
LINE-IN
B
LIME GREEN
LINE-OUT
C
PINK
MIC-IN
1 AGND
CODEC_INR
IN1
IN2
CODEC_INL
CODEC_OUTR
IN3
IN4
CODEC_OUTL
NC1
NC2
NC3
MIC_IN
AGND
GND4
GND3
GND2
GND1
3.5MM
U923A
TLV320AIC23B
VDD
VDDA
C288
0.01UF
C287
0.01UF
R735
10K
MODE
RHPOUT
LHPOUT
XTI/MCLK
XTO
CLKOUT
BCLK
DIN
DOUT
LRCIN
LRCOUT
CS
SCLK
SDIN
MICBIAS
MICIN
VMID
LLINEIN
RLINEIN
LOUT
ROUT
DVDD
BVDD
AVDD
HPVDD
DGND
AGND
HPGND
NC_A1
NC_A9
NC_J9
NC_J1
DSPI_PCS5
DSPI_SCK
DSPI_SOUT
MIC_IN
CODEC_INL
CODEC_INR
CODEC_OUTR
CODEC_OUTL
C235
22UF
C247
0.1uF
J910
TSW-103-07-S-D
SSI_MCLK
SSI_RXD
SSI_TXD
SSI_BCLK
SSI_FS
U1R
SSIMCLK
SSIRXDU1RXD
SSITXDU1TXD
SSIBCLKU1CTSB
SSIFSU1RTSB
SSI
SKT360
U923B
TLV320AIC23B
C285
0.1uF
C286
0.1uF
FB8
600OHM
FB9
600OHM
AUDIO
U1M
DACK1bULPIDIR
DREQ1bUSBCLKIN
DACK0bDSPIPCS3
DREQ0b
ULPIDIR
USBCLKIN
DREQ0
DACK0
DMA
SKT360
R1004 and R1005 should be placed as close to U928 as possible.
VCC
C306
0.1uF
R1004
10K
R1005
10K
S1
J909
USB_MINI_AB_SKT
USB-AB_N
USB-AB_P
OTG/dual-role USB via ULPI interface
PLACE CAPACITORS CLOSE TO VDD3.3 PINS ON USB3300
C300
4.7UF
C304
0.01UF
C301
0.01UF
C302
0.01UF
C303
0.01UF
U927
3V3VDD1
3V3VDD2
3V3VDD3
3V3VDD4
3V3VDD5
1V8VDD1
1V8VDD2
1V8VDDA
GND1
GND2
GND3
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
DP
DM
VBUS
CPEN
EXTVBUS
RBIAS
ID
STP
DIR
CLKOUT
NXT
XO
XI
RESET
USB3300
U928
ENA
ENB
IN
GND
FLGA
FLGB
OUTA
OUTB
MIC2026-1YM
R151
0 OHM
C305
1.0UF
JP918
HDR_1X3
R738
12K
ULPI_RESET
USBCLK_24
USBCLK_60
U1P
USBVBUSENUSBPULLUPULPINXT
USBVBUS-OCULPISTP
USBDEVDMNS
USBDEVDPLS
FEC0TXERULPIDATA0
FEC0RXCLKULPIDATA1
FEC0TXD2ULPIDATA2
FEC0TXD3ULPIDATA3
FEC0RXD2ULPIDATA4
FEC0RXD3ULPIDATA5
FEC0CRSULPIDATA6
FEC0COLULPIDATA7
USB_VBUS_EN
USB_VBUS_OC
USB_DEV_DMNS
USB_DEV_DPLS
ULPI_DATA0
ULPI_DATA1
ULPI_DATA2
ULPI_DATA3
ULPI_DATA4
ULPI_DATA5
ULPI_DATA6
ULPI_DATA7
SKT360
USB
R9082
15K
R9081
15K
R736
33ohm
R737
33ohm
USB-A_N
USB-A_P
P4
USB_TYPE_A
R739
0 OHM
C307
47UF
FS/LS Host via MCF5445x on-chip transceiver
C289
4.7UF
C291
0.1uF
C290
4.7UF
C292
0.1uF
USB
Layout Notes:
* The required 33 ohm series source termination resistors should be placed as closely to the USB_DEV_DMNS and USB_DEV_DPLS outputs as possible.
* Route D- and D+ signals on the top or bottom layer of the board keeping them as short as possible with a minimum amount of vias and corners.
* Use 45deg turns instead of 90deg turns.
* The trace width and spacing of the D- and D+ signals should be such that the differential impedance is 90 Ohms.
* Maintain the parallelism (skew matching) between D- and D+. These traces should be the same overall length.
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P&E Microcomputer Systems
USB ColdFire Multilink BDM Interface

CF_RESET — BDM_RESET

CF_TEA — FB_TA

CF_DSO — DSO

CF_FREEZE — TCLK_PSTCLK

CF_DSCLK — DSCLK

CF_BKPT — BKPT

PST0 — PSTDDATA0

PST1 — PSTDDATA1

PST2 — PSTDDATA2

PST3 — PSTDDATA3

CF_DSI — DSI

EXTERNAL_DSI — EXTERNAL_DSI

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Drawing Title:
P&E CONFIDENTIAL INFORMATION

Page Title:
USB TO BDM COLDFIRE REFERENCE DESIGN

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