Vybrid Automotive Customer Evaluation Board

Table of Contents:

Notes:
- All components and board processes are to be ROHS compliant.
- All small capacitors are 0402 unless otherwise stated.
- All zero ohm links are 0603.
- All connectors and headers are denoted Px and are 2.54mm pitch, unless otherwise stated.
- All jumpers are denoted Jx. Vast majority of them are 2-mm pitch.
- Jumper default positions are shown. 2-way jumpers have "source" as pin 1.
- All Switches denoted SWx.
- All Test Points denoted TPx.
- All Test Point Vias denoted TPVx.

- User notes given throughtout schematic.
- *Specific PCB LAYOUT notes detailed in ITALICS.*
- Jumper settings given throughtout schematic.
- Modifications from previous major board revision given throughtout schematic.

Revision Information

Rev	Date	Designer	Comments
A	7 April 2013	G. Ron	Closer to reference design: DDR, power, no socket. Design leverage from Rev.D 27419. Power design leverage from Rev.H 27442 (Vybrid Tower board). Bluetooth connector like on i.MX6 boards.
B	24 April 2013	G. Ron	SCH change: - New 24 MHz crystal. Fab change. - L1 TOP: remove GND plane in between USB and USB1 diff pairs. - Correct Fab note 22 to match netname changes on board. - Change Fab note 6 to 0.0035"/0.0035". - Change Fab note 7 to (2-8 microinches).
B1	8 Oct. 2014	D.K.	Release to production. Update Marketing Part Number to EVB-VF522R3.
B2	20 Nov. 2014	N.G.	Default jumper settings updated on schematic.

Note: These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale Vybrid family of microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with Vybrid processors.
Although best design practices have been applied, some areas may not be suitable for a mass-production design.
System evaluation was not performed over process fluctuations, voltage changes, and temperature variations.

For an added resource, refer to Vybrid Hardware Development Guide document.

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Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Designer: N.G.	Drawing Title: **EVB-VF522R3**	
Drawn by: N.G.	Page Title: **Title and Revision History**	
Approved: Ross M.	Size B	Document Number SCH-28141 PDF: SPF-28141 — Rev B2
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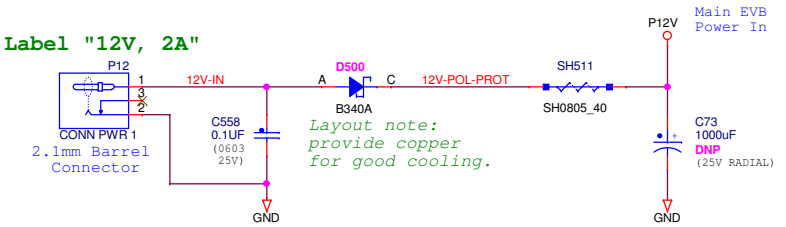
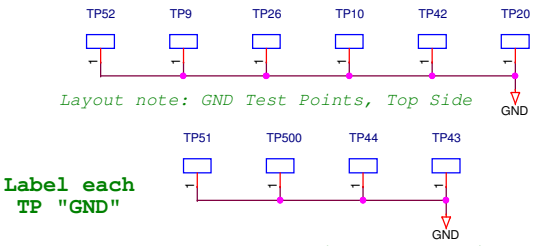
ut and Linear Voltage Regulators (1.2V / 1.8V / 3.3V)

Power Supply Input, Polarity Protection, and Filter

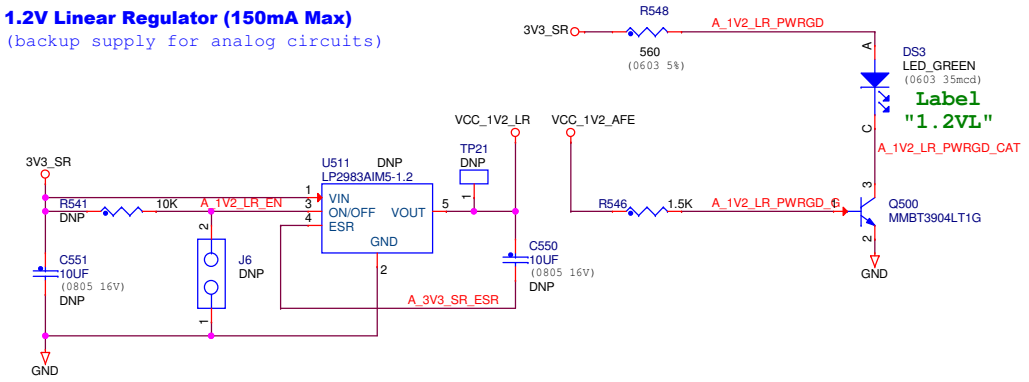


Test and reference points



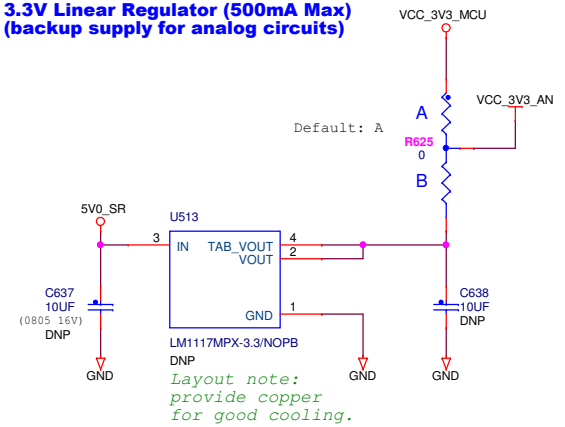
1.2V Linear Regulator (150mA Max)

(backup supply for analog circuits)



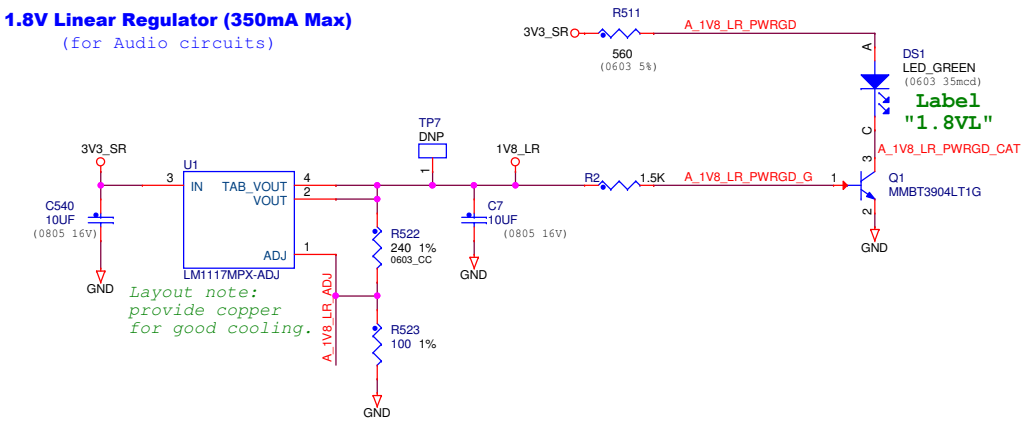
3.3V Linear Regulator (500mA Max)

(backup supply for analog circuits)



1.8V Linear Regulator (350mA Max)

(for Audio circuits)



Note: Modifications from Rev.D 27419:
- 12V input circuitry simplified.
- D500 (wrong-polarity protection) connection changed.
- optional 1.2V Linear Regulator circuitry added and DNP-ed.
- LED indication for VCC_1V2_AFE rail added.
- LED indication transistors from FET to bipolar.

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **Main input and Linear voltage regulators (1.2V / 1.8V / 3.3V)**

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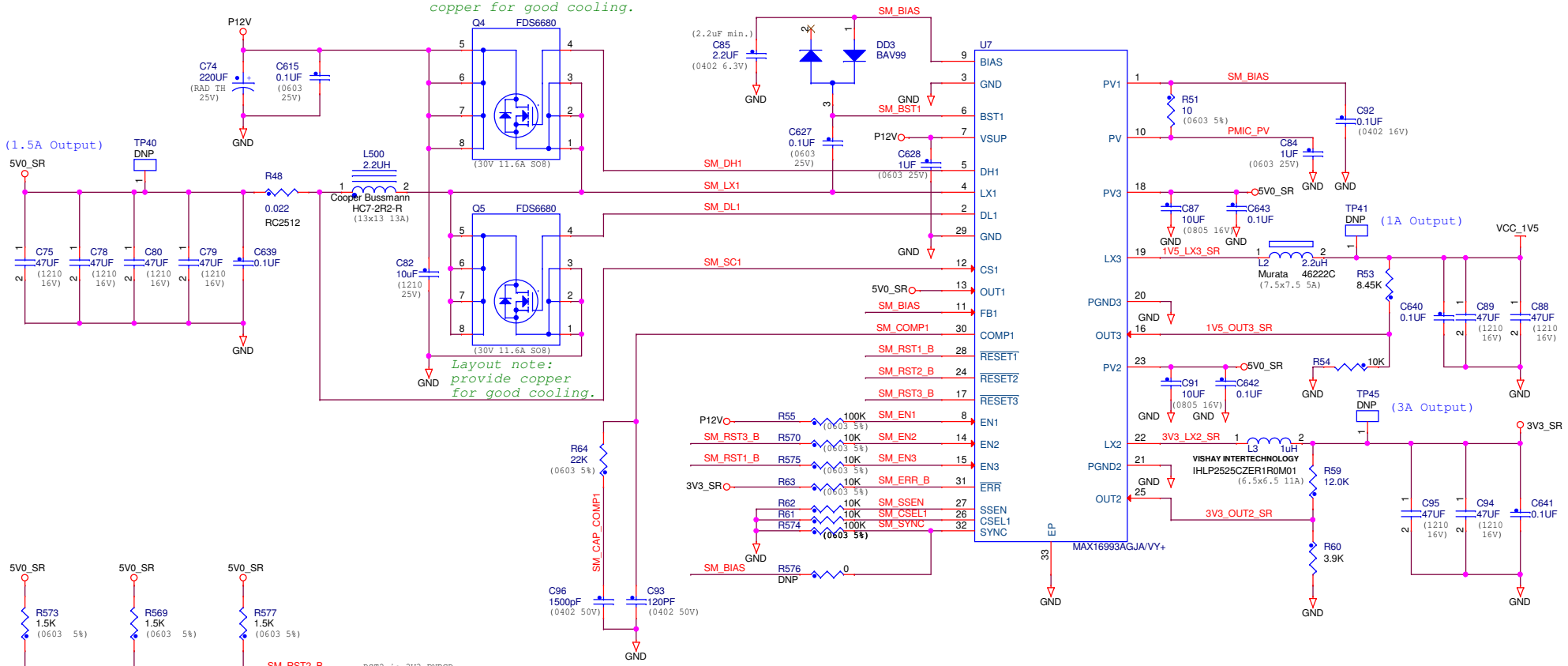
-Mode Voltage Regulator (5V, 3.3V, 1.5V)

Part must be 'Option E' per
Selector output voltage guide.



Note: Modifications from Rev.D 27419:
- full re-design (multi-output regulator instead of multiple single-output ones).

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ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	EVB-VF522R3		
Page Title:	Switch-Mode Voltage Regulator		
Size B	Document Number SCH-28141 PDF: SPF-28141		Rev B2
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J Power Connections

Layout note:
Place 0.22uF close to each SDRAMC pin,
better on opposite PCB side under the 364BGA.

Layout note:
Place 0.22uF close to each VDD pin, better to place one
by one at the opposite PCB side under the 364BGA.

Diode DD2 guarantees 3.3V power
is uninterrupted when J9 open

Layout note:
Place 0.1uF close to each VDD33 pin, better to place one
by one at the opposite PCB side under the 364BGA.

Compatible with
user-supplied
2016/2025/2032
coin cells.

Diodes are not
automotive. Use
any regular diode
with min. 0.5A and
fitting footprint.
For application without 1.5V rail,
i.e. without DDR. install diodes
and move 0-Ohm resisitor from
posistion A to B.

Best performance when x_AFE
rails powered from dedicated
linear voltage regulators.

Best performance when x_ADC
rails powered from dedicated
linear voltage regulators.

Most critical for VREFH_ADC;
without power filtering, actual ADC
resolution might be degraded.

Resistor "Storage" for Power Rail Current Measurements
(if required, cut "Shorts" of interest and install resistors to measure power rails' currents)

R38 0.02 (1% 0805) TPV15 TPV16
R20 0.02 (1% 0805) TPV2 TPV4
R33 0.02 (1% 0805) TPV13 TPV10
R52 0.02 (1% 0805) TPV28 TPV27
R34 0.02 (1% 0805) TPV11 TPV14
R46 0.02 (1% 0805) TPV22 TPV21
R49 0.02 (1% 0805) TPV24 TPV23
R50 0.02 (1% 0805) TPV26 TPV25

Note: Modifications from Rev.D 27419:
- power management scheme copied from Tower module.

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ICAP Classification:	FCP: ___ FIUO: X PUBI: ___
Drawing Title:	EVB-VF522R3
Page Title:	MCU Power Connections
Size: C	Document Number: SCH-28141 PDF: SPF-28141 Rev: B2
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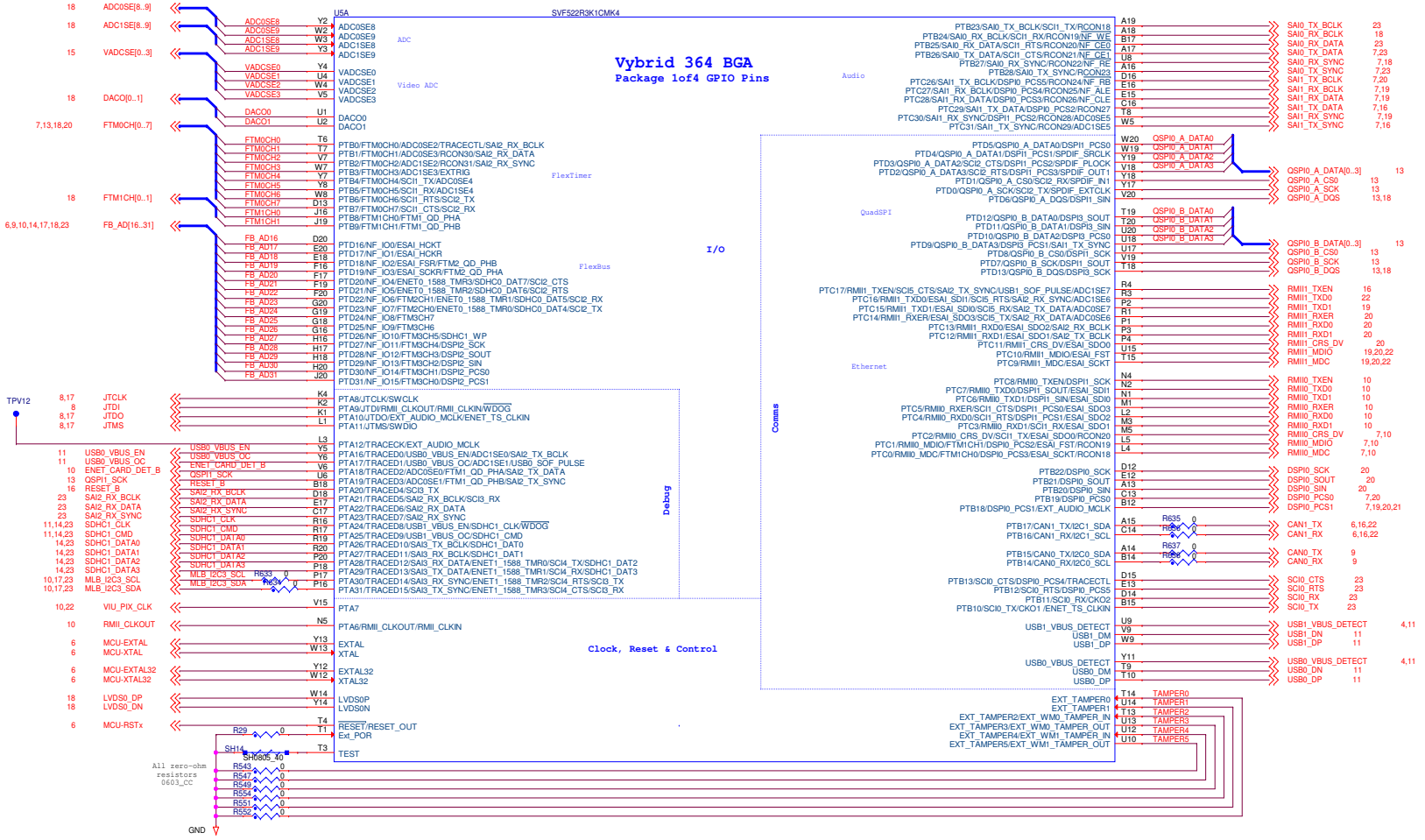
GPIO & Peripheral Connections



ICAP Classification:	FCP: ___ FIUO: X PUBI: ___
Drawing Title:	EVB-VF522R3
Page Title:	MCU GPIO & Peripheral Connections
Size: C	Document Number: SCH-28141 PDF: SPF-28141 Rev: B2
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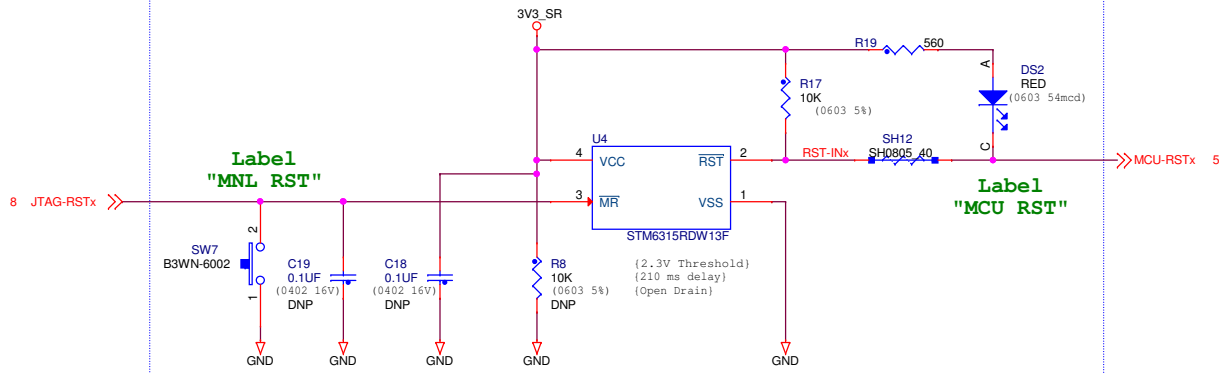
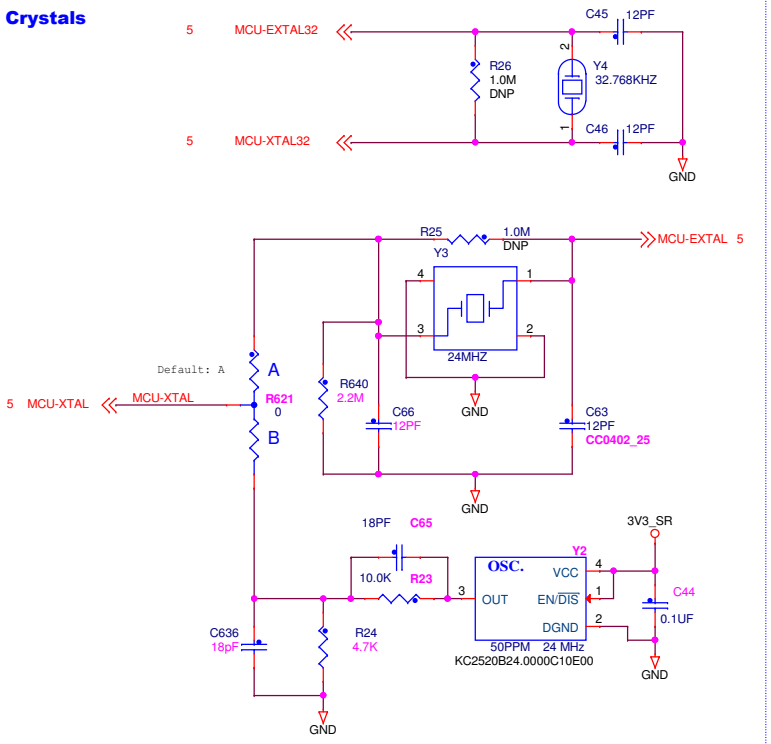
incl. I2C Reset Mux) and Clocks

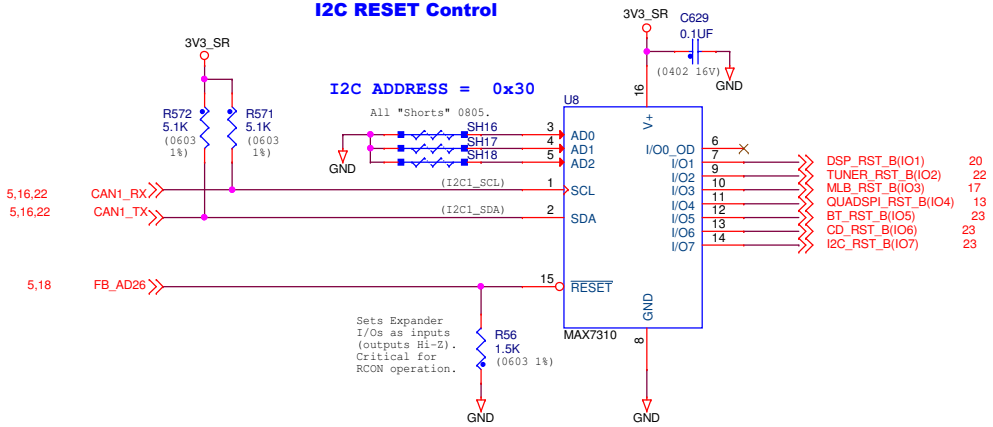
MCU Reset



Crystals



I2C RESET Control



(1.5K pull-Down on DSP sheet)
(1.5K pull-down on tuner sheet)
(1.5K pull-down on MLB sheet)
(1.5K pull-downon QUADSPI sheet)
(1.5K pull-down on board)
(1.5K pull-down on sheet with CD Connector)
(1.5K pull-down I2C_RST(IO0))

Note: Modifications from Rev.D 27419:
- reset circuit copied from i.MX6 design + simplified,
- R640 (2.2M resistor) added as per Erratum e5880.
- I2C RESET Control IO0 disconnected.
- I2C RESET Control IO7 re-assigned to 3.3V I2C Daughtercard.

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **Reset - (incl I2C reset Mux) and Clocks**

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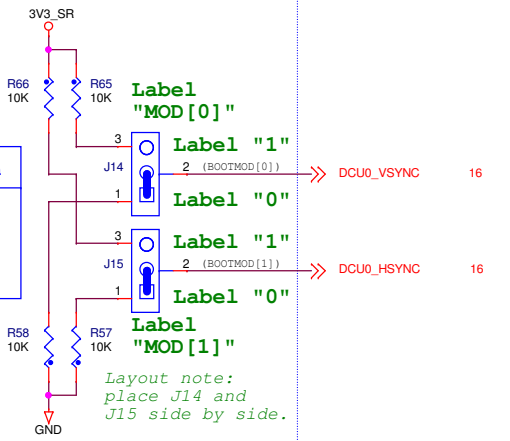
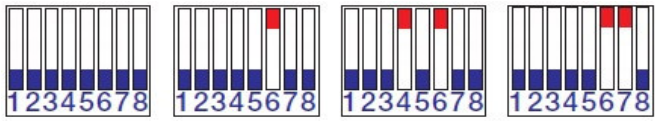
de / RCON Configuration

Boot Mode Selection

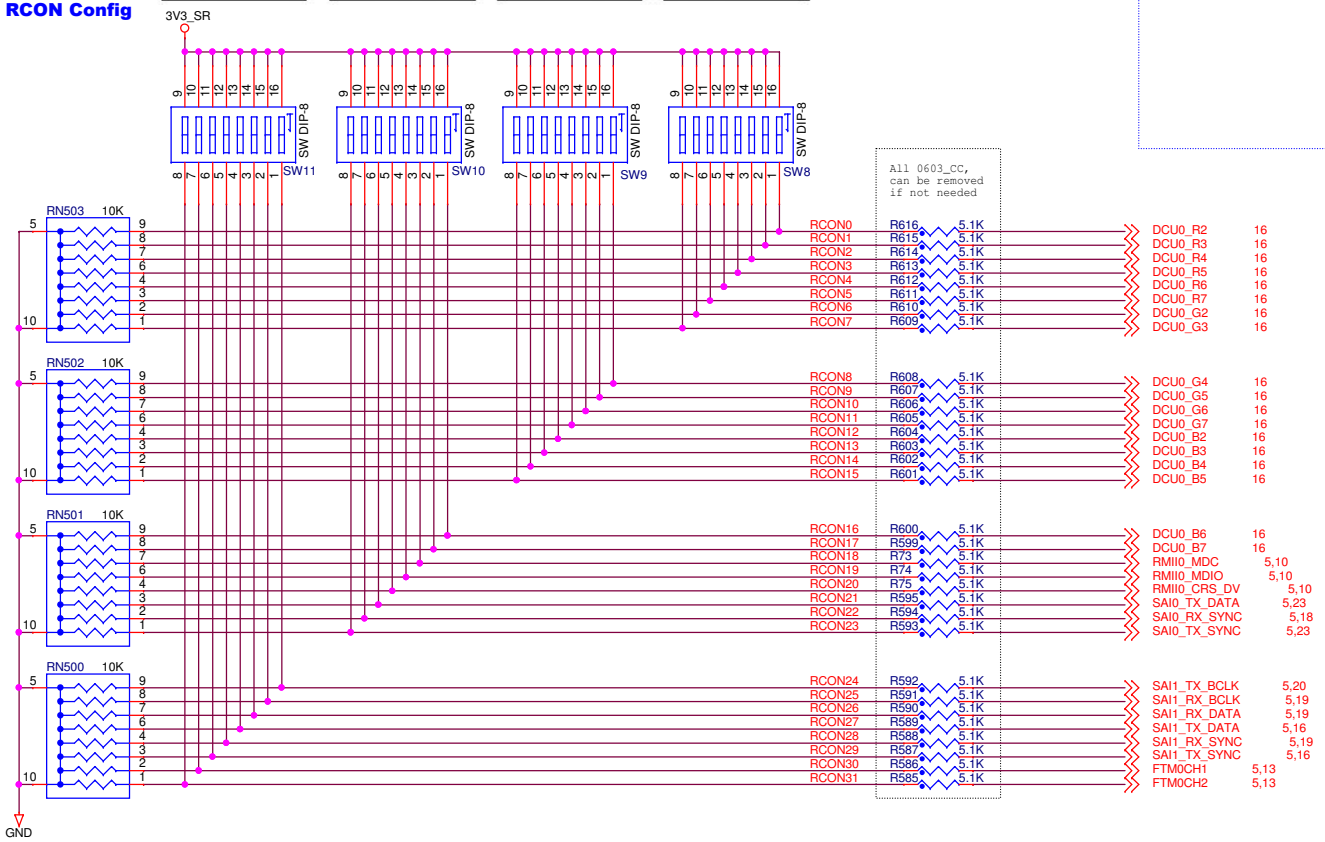
BOOTMOD[1:0]	Boot Description
00	Boot from Fuses
01	Serial Download
10 (Default)	From RCON Sw.
11	Reserved



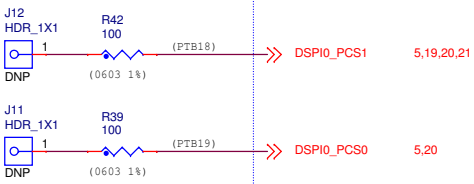
Default



RCON Config



Factory use only



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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **Boot mode / RCON configuration**

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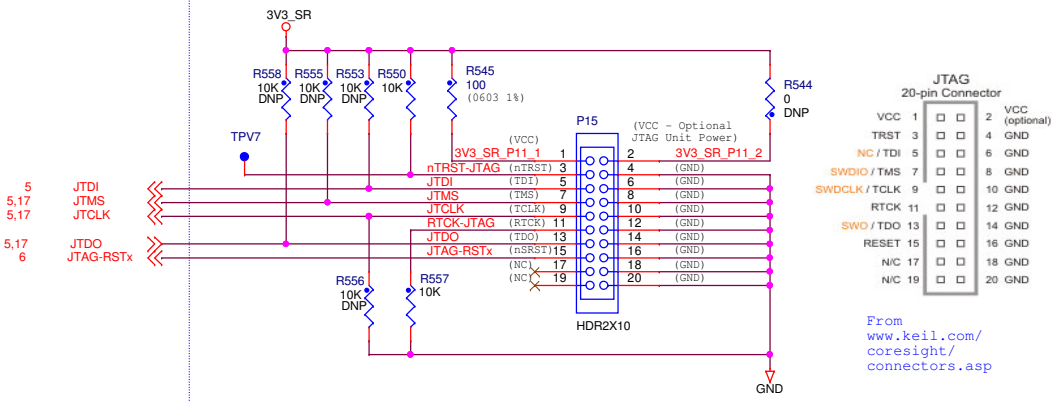
i Cortex Connectors

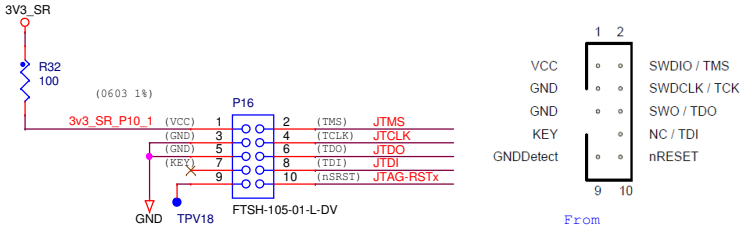
ARM Standard (legacy) JTAG (20-pin)



From www.keil.com/coresight/connectors.asp

ARM Cortex (10-pin)

Layout note: pin 7 of P16 must be physically removed - used as polarization key.



From www.keil.com/coresight/connectors.asp

Pin 9 (GNDDetect) may be optionally used by target system to detect debugger is present.

Note: Modifications from Rev.D 27419:
- ARM ETM connector removed.

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **JTAG and Cortex Connectors**

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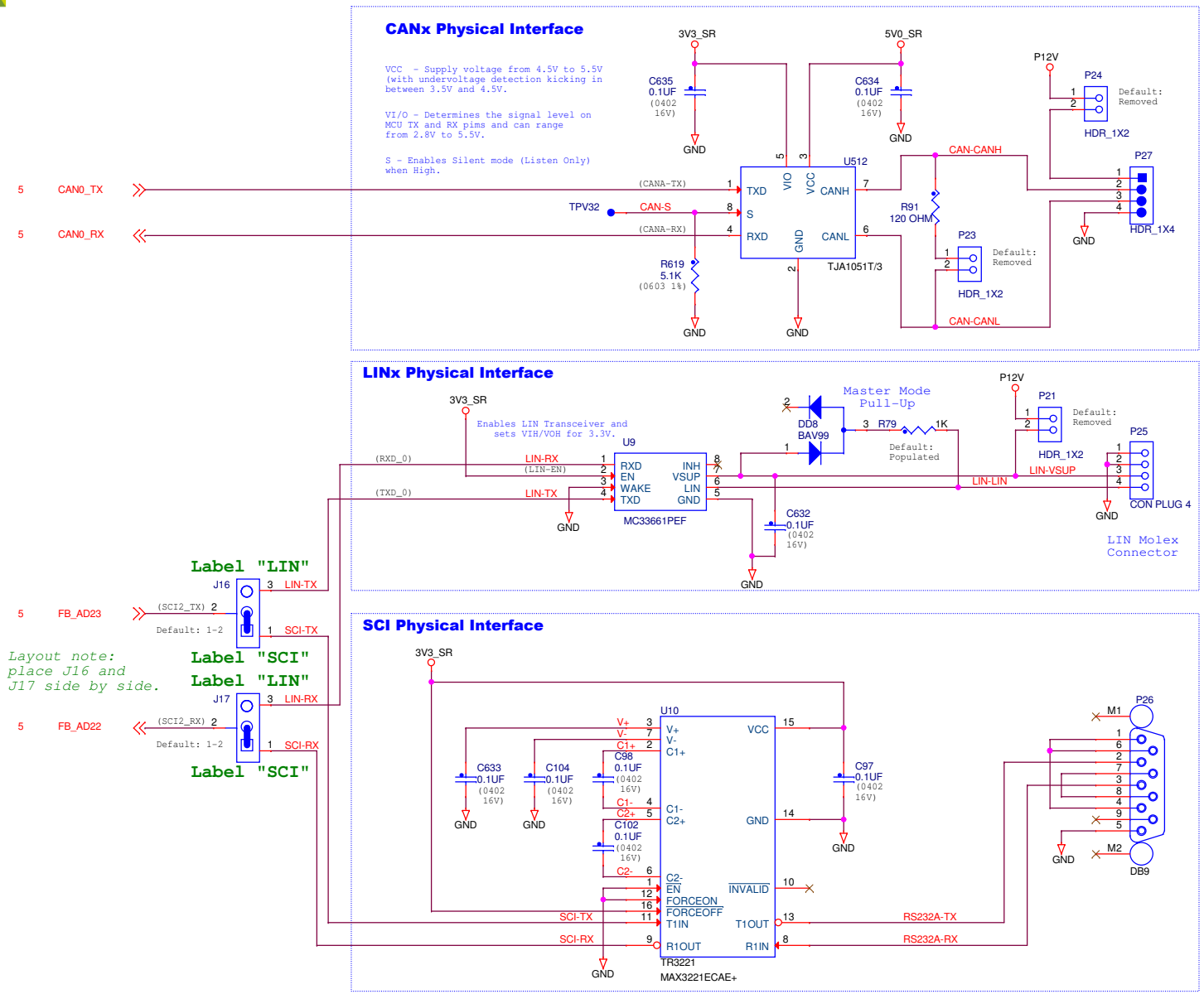
N, and SCI Interfaces



Note: Modifications from Rev.D 27419:
- SCI_0 is now used for Bluetooth and SCI_2 for RS-232.

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ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **CAN, LIN, and SCI Interfaces**

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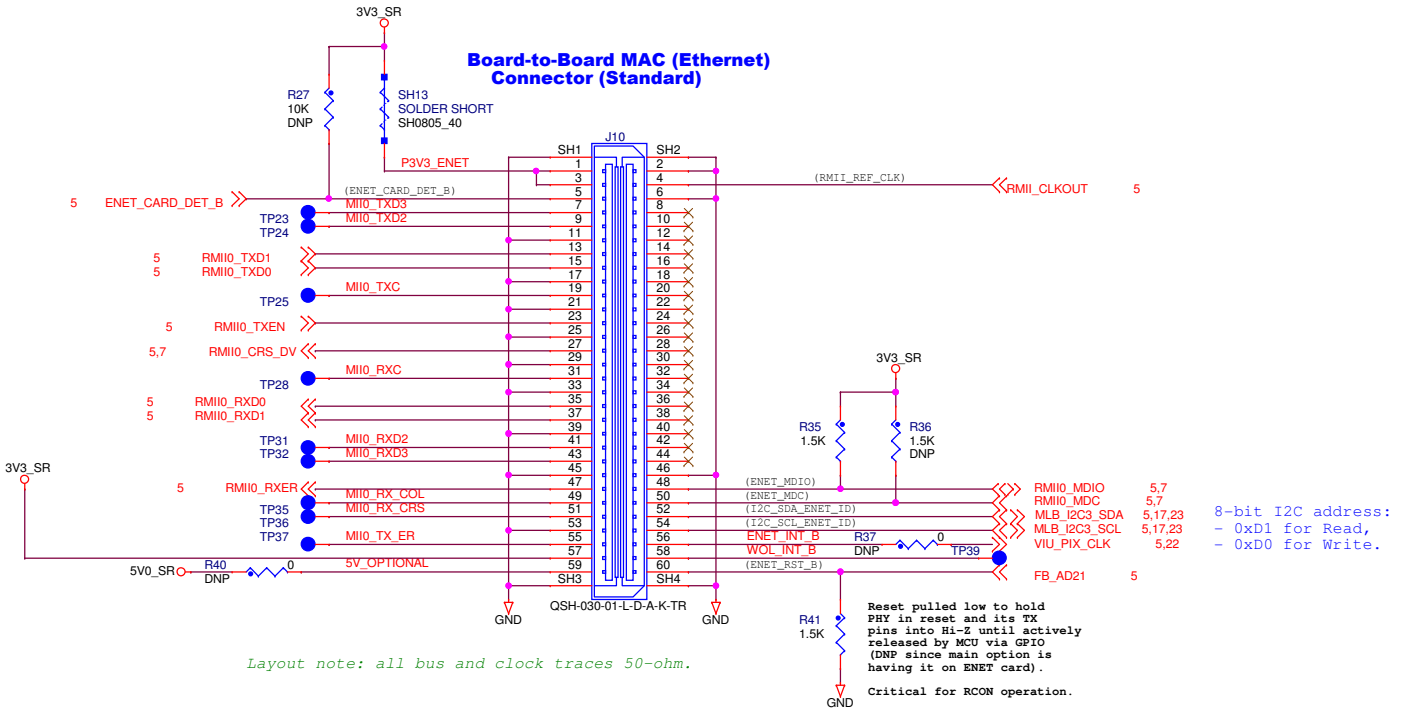
thernet) Connections



Layout note: all bus and clock traces 50-ohm.

Note: Modifications from Rev.D 27419:
- On-board PHY replaced with standard ENET board-to-board connector,
- PHY reset changed from SCI0_RTS (now used by Bluetooth) to FB_AD[21] (SCI2_RTS),
- Vybrid's TRACED2 pin now used as IO for ENET_CARD_DET_B (after ARM ETM connector got removed).

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ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	EVB-VF522R3		
Page Title:	MAC (Ethernet) Connections		
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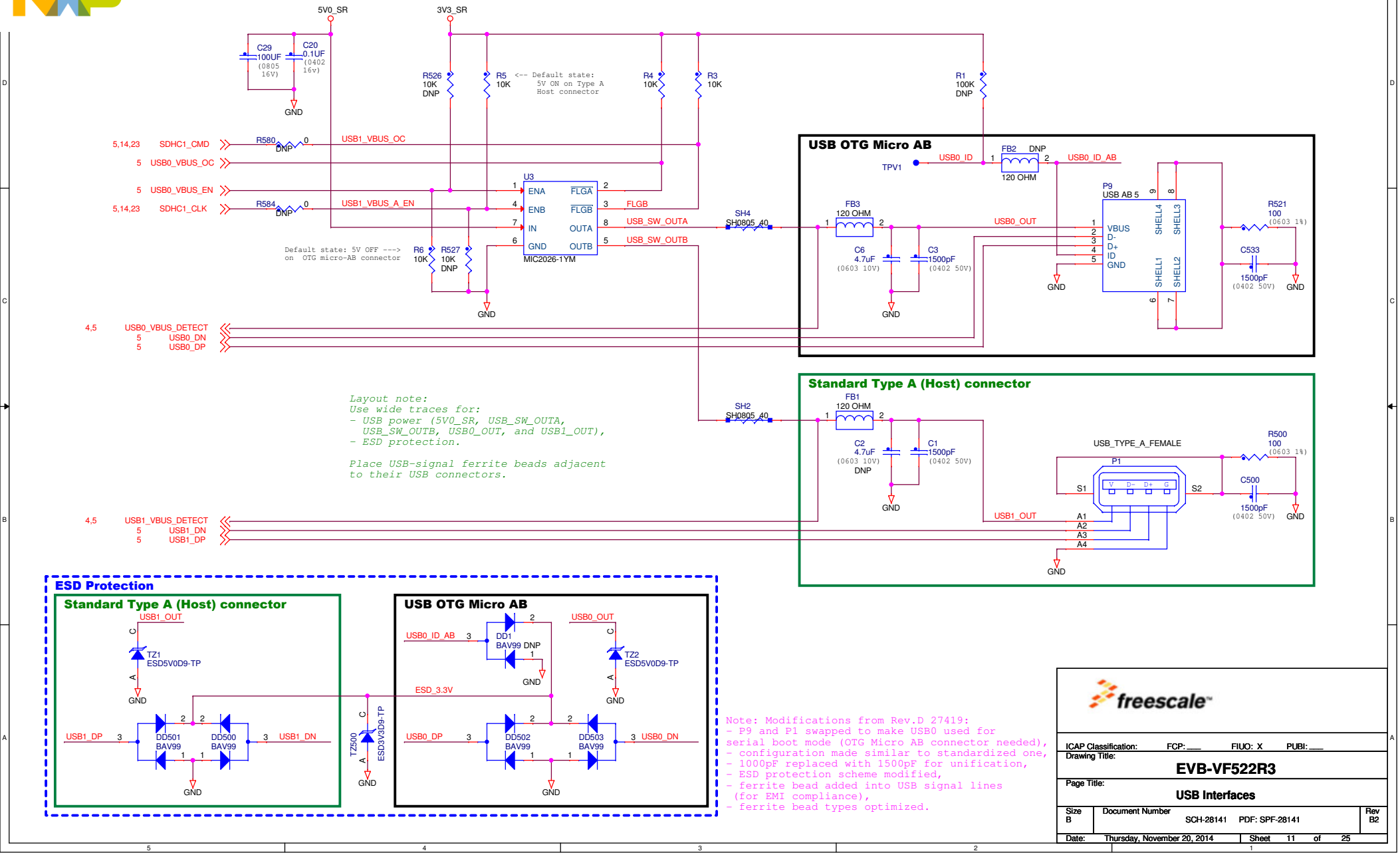

Note: Modifications from Rev.D 27419:
- P9 and P1 swapped to make USB0 used for serial boot mode (OTG Micro AB connector needed),
- configuration made similar to standardized one,
- 1000pF replaced with 1500pF for unification,
- ESD protection scheme modified,
- ferrite bead added into USB signal lines (for EMI compliance),
- ferrite bead types optimized.

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **USB Interfaces**

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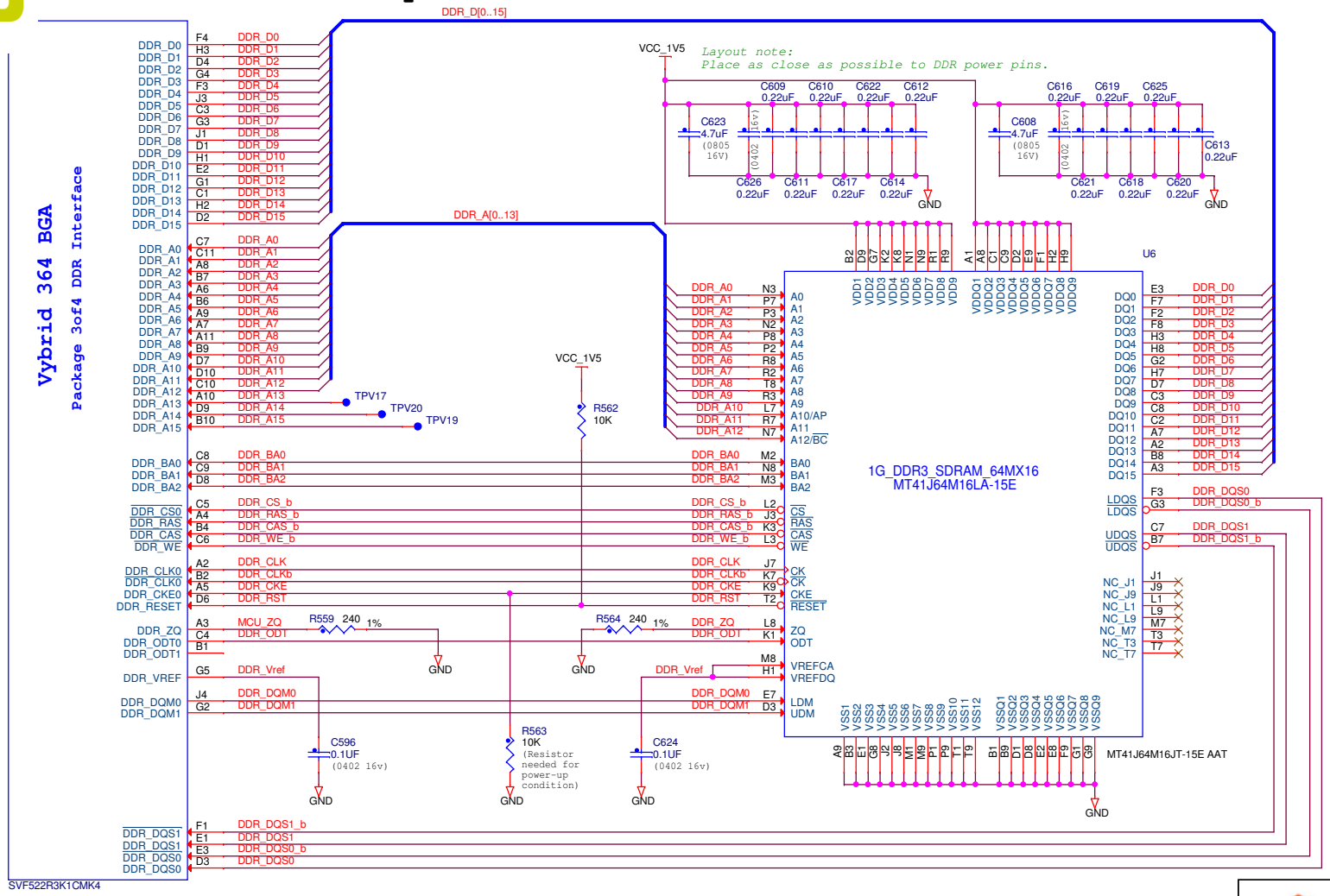
Connections and Memory



Note: Modifications from Rev.D 27419:
- In 0.75V Reference circuit 240 1% instead of 470 5% (precision improvement and BOM consolidation),
- pull-up added on DDR_RST line to support DDR3 Self-Refresh when Vybrid in LPSTOP modes.

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ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	EVB-VF522R3		
Page Title:	DDR3 MCU Connections and Memory		
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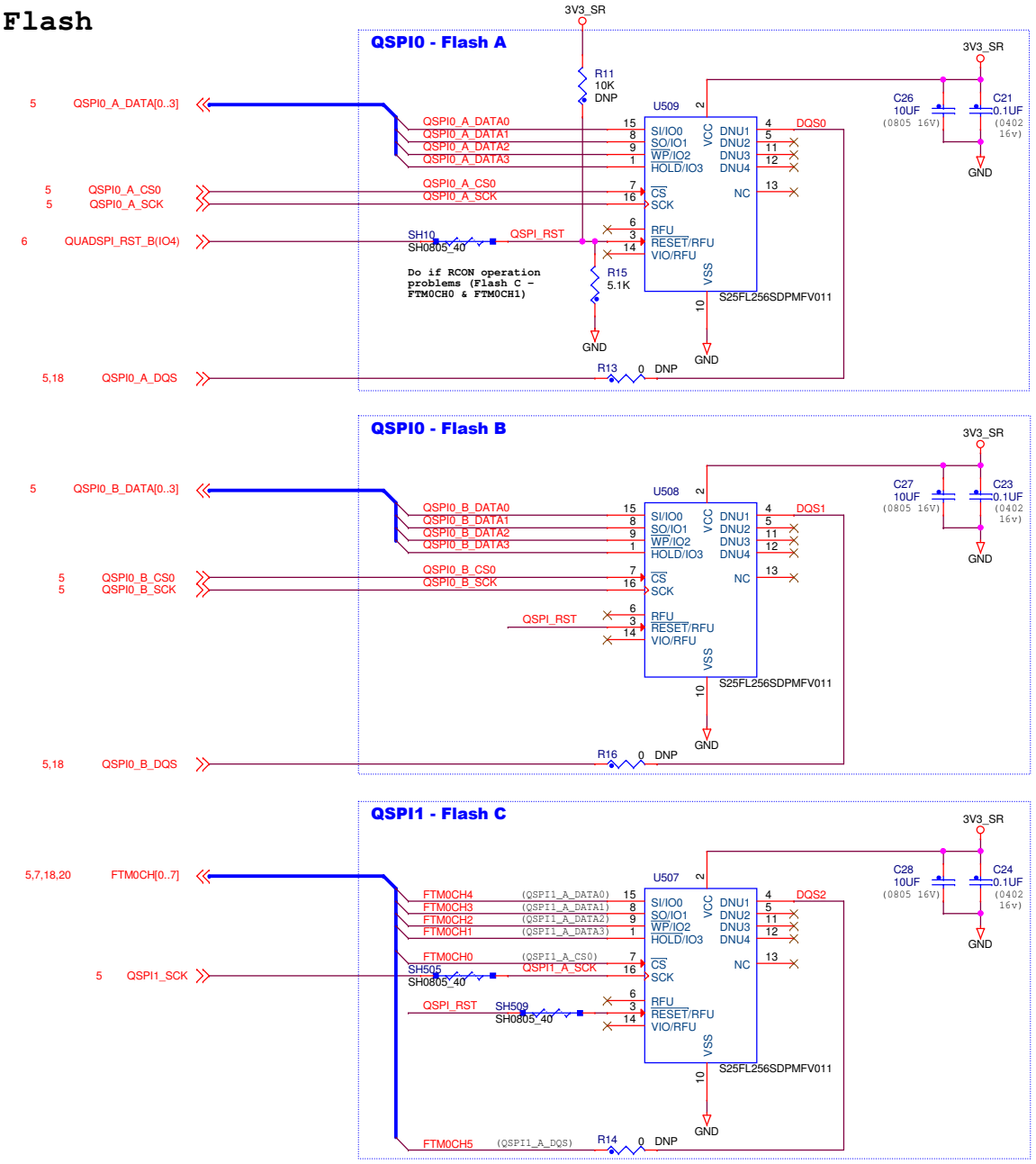
Flash



Flash size 32MB, Sector size 64KB.

DQSx signal not used on SPANSION Flash, so may be used for GPIO in this instance.

Flash devices have internal pull-up on CS line, so no need for external pull resistors.

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **QuadSPI Flash**

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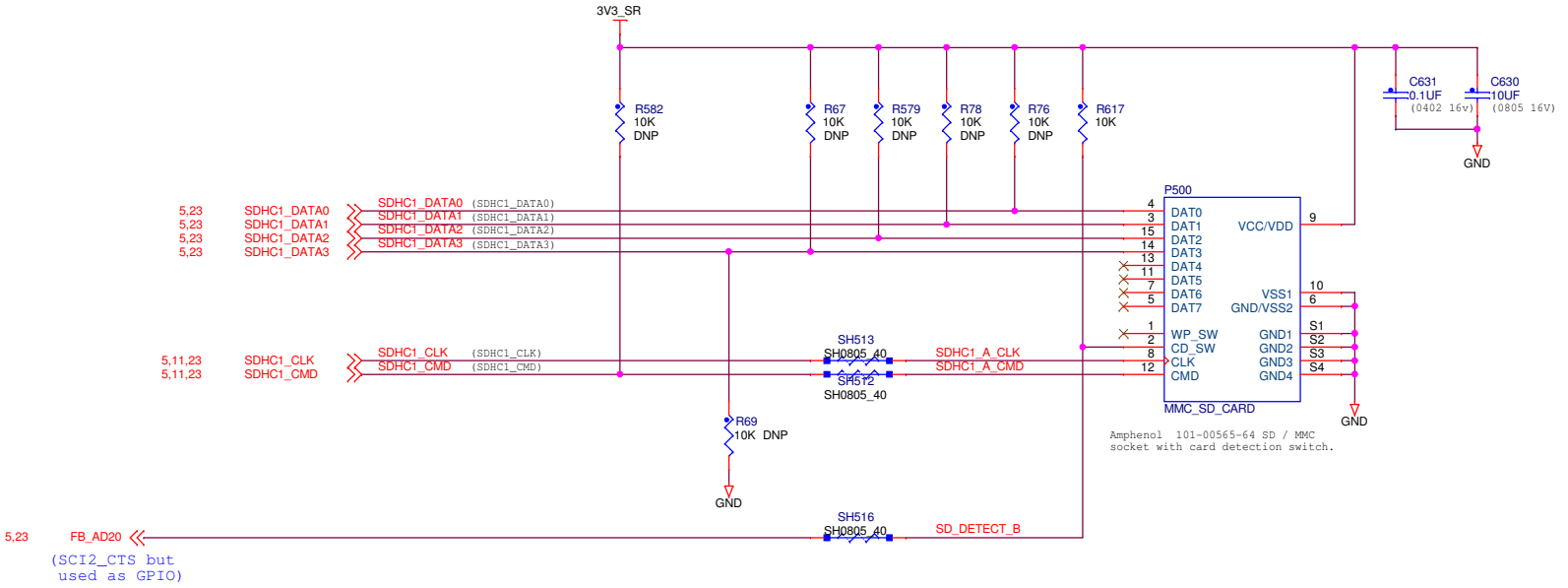

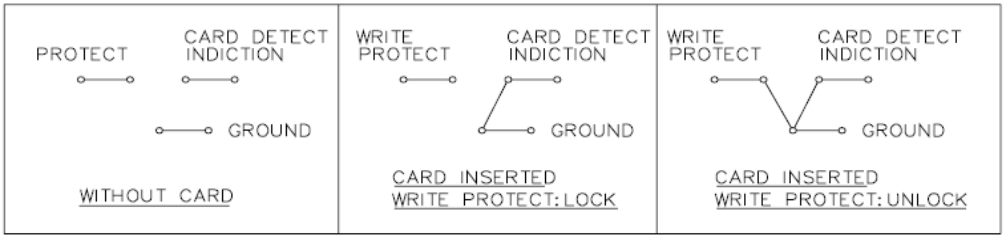

Note: Modifications from Rev.D 27419:
- SD socket changed to type with card detection switch, routed to pin FB_AD[20],
- Series 20-Ohm in SDHC1_CLK line deleted.

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **SD Card Slot**

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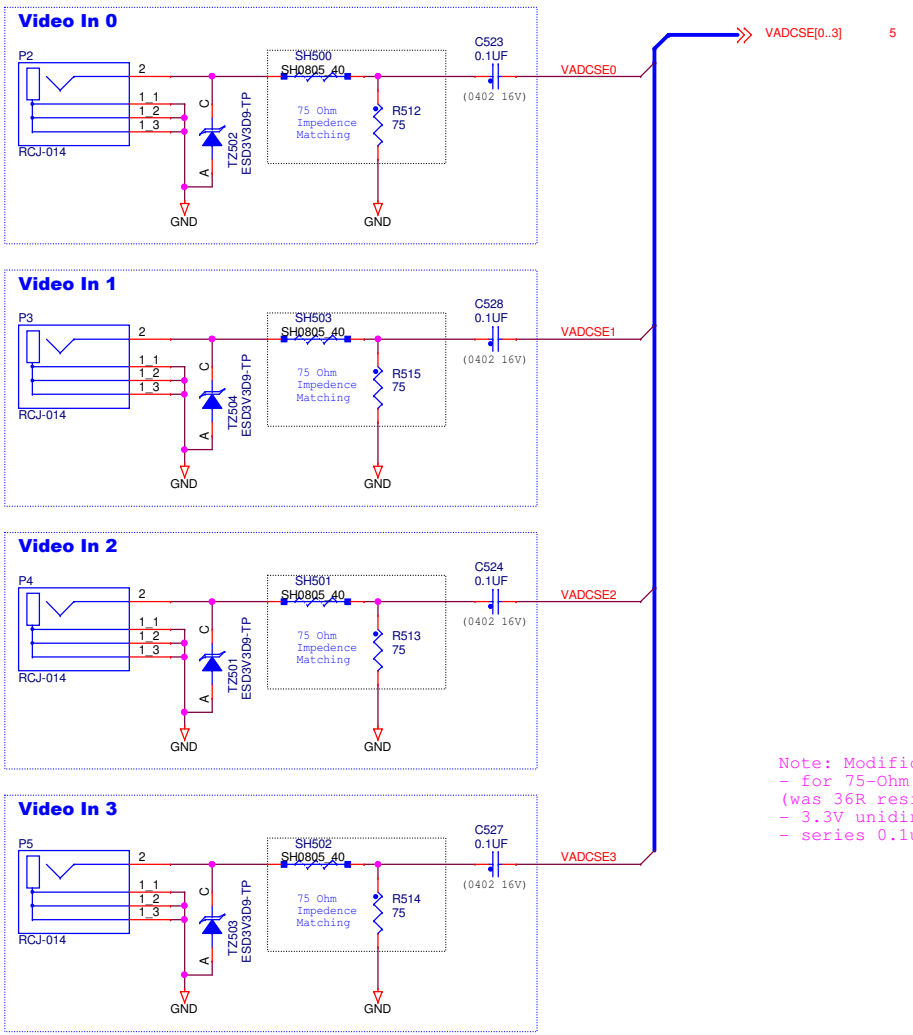
ADC (VADC) Inputs



RCA Connectors

Note: Modifications from Rev.D 27419:
- for 75-Ohm impedence matching, changed to series "Short" (was 36R resistor) with 75R pull-down (was 39R),
- 3.3V unidirectonal TVSs instead of 30V bidir. ones,
- series 0.1uF instead of 47nF (value unification).

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **Video ADC (VADC) Inputs**

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rface

Vybrid 364 BGA
Package 4of4 DCU Pins

SVF522R3K1CMK4

PTE21/DCU0_B0	V16	DCU0_B0
PTE22/DCU0_B1	W17	DCU0_B1
PTE23/DCU0_B2/RCON12	J17	DCU0_B2
PTE24/DCU0_B3/RCON13	D19	DCU0_B3
PTE25/DCU0_B4/RCON14	C19	DCU0_B4
PTE26/DCU0_B5/RCON15	C20	DCU0_B5
PTE27/DCU0_B6/RCON16	B20	DCU0_B6
PTE28/DCU0_B7/RCON17/EWM_out	K16	DCU0_B7
PTE13/DCU0_G0	Y16	DCU0_G0
PTE14/DCU0_G1	W15	DCU0_G1
PTE15/DCU0_G2/RCON6	L18	DCU0_G2
PTE16/DCU0_G3/RCON7	L20	DCU0_G3
PTE17/DCU0_G4/RCON8	K20	DCU0_G4
PTE18/DCU0_G5/RCON9	K19	DCU0_G5
PTE19/DCU0_G6/RCON10	K18	DCU0_G6
PTE20/DCU0_G7/RCON11/EWM_in	A12	DCU0_G7
PTE5/DCU0_R0	T16	DCU0_R0
PTE6/DCU0_R1	W16	DCU0_R1
PTE7/DCU0_R2/RCON0	M20	DCU0_R2
PTE8/DCU0_R3/RCON1	M19	DCU0_R3
PTE9/DCU0_R4/RCON2	M17	DCU0_R4
PTE10/DCU0_R5/RCON3	M16	DCU0_R5
PTE11/DCU0_R6/RCON4	L16	DCU0_R6
PTE12/DCU0_R7/DSPI1_PCS3/RCON5/LPT_ALT0	L17	DCU0_R7
PTE0/DCU0_HSYNC/DCU0_TCON1/BOOTMOD1	N16	DCU0_HSYNC
PTE1/DCU0_VSYNC/DCU0_TCON2/BOOTMOD0	N18	DCU0_VSYNC
PTE2/DCU0_PCLK	N19	DCU0_PCLK
PTE3/DCU0_TAG/DCU0_TCON0/ADC0SE5	Y15	DCU0_TAG
PTE4/DCU0_DE/DCU0_TCON3	N20	DCU0_DE

DCU0_B[0..7] 7
DCU0_G[0..7] 7
DCU0_R[0..7] 7

TPV29
TPV33

7 DCU0_VSYNC (BOOTMOD[0])
7 DCU0_HSYNC (BOOTMOD[1])

5,7 SAI1_TX_SYNC (ADC1SE5) R88 0 DCU_YD
DCU0_TAG (GPIO) R90 0 DCU_XR
5 RMII1_TXEN (ADC1SE7) R87 560 DCU_XL_J
5,7 SAI1_TX_DATA (GPIO) R83 560 DCU_YU_J

Prevent resistive touch panel from being touched while booting up. Critical for RCON operation (I/Os shared).

To read resitive touch panel:

2 — 1 & 2 Require ADC input plus ability to drive HIGH
3 — 0 & 3 Need ability to drive HIGH or LOW

1 — J19: 1 Default: 1-2, 2 DCU_XL
0 — J18: 1 Default: 1-2, 2 DCU_YU

I2C Input (alternative)

5,6,22 CAN1_TX — CAN1_TX (I2C1_SDA)
5,6,22 CAN1_RX — CAN1_RX (I2C1_SCL)

Routed to RCON Pull-Up / -Down

7 DCU0_R2
7 DCU0_R3
7 DCU0_R4
7 DCU0_R5
7 DCU0_R6
7 DCU0_R7

7 DCU0_G2
7 DCU0_G3
7 DCU0_G4
7 DCU0_G5
7 DCU0_G6
7 DCU0_G7

7 DCU0_B2
7 DCU0_B3
7 DCU0_B4
7 DCU0_B5
7 DCU0_B6
7 DCU0_B7

External reset:
- Valid for HDMI card,
- Invalid for MX51 LCD panel.

5 RESET_B — R70 10K DNP (HDMI_I2C_SDA) DCU_XL, (HDMI_I2C_SCLK) DCU_YU, SH514 SH515 SH0805_40 (RESET_B)

Reset pulled low to hold connected device in reset and its TX pins (if relevant) into Hi-Z until actively released by MCU via GPIO. Critical for RCON operation of shared DCU lines.

R71 10K — GND

24-bit DCU Daughtercard Connector (Standard)

Compatible graphic devices / daughtercards:
- HDMI (FSL # MCIMXHDMICARD/ # 26673),
- Display (FSL # LCD-WVGA-7IN-1 / # 28239)

P20: SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8 — QSH-060-01-L-D-A

1V8_LR, 3V3_SR, 5V0_SR

DCU0_PCLK (DISP_CLOCKIN)

HDMI_SCLK (SPDIF_OUT) HDMI_SPDIF TP46 TP47
HDMI_SD0 HDMI_WS TP48 TP49

Bus speed ~35MHz max.

(DISP_DAT0)	DCU0_B0	
(DISP_DAT1)	DCU0_B1	
(DISP_DAT2)	DCU0_B2	
(DISP_DAT3)	DCU0_B3	
(DISP_DAT4)	DCU0_B4	
(DISP_DAT5)	DCU0_B5	
(DISP_DAT6)	DCU0_B6	
(DISP_DAT7)	DCU0_B7	
(DISP_DAT8)	DCU0_G0	
(DISP_DAT9)	DCU0_G1	
(DISP_DAT10)	DCU0_G2	
(DISP_DAT11)	DCU0_G3	
(DISP_DAT12)	DCU0_G4	
(DISP_DAT13)	DCU0_G5	
(DISP_DAT14)	DCU0_G6	
(DISP_DAT15)	DCU0_G7	
(DISP_DAT16)	DCU0_R0	
(DISP_DAT17)	DCU0_R1	
(DISP_DAT18)	DCU0_R2	
(DISP_DAT19)	DCU0_R3	
(DISP_DAT20)	DCU0_R4	
(DISP_DAT21)	DCU0_R5	
(DISP_DAT22)	DCU0_R6	
(DISP_DAT23)	DCU0_R7	
(DISP_VSYNC)	DCU0_VSYNC	
(DISP_BRIGHTN.)	D_BRIGHT	
(DISP_HSYNC)	DCU0_HSYNC	
(DISP_DRDY)	DCU0_DE	

R86 10K — PWR_EN

DCU_YU (DISP_TOP)
DCU_YD (DISP_BOTTOM)
DCU_XL (DISP_LEFT)
DCU_XR (DISP_RIGHT)

R618 10K

DS8 DNP LED_GREEN (0603 35mcd) — Label "DVI_DET_L"
DS7 DNP LED_GREEN (0603 35mcd) — Label "DVI_DET_H"

R96 1K DNP (0603 5%) — INT

Layout note: all DCU traces 50-ohm.

Note: Modifications from Rev.D 27419:
- Universal DCU daughter-card connector used,
- Vybrid's TRACED4 pin used as optional RESET_B.

freescale

ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **EVB-VF522R3**

Page Title: **DCU Interface**

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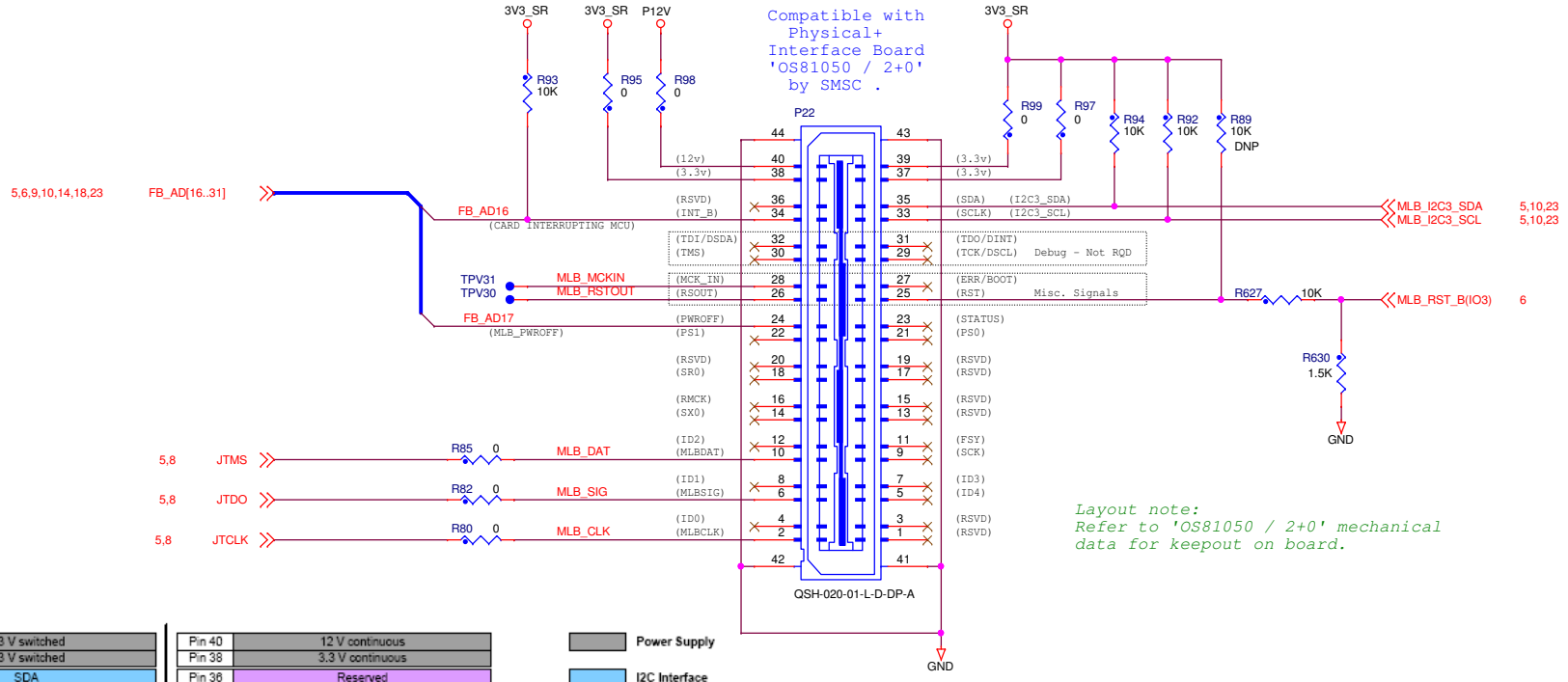
B) Daughtercard Connections



Layout note:
Refer to 'OS81050 / 2+0' mechanical data for keepout on board.

Pin 39	3.3 V switched	Pin 40	12 V continuous
Pin 37	3.3 V switched	Pin 38	3.3 V continuous
Pin 35	SDA	Pin 36	Reserved
Pin 33	SCL	Pin 34	INT
Pin 31	TDO/DINT	Pin 32	TDI/DSDA
Pin 29	TCK/DSCL	Pin 30	TMS
Pin 27	ERR/BOOT	Pin 28	MCK_IN
Pin 25	RST	Pin 26	RSOUT
Pin 23	STATUS (STATUS/NOACT/SCBUS)	Pin 24	PWROFF
Pin 21	PS0	Pin 22	PS1
Pin 19	Reserved	Pin 20	Reserved
Pin 17	Reserved	Pin 18	SR0
Pin 15	Reserved (MOST_RXP)	Pin 16	RMCK
Pin 13	Reserved (MOST_RXN)	Pin 14	SX0
Pin 11	FSY	Pin 12	PhyIntfBrd_ID2
Pin 9	SCK	Pin 10	MLBDAT
Pin 7	PhyIntfBrd_ID3	Pin 8	PhyIntfBrd_ID1
Pin 5	PhyIntfBrd_ID4	Pin 6	MLBSIG
Pin 3	Reserved	Pin 4	PhyIntfBrd_ID0
Pin 1	Reserved	Pin 2	MLBCLK

- Power Supply
- I2C Interface
- Debug & JTAG Interface
- Misc Signals
- Board ID
- Network Interface
- RMCK
- I2S Interface
- MediaLB 3-Pin

Note: Modifications from Rev.D 27419:
- INT line pull-up added,
- Series resistor into RST line added.

Figure 5-1: Connector Interface to Main Board

freescale

ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **MOST (MLB) Daughtercard Connections**

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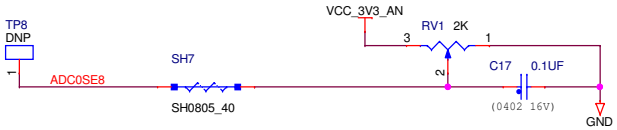
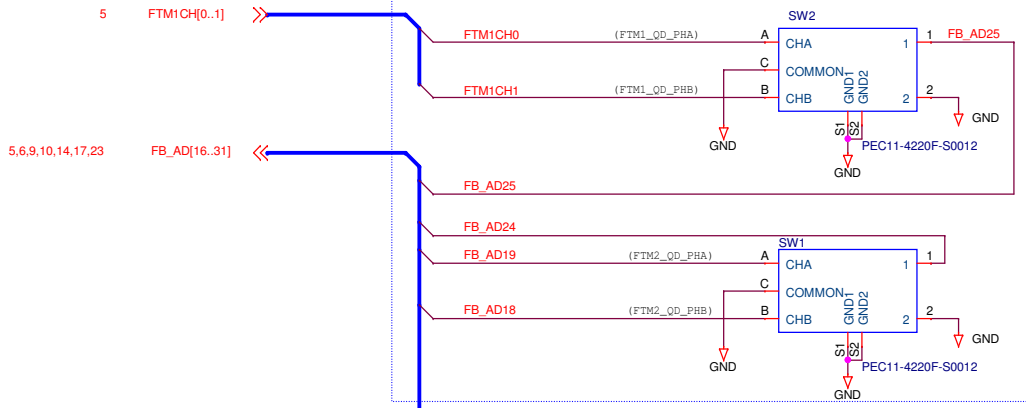
ipherals, Audio Controls, and GPIOs

ADC Input Potentiometer and Test Point

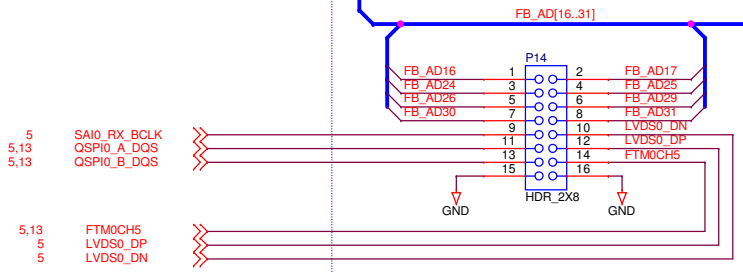
(Ideally run from linear 3.3V regulator to provide stable input voltage).



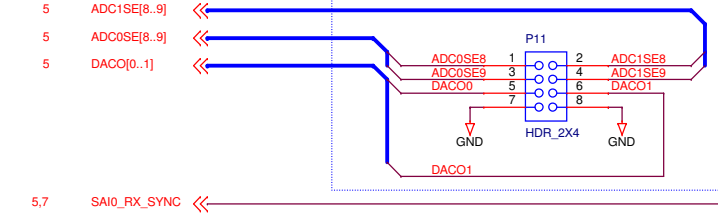
Incremental Encoders (Volume and Tuning)



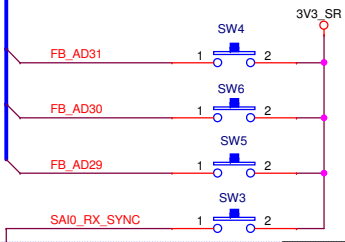
Header for Digital Accessible GPIOs



Header for Analog Accessible GPIOs



Push Buttons for Presets



Caution:
SW3 is also an RCON pin controlled via switches on page 9. If Pulled high for RCON, this switch will have no effect.

freescale

ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **User Peripherals, Audio Controls, and GPIOs**

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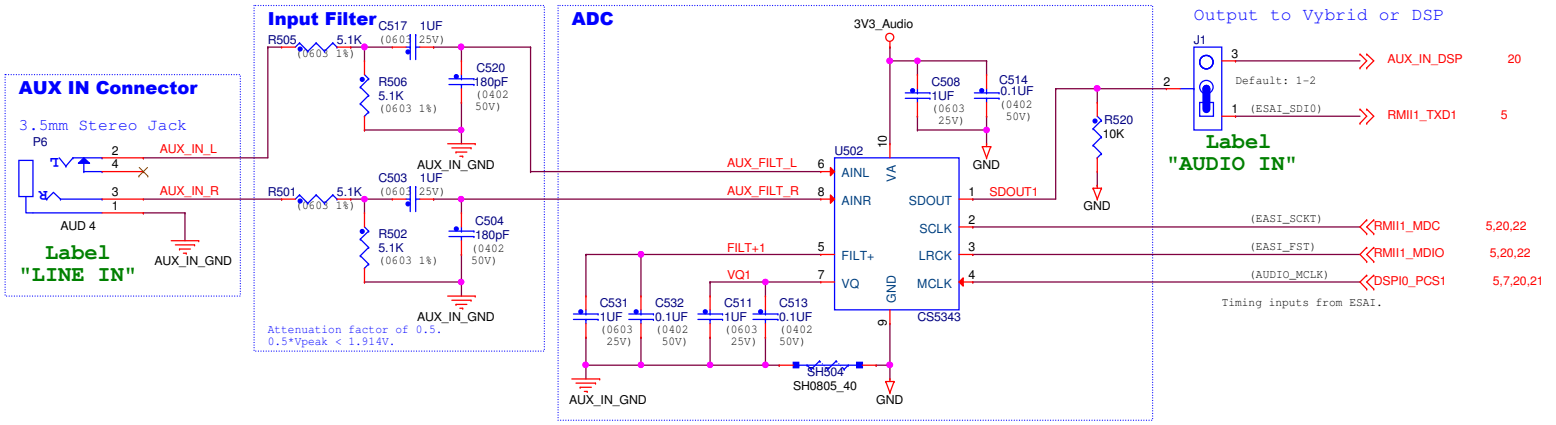
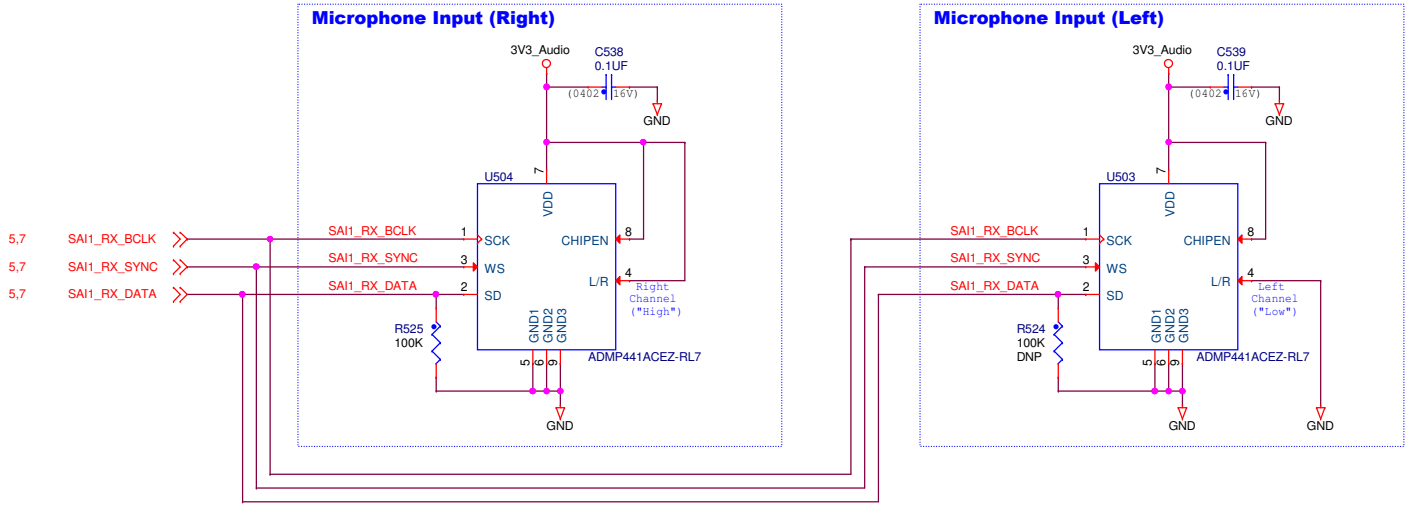
Line and Microphone Inputs



Layout note:
Should have clean GNDs - tips in Datasheet.



Note: Modifications from Rev.D 27419:
- Separate AUX_IN_GND created.

freescale

ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	EVB-VF522R3		
Page Title:	Audio 1: Line and Microphone Inputs		
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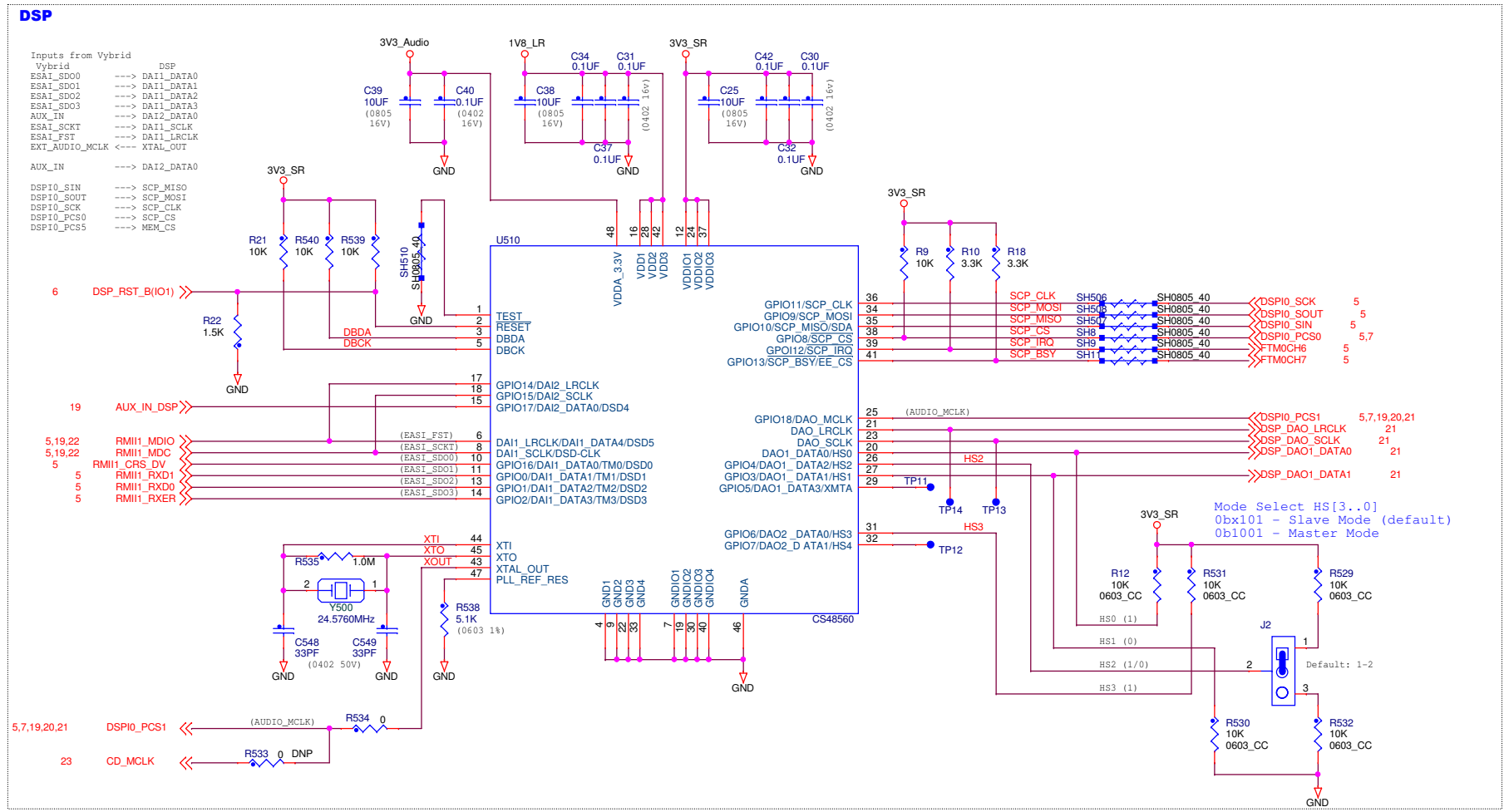
DSP
Inputs from Vybrid
Vybrid DSP
ESAI_SDO0 ---> DAI1_DATA0
ESAI_SDO1 ---> DAI1_DATA1
ESAI_SDO2 ---> DAI1_DATA2
ESAI_SDO3 ---> DAI1_DATA3
AUX_IN ---> DAI2_DATA0
ESAI_SCKT ---> DAI1_SCLK
ESAI_FST ---> DAI1_LRCLK
EXT_AUDIO_MCLK <--- XTAL_OUT
AUX_IN ---> DAI2_DATA0
DSPI0_SIN ---> SCP_MISO
DSPI0_SOUT ---> SCP_MOSI
DSPI0_SCK ---> SCP_CLK
DSPI0_PCS0 ---> SCP_CS
DSPI0_PCS5 ---> MEM_CS
3V3_Audio
1V8_LR
3V3_SR
C39 10UF (0805 16V)
C40 0.1UF (0402 16V)
C38 10UF (0805 16V)
C34 0.1UF
C31 0.1UF
C37 0.1UF
C25 10UF (0805 16V)
C42 0.1UF
C30 0.1UF
C32 0.1UF
GND
R21 10K
R540 10K
R539 10K
SH510 SH0805_40
U510
VDDA_3.3V
VDD1
VDD2
VDD3
VDDIO1
VDDIO2
VDDIO3
R9 10K
R10 3.3K
R18 3.3K
6 DSP_RST_B(IO1)
R22 1.5K
DBDA
DBCK
TEST
RESET
DBDA
DBCK
GPIO11/SCP_CLK
GPIO9/SCP_MOSI
GPIO10/SCP_MISO/SDA
GPIO8/SCP_CS
GPOI12/SCP_IRQ
GPIO13/SCP_BSY/EE_CS
SCP_CLK
SCP_MOSI
SCP_MISO
SCP_CS
SCP_IRQ
SCP_BSY
SH0805_40
DSPI0_SCK 5
DSPI0_SOUT 5
DSPI0_SIN 5
DSPI0_PCS0 5,7
FTM0CH6 5
FTM0CH7 5
19 AUX_IN_DSP
GPIO14/DAI2_LRCLK
GPIO15/DAI2_SCLK
GPIO17/DAI2_DATA0/DSD4
5,19,22 RMII1_MDIO
5,19,22 RMII1_MDC
5 RMII1_CRS_DV
5 RMII1_RXD1
5 RMII1_RXD0
5 RMII1_RXER
(EASI_FST)
(EASI_SCKT)
(EASI_SDO0)
(EASI_SDO1)
(EASI_SDO2)
(EASI_SDO3)
DAI1_LRCLK/DAI1_DATA4/DSD5
DAI1_SCLK/DSD-CLK
GPIO16/DAI1_DATA0/TM0/DSD0
GPIO0/DAI1_DATA1/TM1/DSD1
GPIO1/DAI1_DATA2/TM2/DSD2
GPIO2/DAI1_DATA3/TM3/DSD3
GPIO18/DAO_MCLK
DAO_LRCLK
DAO_SCLK
DAO1_DATA0/HS0
GPIO4/DAO1_ DATA2/HS2
GPIO3/DAO1_ DATA1/HS1
GPIO5/DAO1_DATA3/XMTA
(AUDIO_MCLK)
HS2
TP11
TP14
TP13
DSPI0_PCS1 5,7,19,20,21
DSP_DAO_LRCLK 21
DSP_DAO_SCLK 21
DSP_DAO1_DATA0 21
DSP_DAO1_DATA1 21
GPIO6/DAO2 _DATA0/HS3
GPIO7/DAO2_D ATA1/HS4
HS3
TP12
XTI
XTO
XOUT
R535 1.0M
Y500 24.5760MHz
C548 33PF (0402 50V)
C549 33PF
R538 5.1K (0603 1%)
XTI
XTO
XTAL_OUT
PLL_REF_RES
GND1
GND2
GND3
GND4
GNDIO1
GNDIO2
GNDIO3
GNDIO4
GNDA
CS48560
Mode Select HS[3..0]
0bx101 - Slave Mode (default)
0b1001 - Master Mode
R12 10K 0603_CC
R531 10K 0603_CC
R529 10K 0603_CC
HS0 (1)
HS1 (0)
HS2 (1/0)
HS3 (1)
J2
Default: 1-2
R530 10K 0603_CC
R532 10K 0603_CC
5,7,19,20,21 DSPI0_PCS1
(AUDIO_MCLK)
R534 0
23 CD_MCLK
R533 0 DNP
Optional Flash
5,7 SAI1_TX_BCLK
(DSPI0_PCS5)
J3
Default: 1-2
SCP_BSY
SCP_MISO
(MCU_MEM_CS)
R7 10K
U2
CE
SO
WP
VSS
VDD
HOLD
SCK
SI
C547 0.1UF (0402 16V)
R528 10K
SCP_CLK
SCP_MOSI
SST25VF032B-80-4I-S2AF
DSP Debug Header
P10
Label "D_ACT"
TP15
(D_ACT)
(DSPI0_PCS5)
SAI1_TX_BCLK
DBDA
DBCK
R536 0 DNP
R537 0 DNP
(Both Resistors 0603_CC)
HDR2X15
DNP
freescale
ICAP Classification: FCP: ___ FIUO: X PUBI: ___
Drawing Title:
EVB-VF522R3
Page Title:
Audio 2: DSP
Size B
Document Number SCH-28141 PDF: SPF-28141
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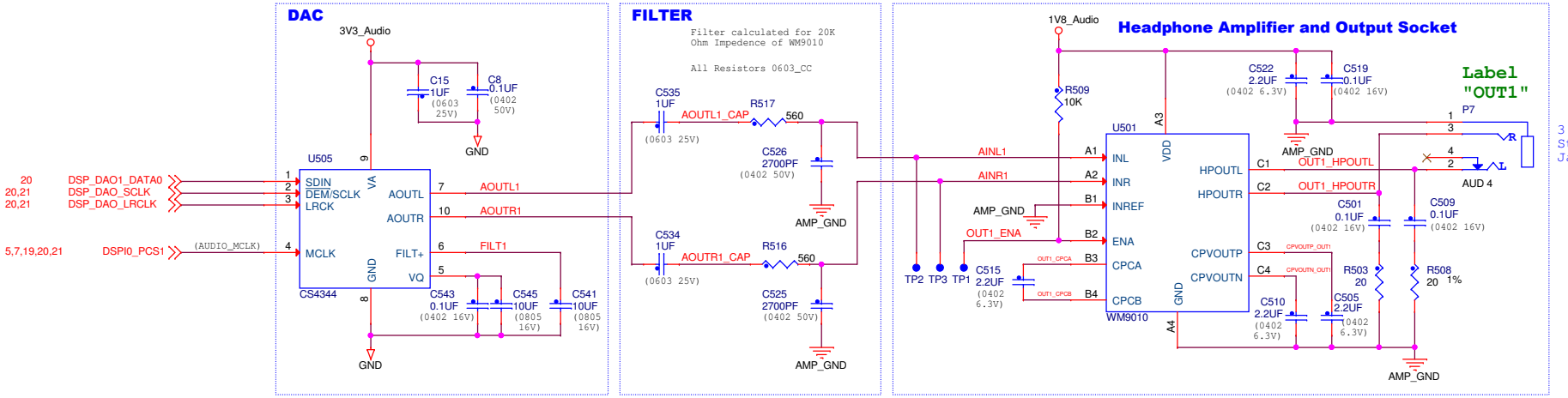
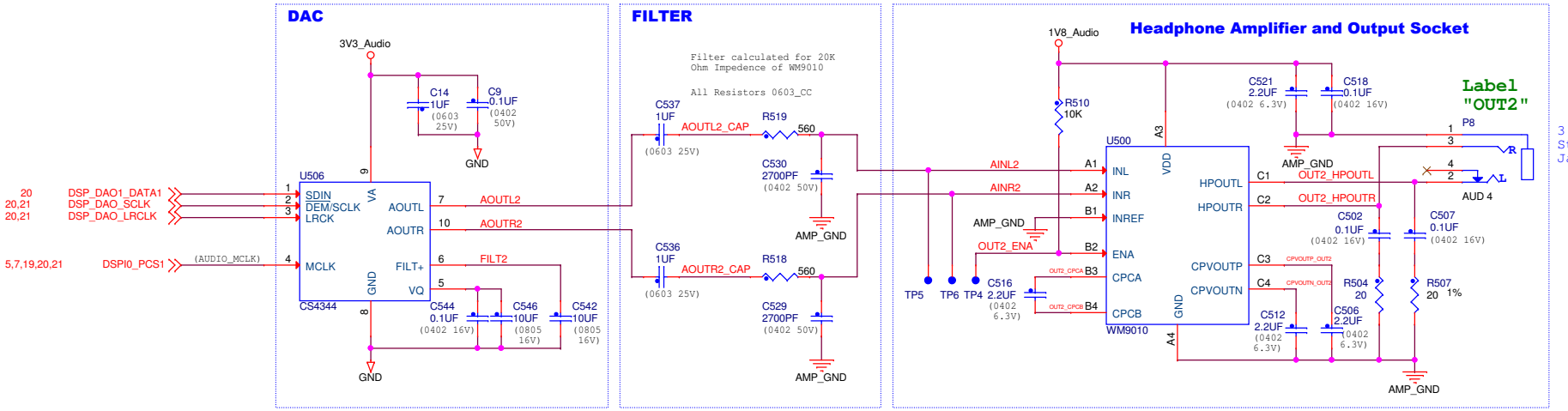
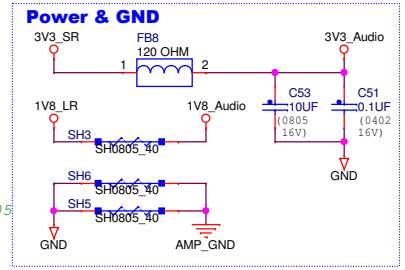
DACs & Amplifier Outputs







Layout note:
- Connect AMP_GND "island" to GND as close to pins 8 of U505 and U506 as possible, with 1 "Short" per IC.

Note: Modifications from Rev.D 27419:
- In FILTER circuit 560 and 2700pF instead of 470 and 3300pF (BOM consolidation).

freescale

ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **Audio 3: DACs & Amplifier Outputs**

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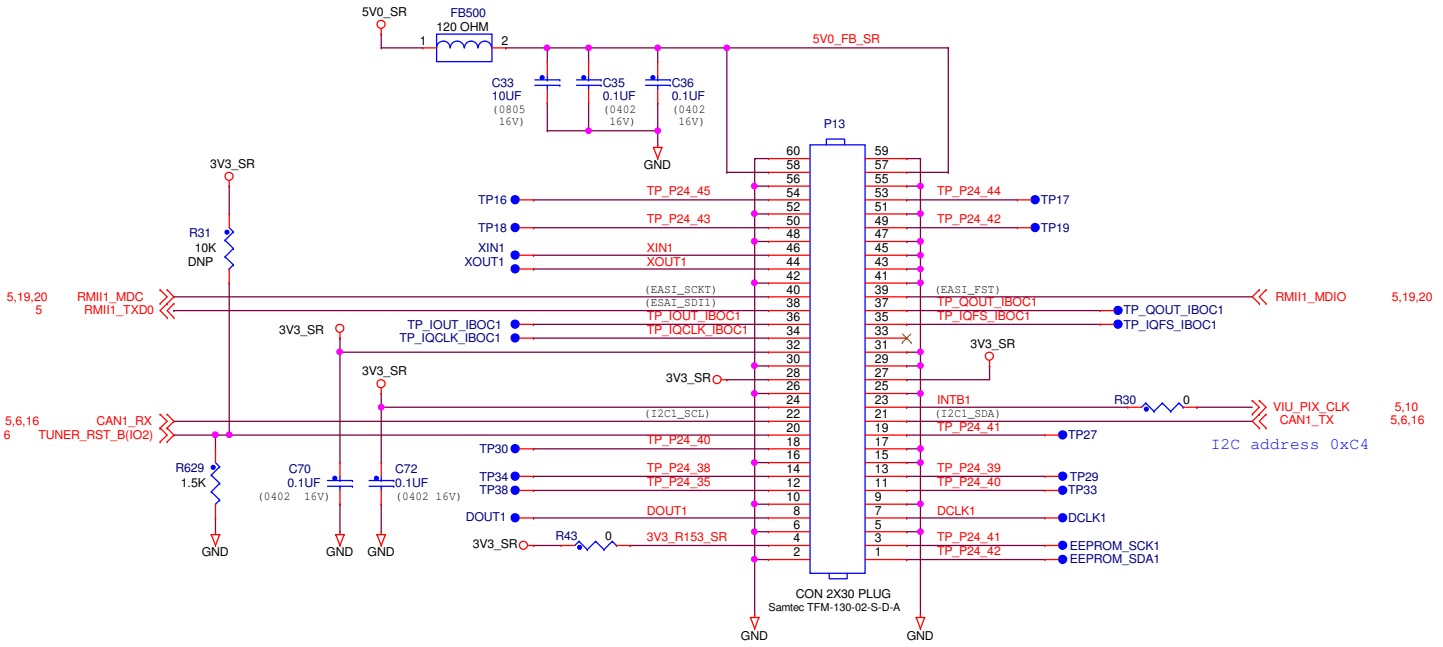
Daughtercard Interface



Compatible with "Si476x LNA-Balun Rev4.0"
RF tuner daughtercard by Silicon Labs.

freescale

ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **RF Tuner Daughtercard Interface**

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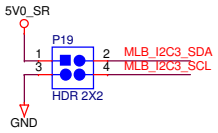
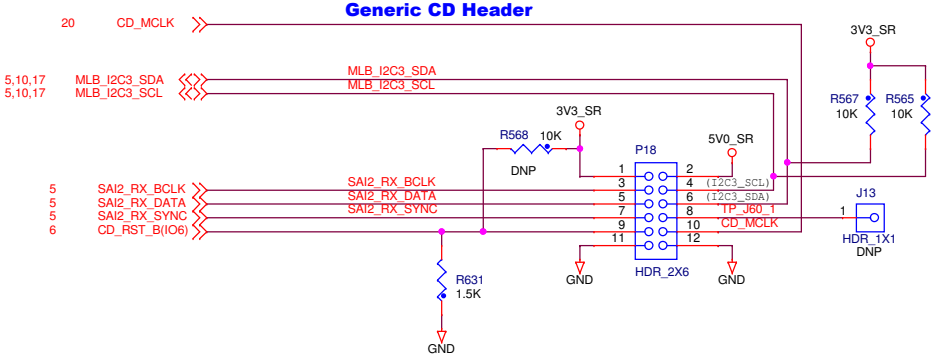
4-Pin Header (I2C3)

(5V power)

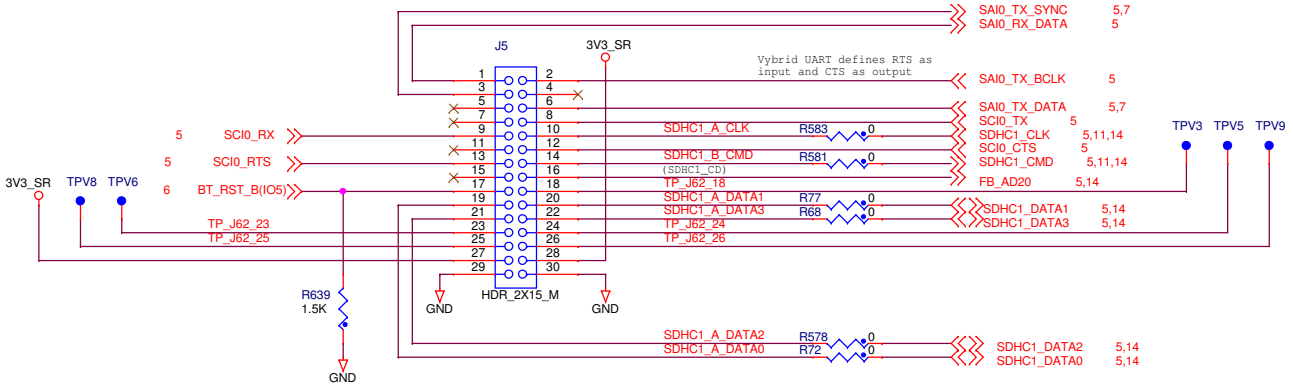


Generic CD Header



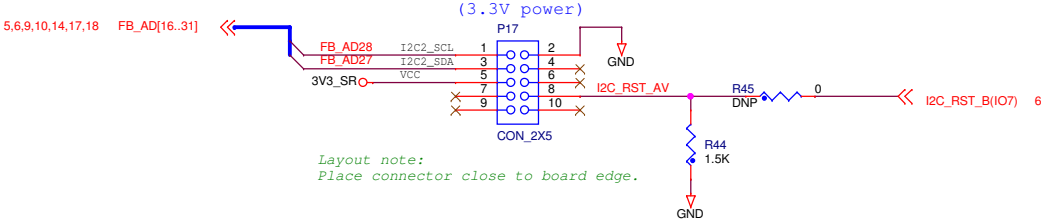
Bluetooth Daughtercard Header

(compatible with
Freescale part number
FD-B-TOOTH-DC)



I2C (Authentication) Daughtercard Header

(3.3V power)



Note: Modifications from Rev.D 27419:
- SCI0_CTS (TRACE_CTL) now used for Bluetooth SCI.
- Bluetooth is now connected to SCI0 rather than SCI2.
- Added LCD 4-pin header (I2C3 interface).
- Connector for different Bluetooth daughtercard type.

freescale

ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **I2C, CD, and Bluetooth Headers**

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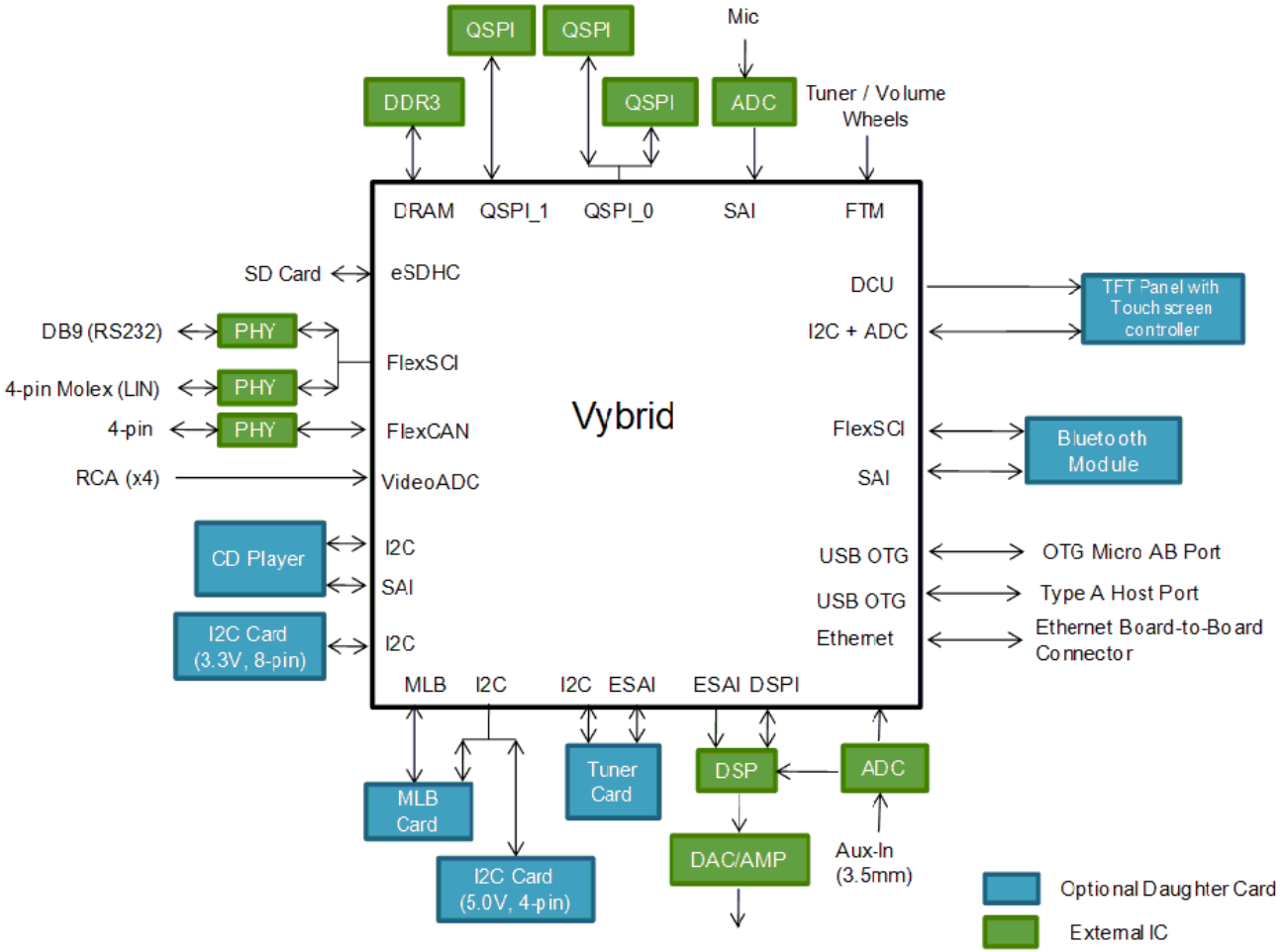
1: Customer EVB Block Diagram



I2C Branch	Device	Write	Read	Speed
1	Tuner	0xc4	0xc5	400kHz
1	Touch Screeen			400kHz
2	IOmux (Reset)	0x30	0x31	400kHz
1	I2C card (3.3V, 8pin)			400kHz
3	Generic CD			400kHz
1	MLB	0x40	0x41	400kHz
3	Ethernet Card	0xD1	0xD2	400kHz
1	Most = MLB			400kHz
1	DCU			400kHz

I2C address of MCIMXHDMICARD/ Agile # 26673, SiI9022A-based HDMI card:

Transmitter Programming Interface (TPI) device address	0x72
CEC Programming Interface (CPI) device address	0xC0
SiI9020-compatible internal registers: first device address	0x72
SiI9020-compatible internal registers: second device address	0x7A

Note: Modifications from Rev.D 27419:
- I2C1 also used for DCU daughtercard connector.
- I2C3 also used for Ethernet daughtercard connector.

freescale

ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **EVB-VF522R3**

Page Title: **Appendix 1: EVB Block Diagram**

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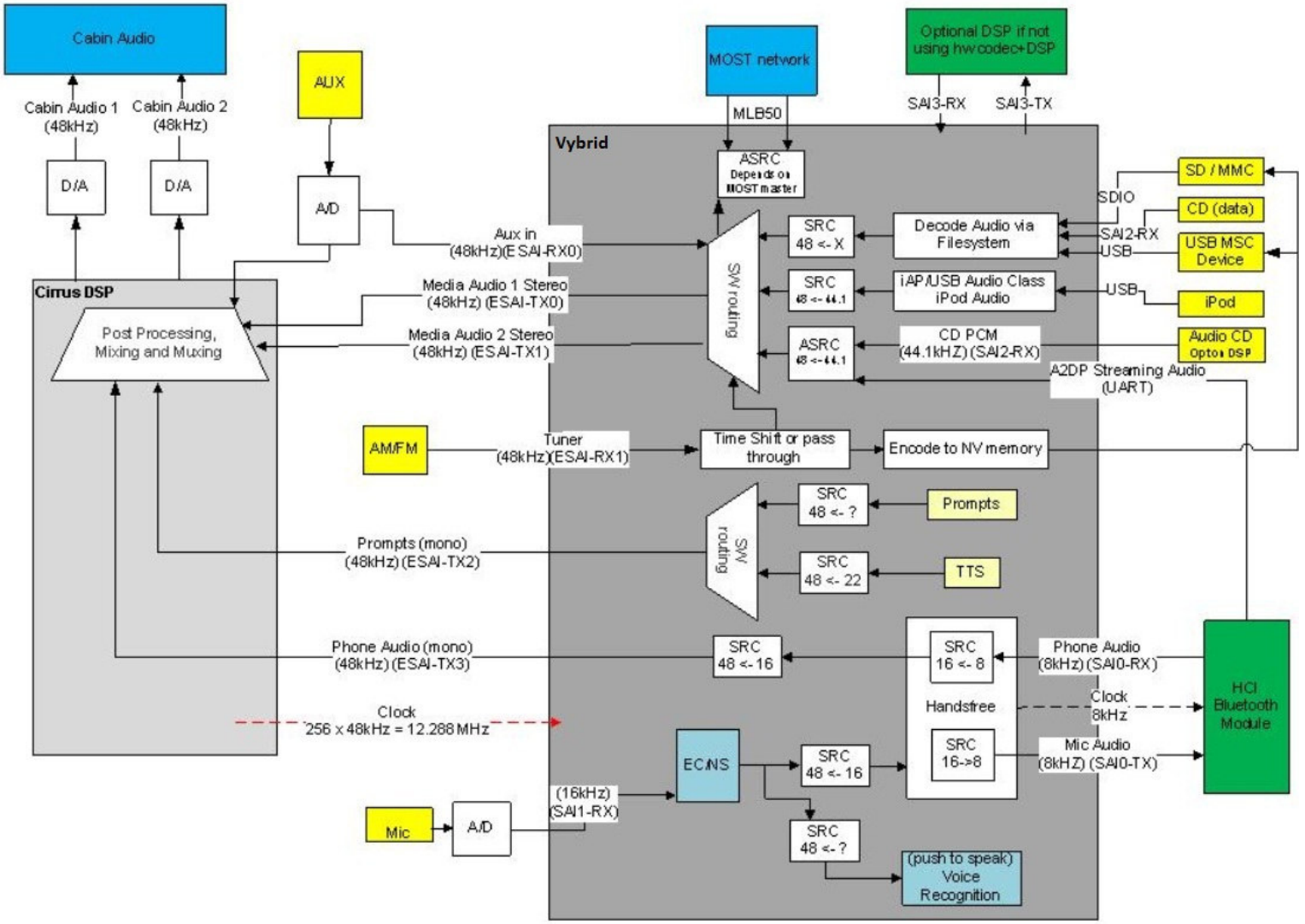
2: Audio Routing Diagram



freescale

ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title:

EVB-VF522R3

Page Title:

Appendix 1: Audio Routing Diagram

Size	Document Number	Rev
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