M5275EVB Evaluation Board

Table Of Contents:

Revision Information

Rev	Date	Designer	Comments
0.7	13 May 04	PBH	Provisional release
0.8	16 June 04	PBH	Updated buffers/transceivers to be dual supply +2.5V & +3.3V
0.9	1 July 04	PBH	Added test points to all the DDR SDRAM signals.
1.0	21 July 04	PBH	Rev 1.0 released schematics for Rev 1.0 EVB

Notes:

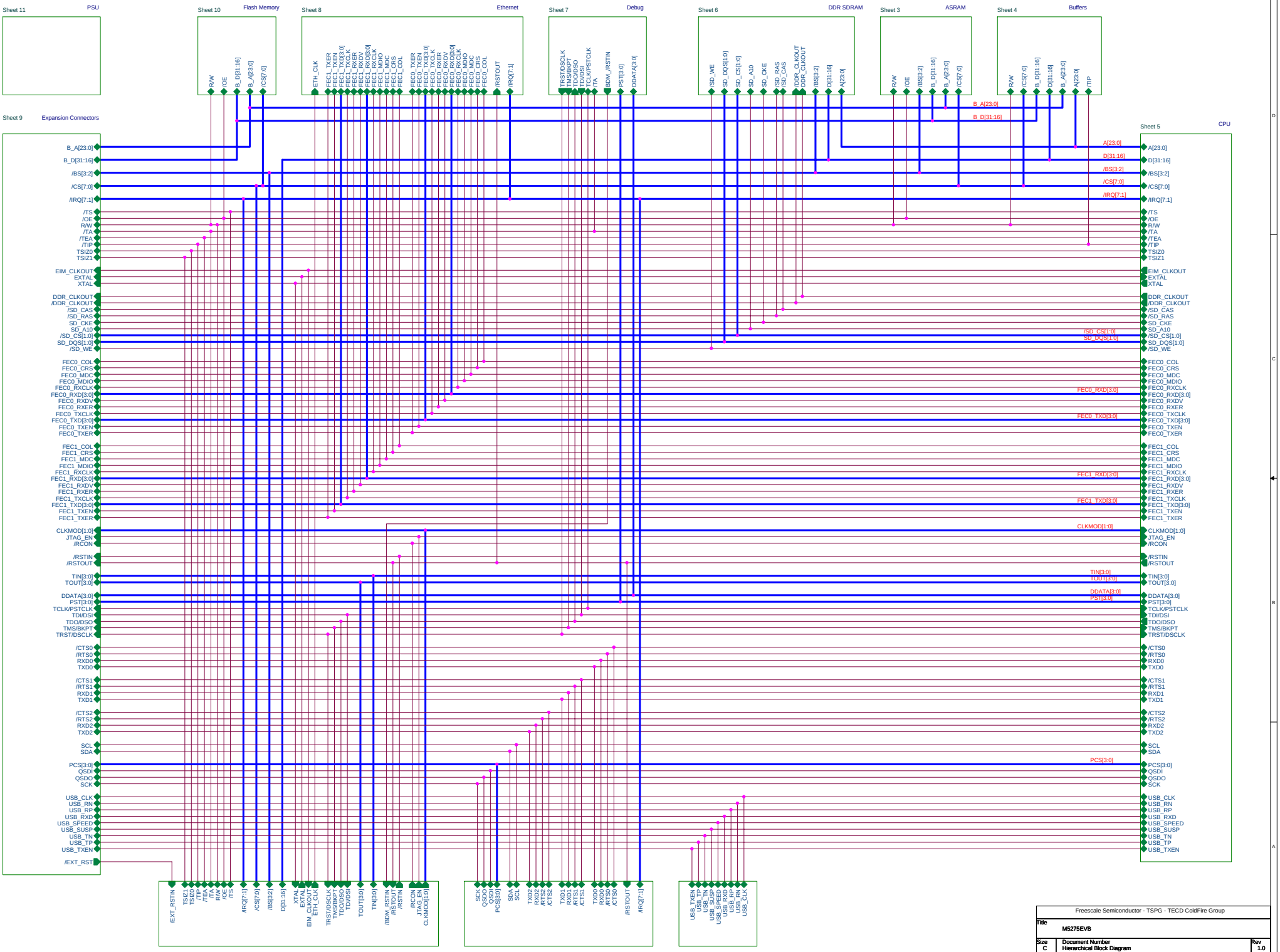
- All decoupling caps less than or equal to 0.1uF are COG SMD 0805 unless otherwise stated
- All decoupling caps greater than 0.1uF are X7R SMD 0805 unless otherwise stated
- All connectors are denoted Jx
- All jumpers are denoted JPx
- All Switches are denoted SWx
- All test points are denoted TPx
- All resistor packs (RPx) and resistors (Rx) are 1% tolerance unless stated otherwise

Freescale Semiconductor - TSPG - TECD ColdFire Group

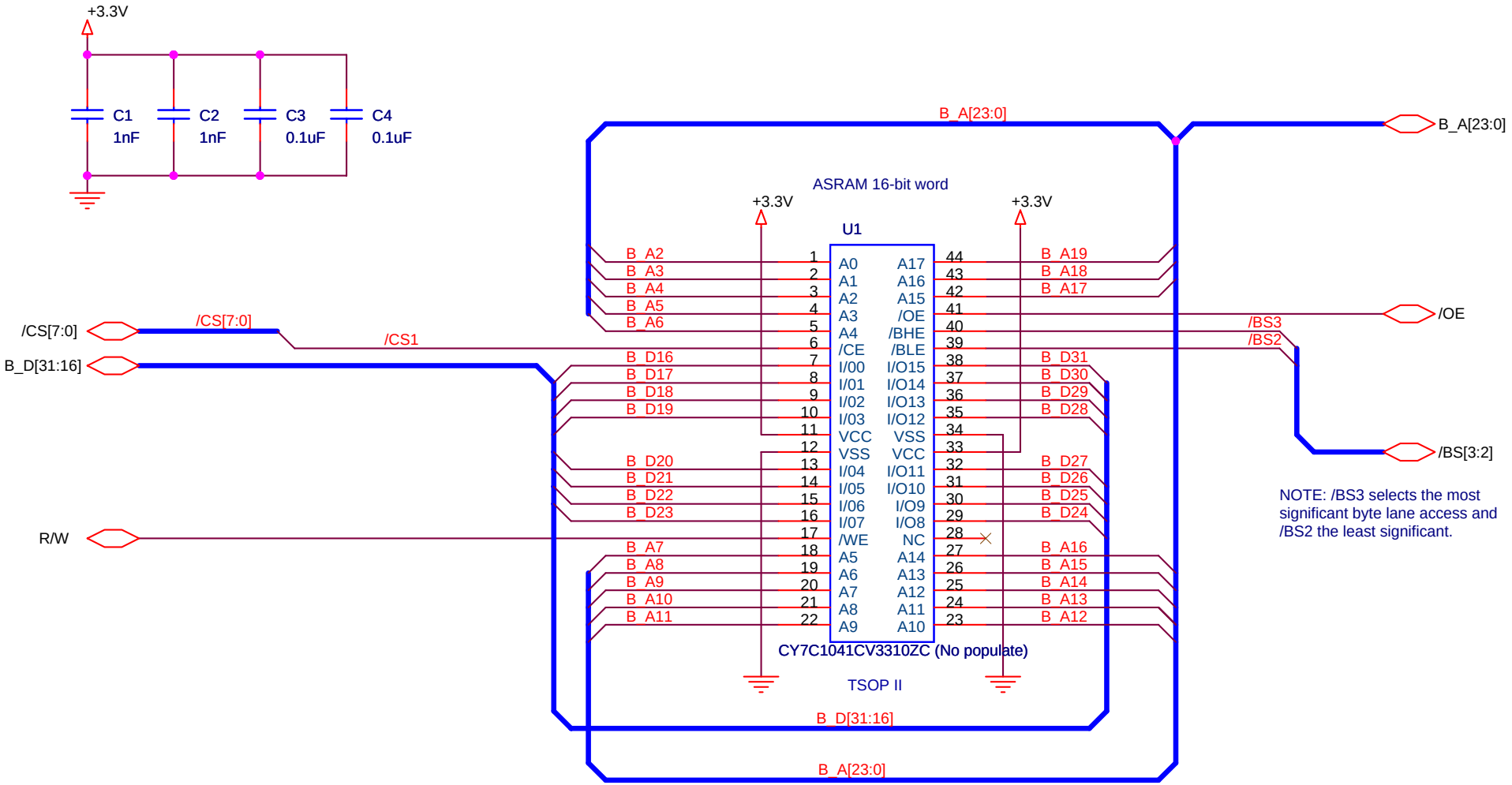
Title

Size B | Document Number M5275EVB | Rev 1.0

Date: Thursday, July 22, 2004 | Sheet 1 of 14



Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title: M5275EVB		
Size: C	Document Number: Hierarchical Block Diagram	Rev: 1.0
Date: Thursday, July 22, 2004	Sheet 2 of 14	



ASRAM is a 256K x 16bit (512KB) device

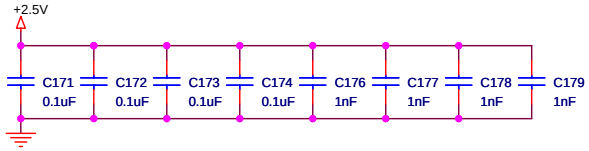
NOTE: Alternative ASRAM's with the same PCB footprint and functionality are :- Renesas HM62W16255HCJP-12

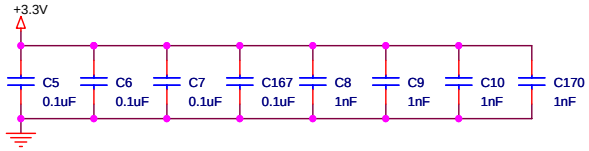
NOTE: Place the SMT footprint for the ASRAM's on the underside of the PCB close to the CPU U6.

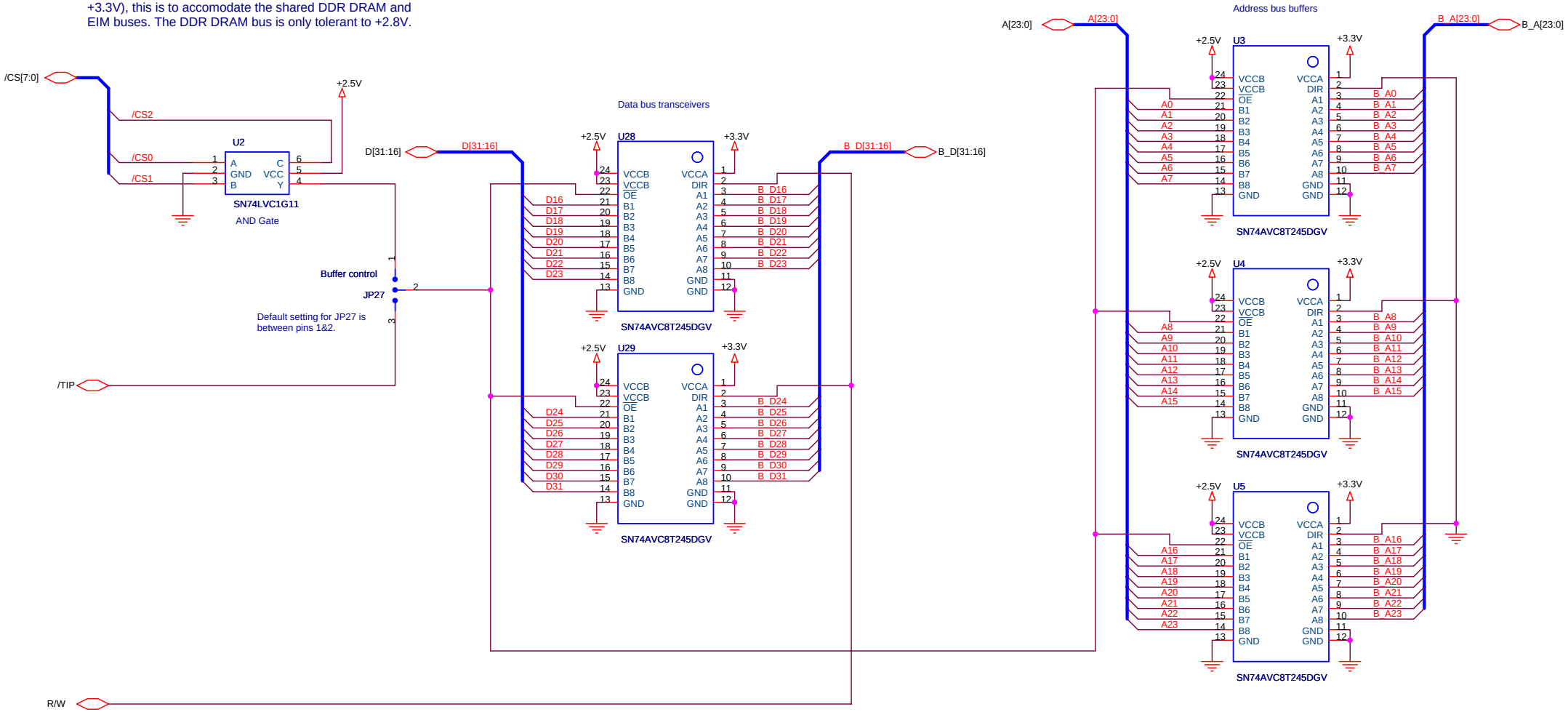
Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title: M5275EVB		
Size: A	Document Number: Asynchronous SRAM	Rev: 1.0
Date: Thursday, July 22, 2004	Sheet 3 of 14	

Address and Data Bus buffers/transceivers are used to buffer the signals for the ASRAM and Flash memories, plus any peripheral connected to /CS2 - this extra chip select is available for use with an external peripheral, perhaps on a daughter-card.

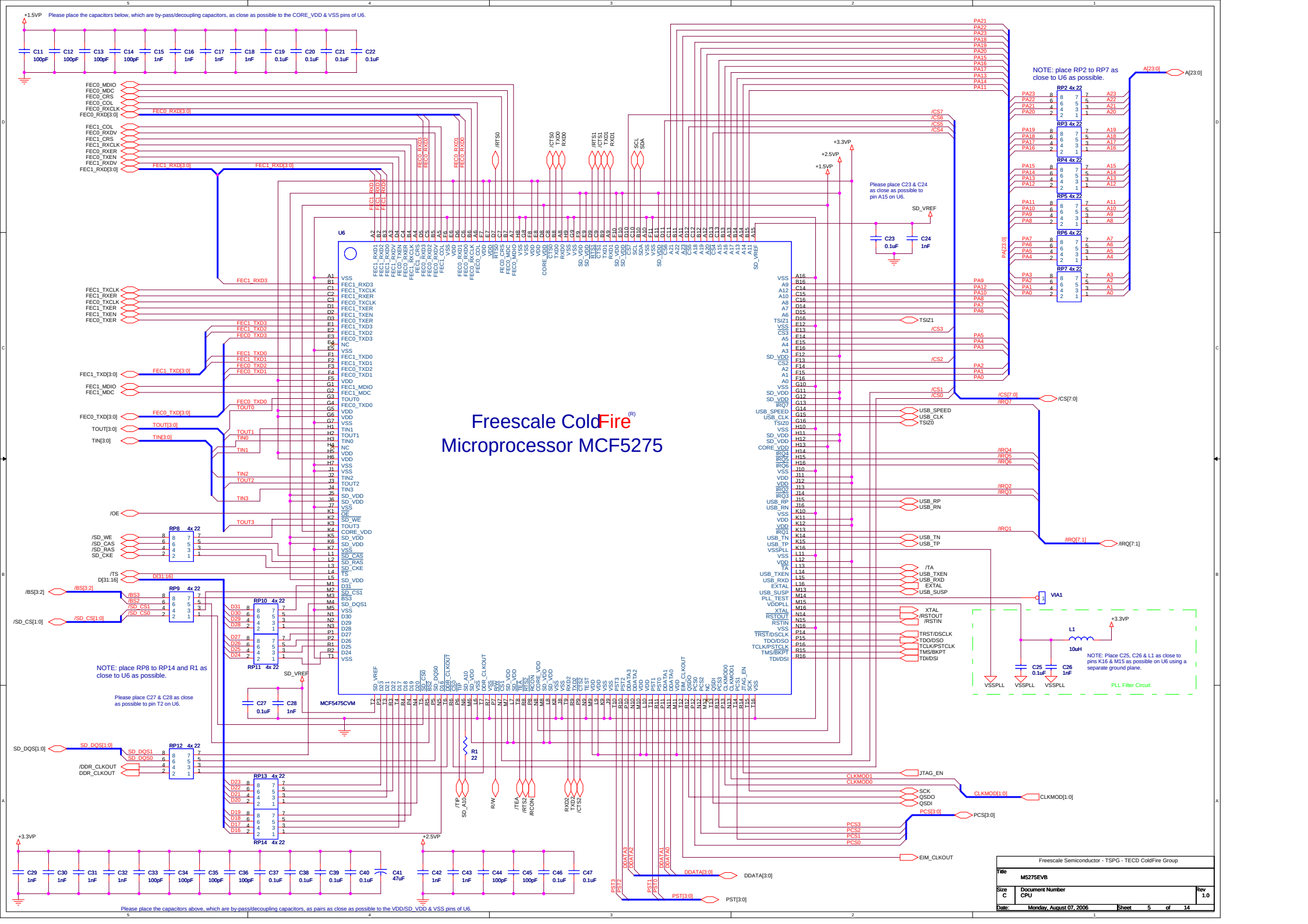
Note: the bus transceivers/buffers are dual supply (+2.5V & +3.3V), this is to accomodate the shared DDR DRAM and EIM buses. The DDR DRAM bus is only tolerant to +2.8V.

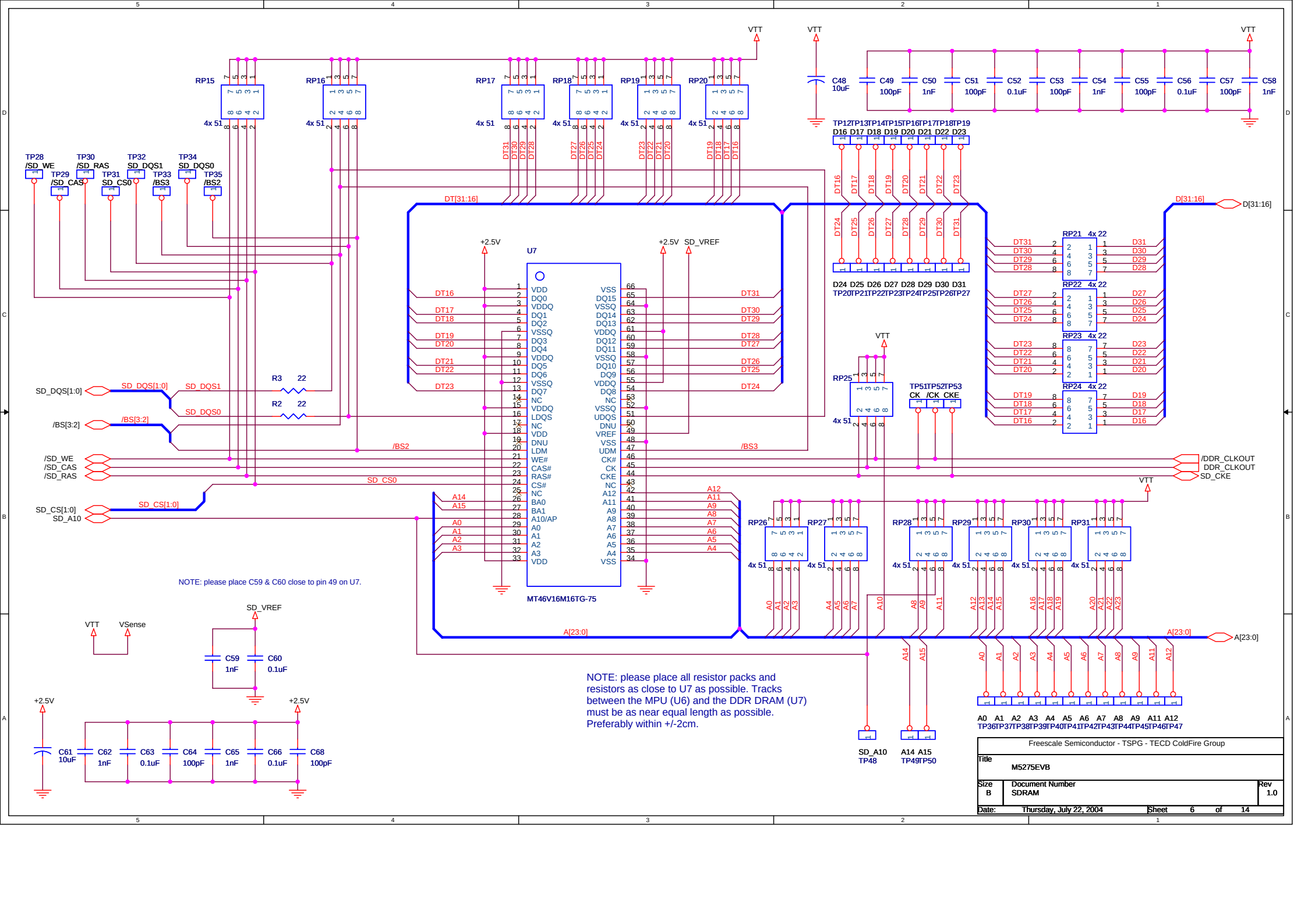


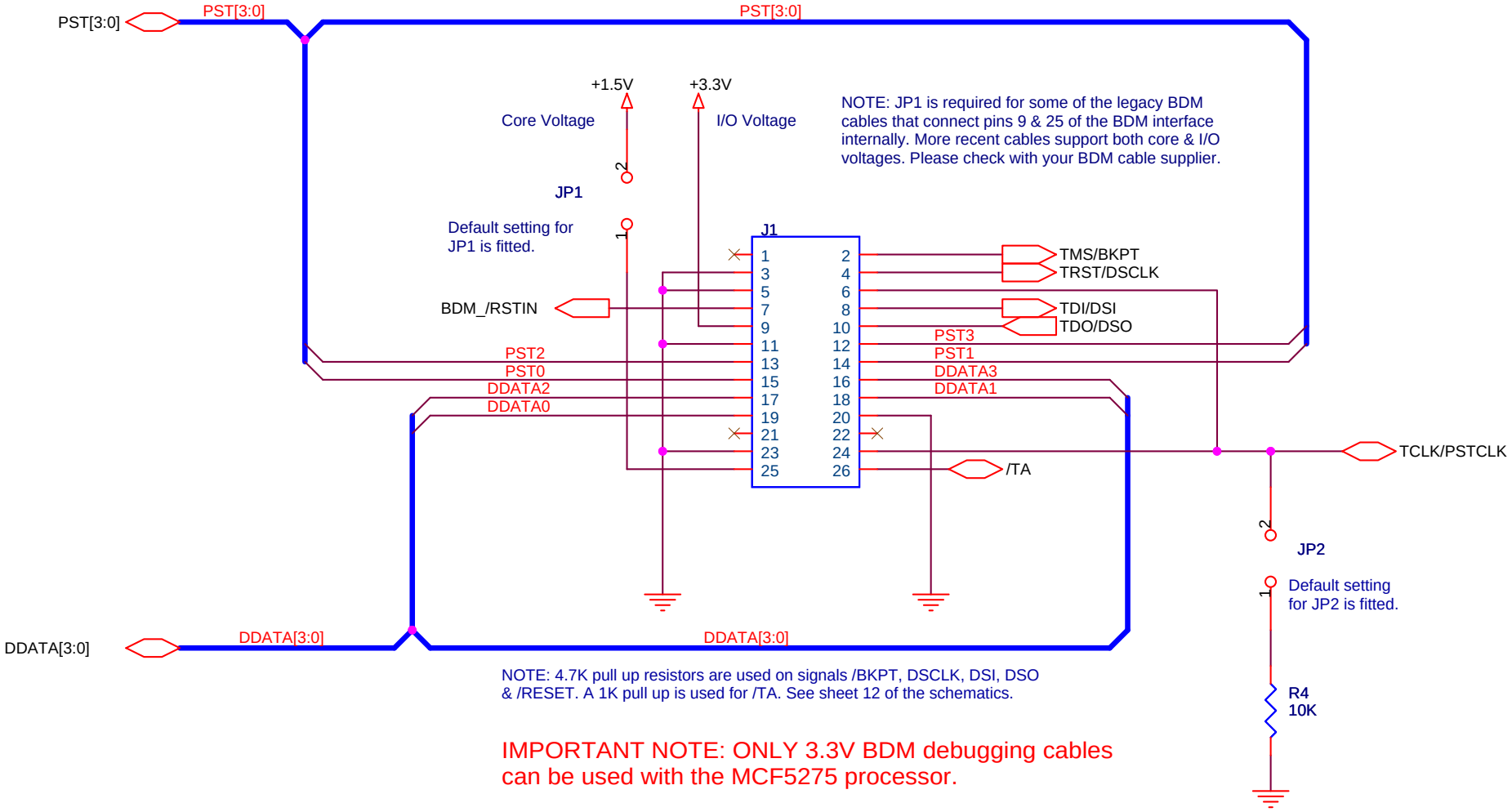




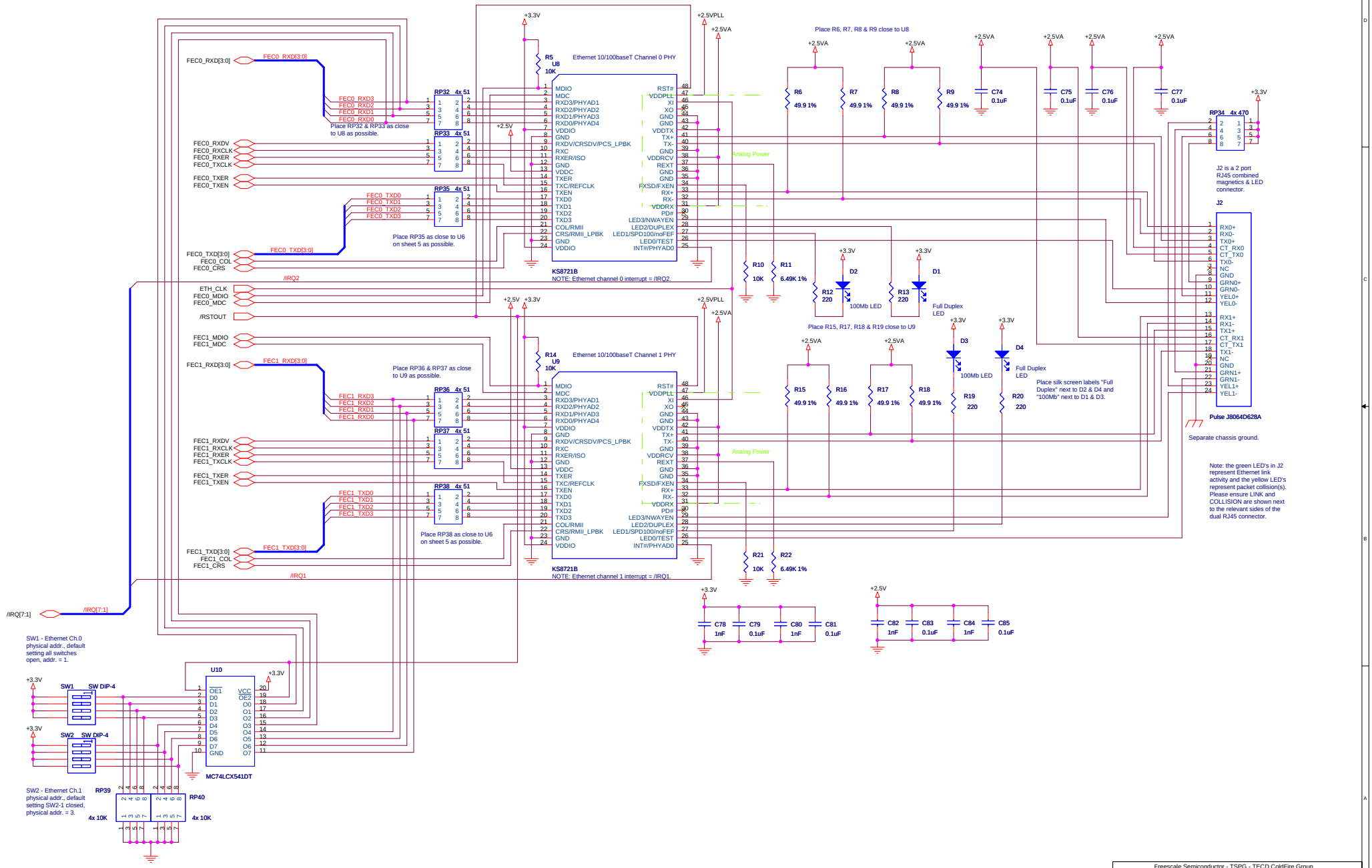
Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title: M5275EVB		
Size: B	Document Number: Buffers	Rev: 1.0
Date: Thursday, July 22, 2004	Sheet 4 of 14	


Please place the capacitors below, which are by-pass/decoupling capacitors, as close as possible to the CORE_VDD & VSS pins of U6.
C11 100pF
C12 100pF
C13 100pF
C14 100pF
C15 1nF
C16 1nF
C17 1nF
C18 1nF
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 0.1uF
NOTE: place RP2 to RP7 as close to U6 as possible.
Please place C23 & C24 as close as possible to pin A15 on U6.
C23 0.1uF
C24 1nF
U6
MCF5475CVM
Freescale ColdFire(R)
Microprocessor MCF5275
NOTE: place RP8 to RP14 and R1 as close to U6 as possible.
Please place C27 & C28 as close as possible to pin T2 on U6.
C27 0.1uF
C28 1nF
R1 22
NOTE: Place C25, C26 & L1 as close to pins K16 & M15 as possible on U6 using a separate ground plane.
L1 10uH
C25 0.1uF
C26 1nF
PLL Filter Circuit
C29 1nF
C30 1nF
C31 1nF
C32 1nF
C33 100pF
C34 100pF
C35 100pF
C36 100pF
C37 0.1uF
C38 0.1uF
C39 0.1uF
C40 0.1uF
C41 47uF
C42 1nF
C43 1nF
C44 100pF
C45 100pF
C46 0.1uF
C47 0.1uF
Please place the capacitors above, which are by-pass/decoupling capacitors, as pairs as close as possible to the VDD/SD_VDD & VSS pins of U6.
Freescale Semiconductor - TSPG - TECD ColdFire Group
Title M5275EVB
Size C
Document Number CPU
Rev 1.0
Date: Monday, August 07, 2006
Sheet 5 of 14


VTT
C48 10uF
C49 100pF
C50 1nF
C51 100pF
C52 0.1uF
C53 100pF
C54 1nF
C55 100pF
C56 0.1uF
C57 100pF
C58 1nF
RP15
RP16
RP17
RP18
RP19
RP20
4x 51
TP28 /SD_WE
TP29 /SD_CAS
TP30 /SD_RAS
TP31 SD_CS0
TP32 SD_DQS1
TP33 /BS3
TP34 SD_DQS0
TP35 /BS2
DT[31:16]
D[31:16]
TP12TP13TP14TP15TP16TP17TP18TP19
D16 D17 D18 D19 D20 D21 D22 D23
D24 D25 D26 D27 D28 D29 D30 D31
TP20TP21TP22TP23TP24TP25TP26TP27
RP21 4x 22
RP22 4x 22
RP23 4x 22
RP24 4x 22
+2.5V
SD_VREF
U7
MT46V16M16TG-75
SD_DQS[1:0]
/BS[3:2]
/SD_WE
/SD_CAS
/SD_RAS
SD_CS[1:0]
SD_A10
R3 22
R2 22
/BS2
/BS3
SD_CS0
RP25
TP51TP52TP53
CK /CK CKE
/DDR_CLKOUT
DDR_CLKOUT
SD_CKE
RP26
RP27
RP28
RP29
RP30
RP31
A[23:0]
NOTE: please place C59 & C60 close to pin 49 on U7.
VSense
C59 1nF
C60 0.1uF
C61 10uF
C62 1nF
C63 0.1uF
C64 100pF
C65 1nF
C66 0.1uF
C68 100pF
NOTE: please place all resistor packs and resistors as close to U7 as possible. Tracks between the MPU (U6) and the DDR DRAM (U7) must be as near equal length as possible. Preferably within +/-2cm.
SD_A10 TP48
A14 A15 TP49TP50
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A11 A12
TP36TP37TP38TP39TP40TP41TP42TP43TP44TP45TP46TP47
Freescale Semiconductor - TSPG - TECD ColdFire Group
Title
M5275EVB
Size B
Document Number
SDRAM
Rev 1.0
Date: Thursday, July 22, 2004
Sheet 6 of 14



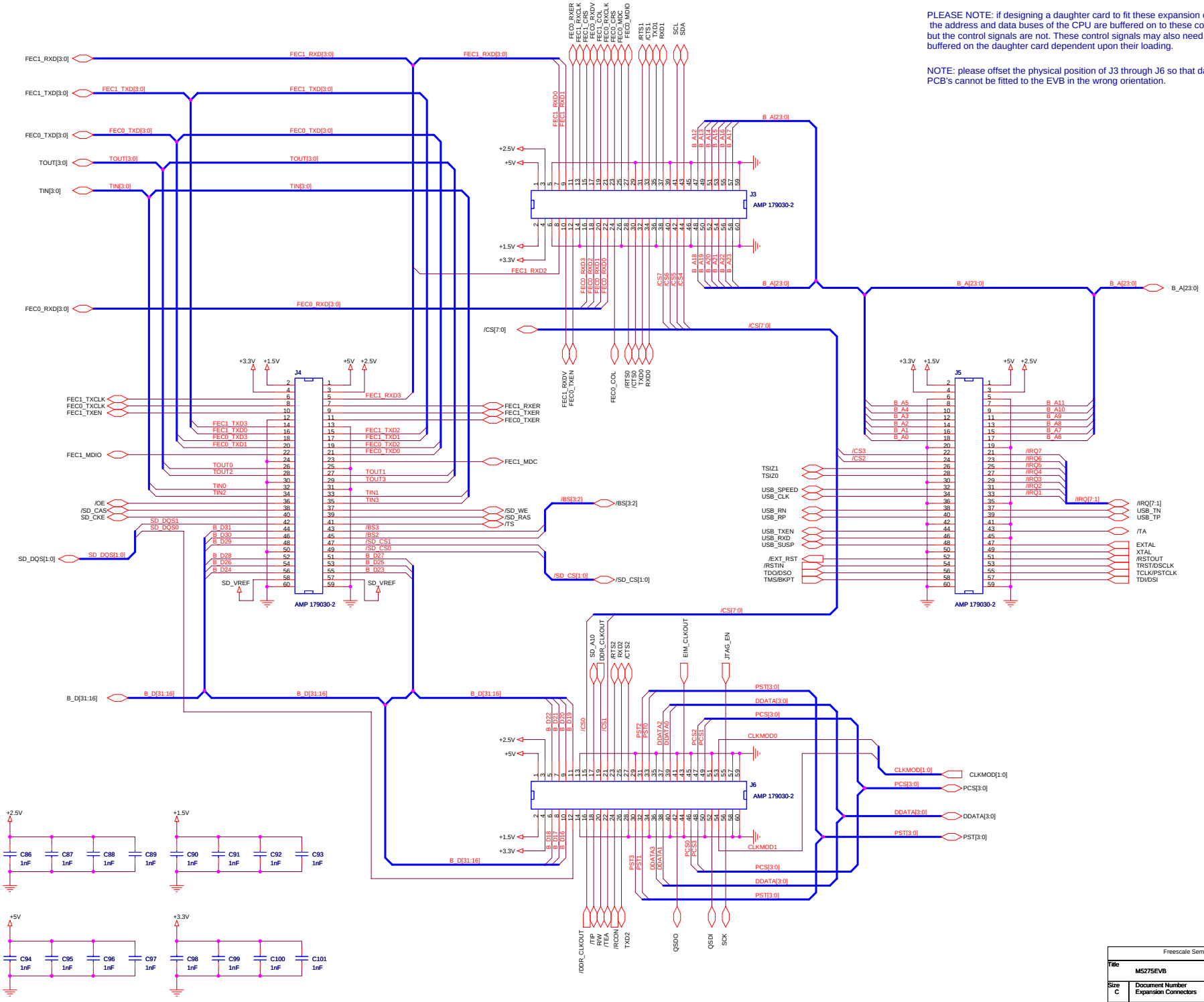
Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title: M5275EVB		
Size: A	Document Number: BDM/JTAG Debug Port	Rev: 1.0
Date: Thursday, July 22, 2004	Sheet 7 of 14	



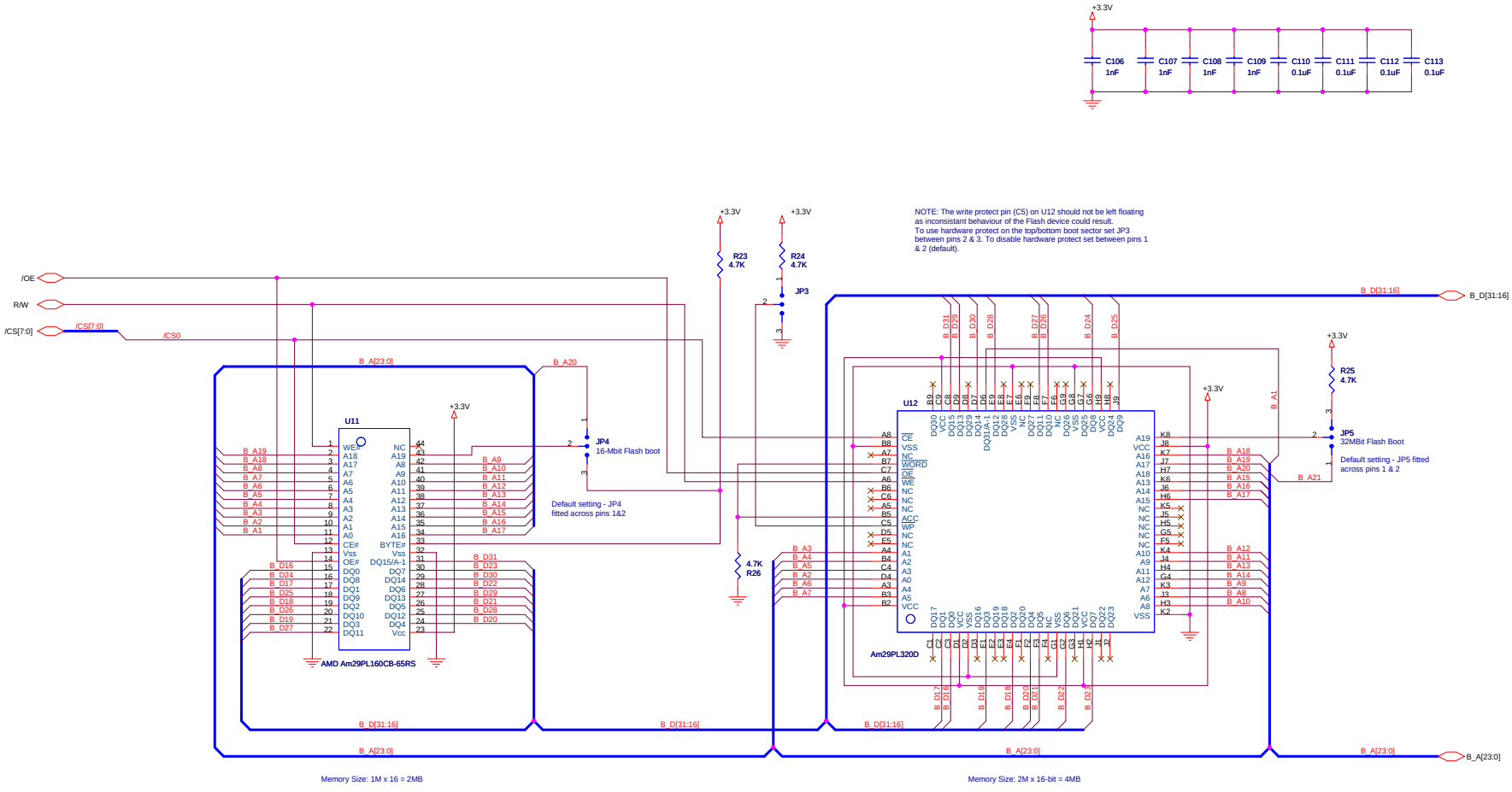
Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title: M5275EVB		
Size: C	Document Number: 10/100BaseT Ethernet Transceiver	Rev: 1.0
Date: Thursday, July 22, 2004	Sheet 8 of 14	

PLEASE NOTE: if designing a daughter card to fit these expansion connectors the address and data buses of the CPU are buffered on to these connectors, but the control signals are not. These control signals may also need to be buffered on the daughter card dependent upon their loading.

NOTE: please offset the physical position of J3 through J6 so that daughtercard PCB's cannot be fitted to the EVB in the wrong orientation.



Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title: M5275EVB		
Size: C	Document Number: Expansion Connectors	Rev: 1.0
Date: Thursday, July 22, 2004	Sheet 9 of 14	


+3.3V
C106 1nF
C107 1nF
C108 1nF
C109 1nF
C110 0.1uF
C111 0.1uF
C112 0.1uF
C113 0.1uF
NOTE: The write protect pin (CS) on U12 should not be left floating as inconsistant behaviour of the Flash device could result. To use hardware protect on the top/bottom boot sector set JP3 between pins 2 & 3. To disable hardware protect set between pins 1 & 2 (default).
/OE
R/W
/CS[7:0]
/CS0
R23 4.7K
R24 4.7K
JP3
B_A[23:0]
B_A20
JP4
16-Mbit Flash boot
Default setting - JP4 fitted across pins 1&2
U11
AMD Am29PL160CB-65RS
B_D[31:16]
R25 4.7K
JP5
32MBit Flash Boot
Default setting - JP5 fitted across pins 1 & 2
U12
Am29PL320D
R26 4.7K
Memory Size: 1M x 16 = 2MB
Memory Size: 2M x 16-bit = 4MB
NOTE: only one of the footprints can/will be populated - BGA (U12) OR SSOP (U11)
Freescale Semiconductor - TSPG - TECD ColdFire Group
Title M5275EVB
Size C
Document Number Flash Memory
Rev 1.0
Date: Thursday, July 22, 2004
Sheet 10 of 14

DC voltage input range +7 to +14V & 1A min.

P1 Power Jack Connector - 2.1mm diameter

Switchcraft RAPC722

POWER SW SLIDE-SPST(Board Edge)

SW3

P2 2-way Bare Wire Power Connector

Augat 25V-02

J7 +12V GND GND +5V

PC disk drive power connector

NOTE: the positive terminal of each power connector must be shown on the silkscreen of the PCB

F1 5A Fast blow.

C119 0.1uF C120 1nF

D10 MBRS340T3 C121 1000uF 35V

3.3V Regulator

U13 LM2596S-3.3 (VIN, VOUT, ~ON/OFF, GND, TAB, FB)

L2 25uH

D7 MBRS340T3 C117 330uF C118 0.1uF

JP6 SHOULD BE INSTALLED DURING ASSEMBLY

JP6 2 PIN JUMPER +3.3VP

R27 270

D8 +3.3V GREEN POWER LED

5.0V Regulator

U14 LM2596S-5 (VIN, VOUT, ~ON/OFF, GND, TAB, FB)

L3 25uH

D11 MBRS340T3 C122 330uF C123 0.1uF

R28 560

D14 +5V GREEN POWER LED

NOTE: SD_VREF = 1.25V
VSense = VTT = termination resistor supply
(Place VSense in the centre of the VTT plane)

U15 LP2995M (NC, GND, VSENSE, VREF, VTT, PVIN, AVIN, VDDQ)

SD_VREF VSense VTT +2.5V

C124 0.1uF C125 330uF C126 330uF C127 47uF

2.5V Regulator

U17 LM2596S-ADJ (VIN, VOUT, ~ON/OFF, GND, TAB, FB)

R30 470 1% R31 15 1% L4 25uH

JP8 SHOULD BE INSTALLED DURING ASSEMBLY

JP8 2 PIN JUMPER +2.5VP

STEWARD HI1206T500R-00 FB1 STEWARD HI1206T500R-00 FB2

+2.5V +2.5VA +2.5VPLL

C131 0.1uF R33 470 1% D17 MBRS340T3 C132 330uF C133 0.1uF

220 R34 D18 +2.5V GREEN POWER LED

C134 0.1uF C135 47uF C136 0.1uF C137 0.1uF C138 1nF C139 47uF

1.5V Regulator

U16 LT1086CM (VIN, ADJ, VOUT)

+5V C129 47uF

R29 120 R32 22

C128 330uF C130 0.1uF

JP7 SHOULD BE INSTALLED DURING ASSEMBLY

JP7 2 PIN JUMPER +1.5VP

R45 10

D16 +1.5V GREEN POWER LED

STEWARD HI1206T500R-00 FB3 Ethernet Ground System Ground

STEWARD HI1206T500R-00 FB4 VSSPLL

VSSPLL - filtered ground for CPU PLL module

NOTE: Diodes prevent excessive difference between 3.3V & 2.5V rails, at power up

+3.3V D5 MRA4003T3 D6 MBRS340T3 +2.5V

NOTE: Schottky Diode prevents excessive difference between 3.3V & 2.5V rails, at power down

+3.3V D9 MBRS340T3 +2.5V

NOTE: Diodes prevent excessive difference between 2.5V & 1.5V rails, at power up

+2.5V D12 MRA4003T3 D13 MRA4003T3 +1.5V

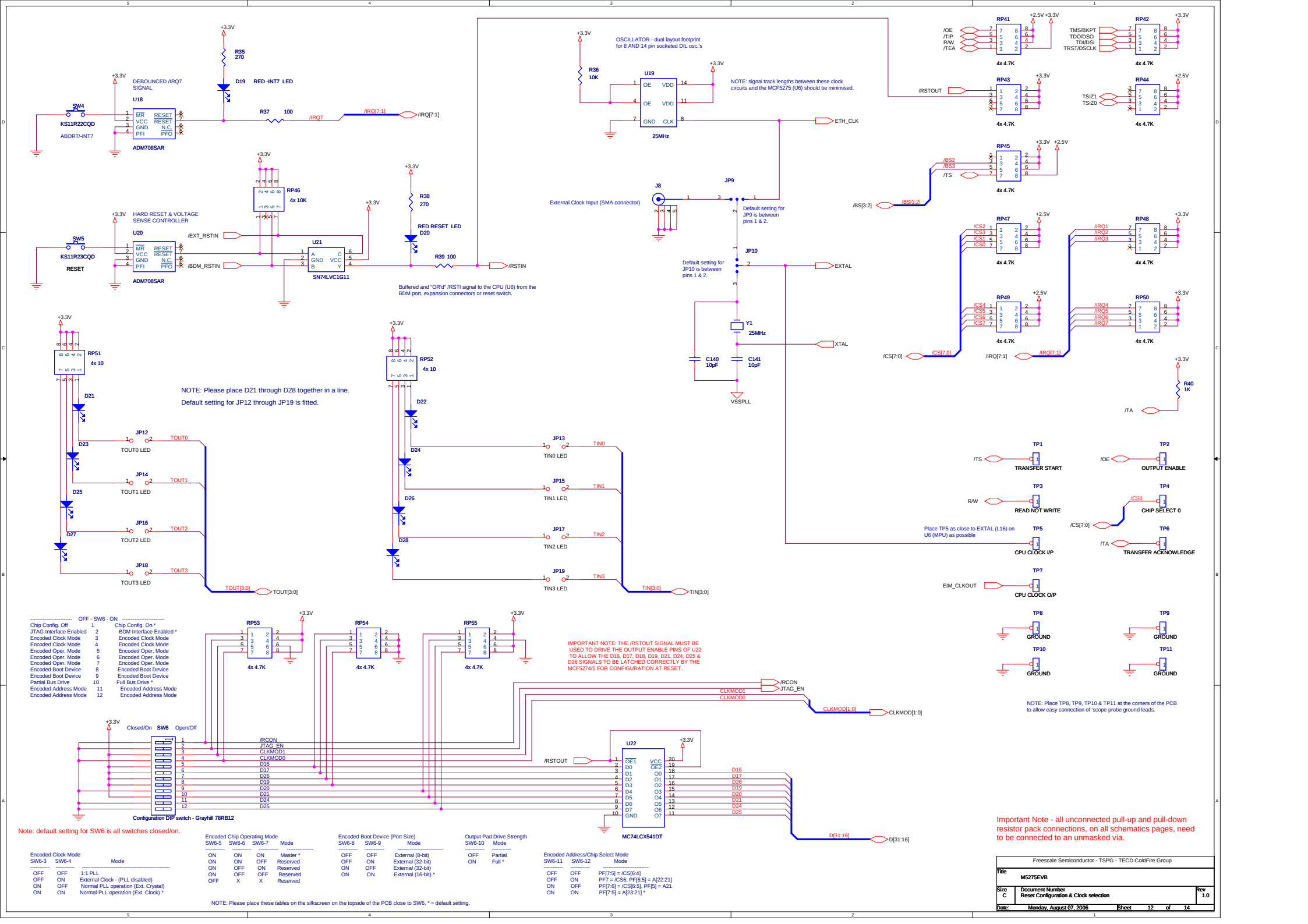
NOTE: Schottky Diode prevents excessive difference between 2.5V & 1.5V rails, at power down

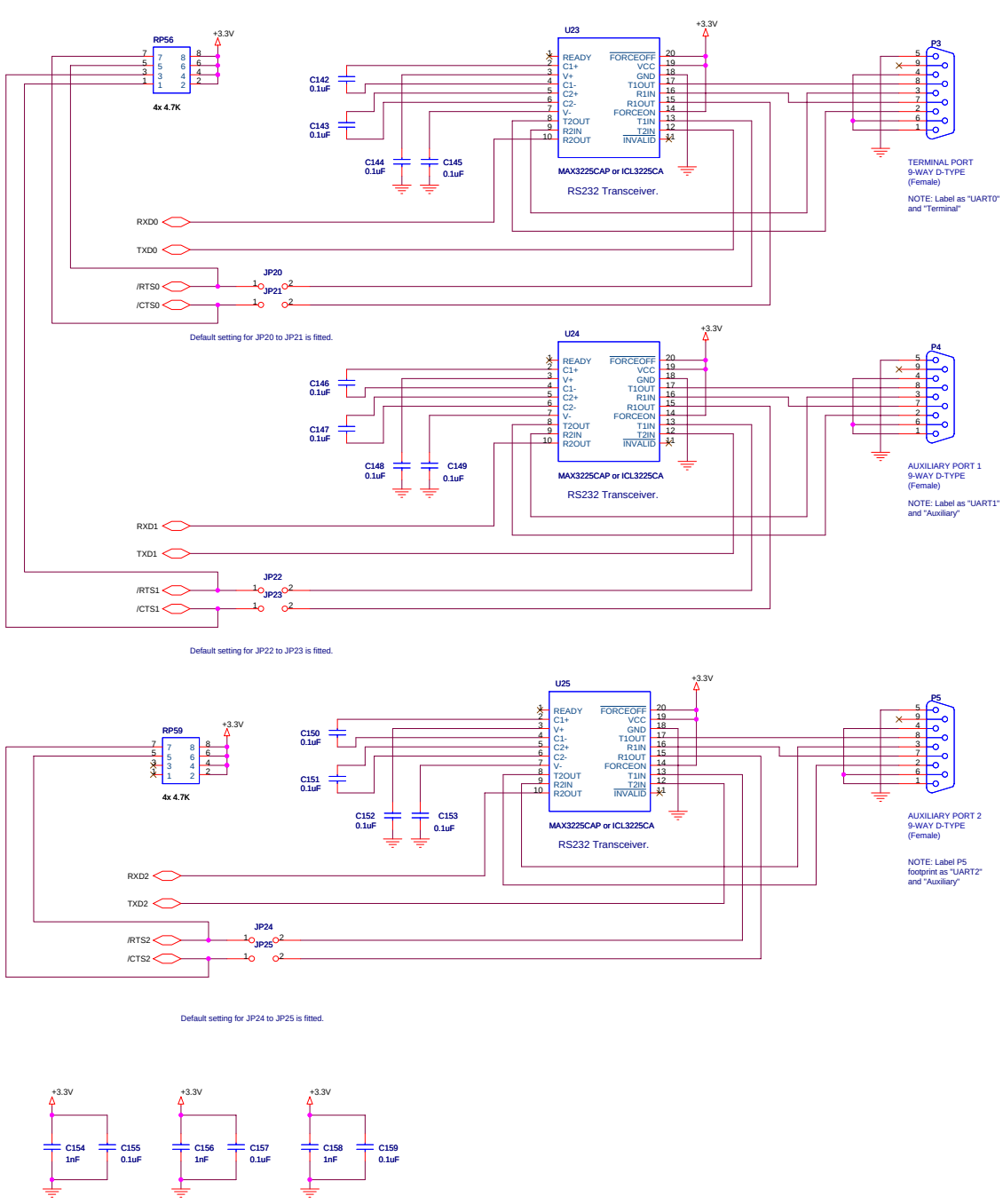
+2.5V D15 MBRS340T3 +1.5V

All resistors are 0805 body size.

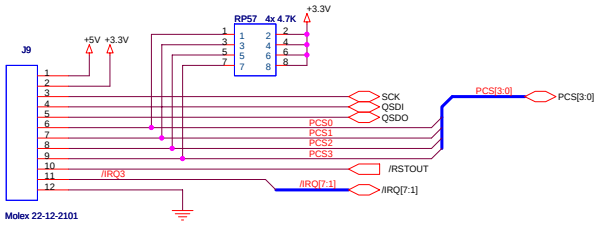
All caps less than 1uF are 0805 body size and COG/NPO dielectric material.

Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title: M5275EVB		
Size: B	Document Number: Power Supply	Rev: 1.0
Date: Thursday, July 22, 2004	Sheet 11 of 14	

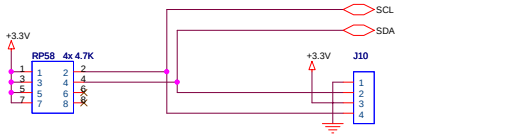

DEBOUNCED /IRQ7 SIGNAL
ABORT/-INT7
HARD RESET & VOLTAGE SENSE CONTROLLER
RESET
OSCILLATOR - dual layout footprint for 8 AND 14 pin socketed DIL osc.'s
NOTE: signal track lengths between these clock circuits and the MCF5275 (U6) should be minimised.
25MHz
External Clock Input (SMA connector)
Default setting for JP9 is between pins 1 & 2.
Default setting for JP10 is between pins 1 & 2.
Buffered and "OR'd" /RSTI signal to the CPU (U6) from the BDM port, expansion connectors or reset switch.
NOTE: Please place D21 through D28 together in a line.
Default setting for JP12 through JP19 is fitted.
IMPORTANT NOTE: THE /RSTOUT SIGNAL MUST BE USED TO DRIVE THE OUTPUT ENABLE PINS OF U22 TO ALLOW THE D16, D17, D18, D19, D21, D24, D25 & D26 SIGNALS TO BE LATCHED CORRECTLY BY THE MCF5274/5 FOR CONFIGURATION AT RESET.
Place TP5 as close to EXTAL (L16) on U6 (MPU) as possible
NOTE: Place TP8, TP9, TP10 & TP11 at the corners of the PCB to allow easy connection of 'scope probe ground leads.
Configuration DIP switch - Grayhill 78RB12
Note: default setting for SW6 is all switches closed/on.
NOTE: Please place these tables on the silkscreen on the topside of the PCB close to SW6, * = default setting.
Important Note - all unconnected pull-up and pull-down resistor pack connections, on all schematics pages, need to be connected to an unmasked via.
Freescale Semiconductor - TSPG - TECD ColdFire Group
M5275EVB
Reset Configuration & Clock selection
Monday, August 07, 2006
Sheet 12 of 14



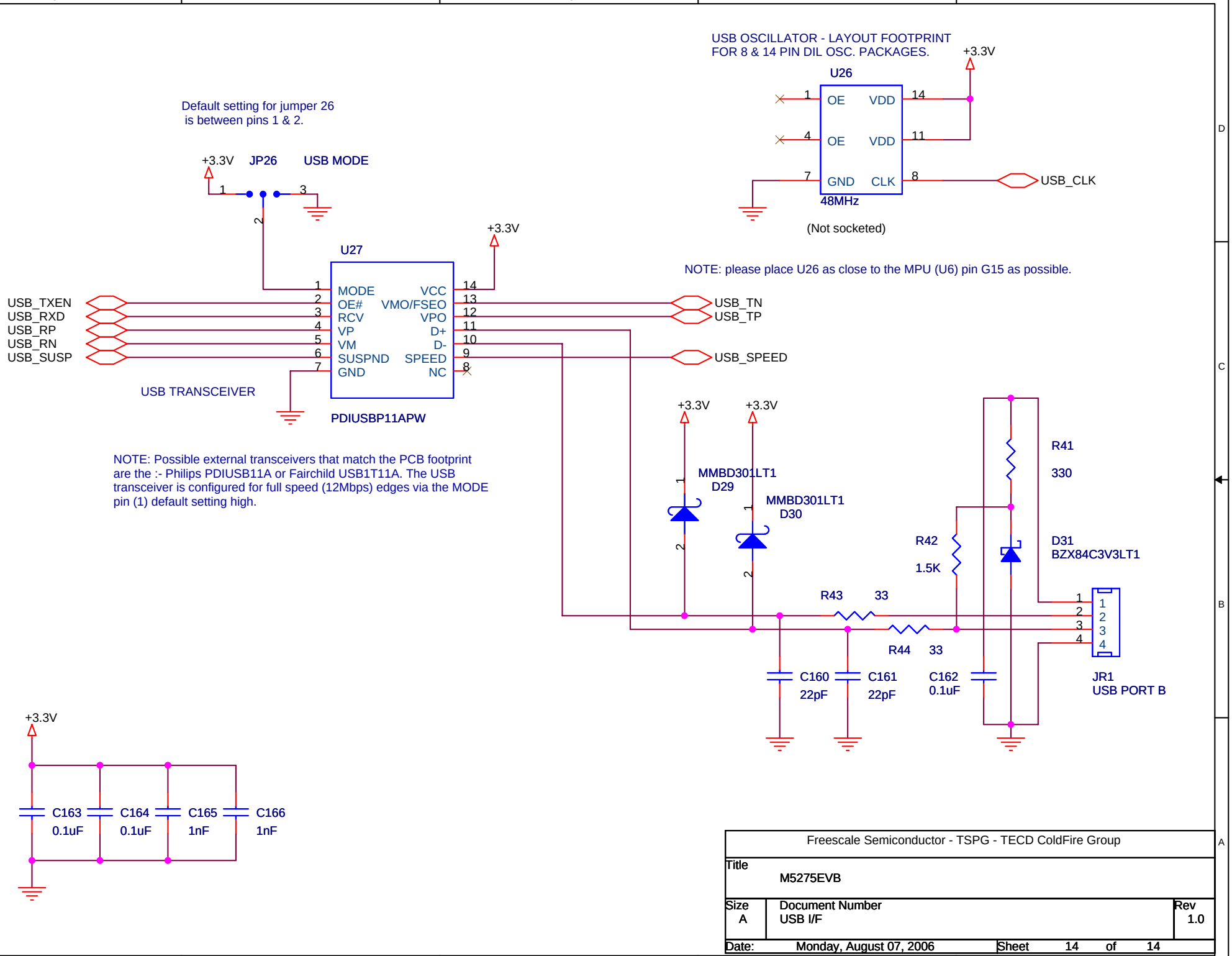
NOTE: J9, the QSPI connector, has additional signals (/RSTOUT & /IRQ3) connected to it to afford a wider range of functionality in any QSPI peripherals connected.



NOTE: the I2C bus on the MCF5275 processor is 3.3V tolerant only. If connection to a 5V system is required high frequency voltage level shifters will be required between the peripheral and processor.



Freescale Semiconductor - TSPG - TECD ColdFire Group		
Title: M5275EVB		
Size: C	Document Number: Serial I/O	Rev: 1.0
Date: Thursday, July 22, 2004	Sheet 13 of 14	


USB OSCILLATOR - LAYOUT FOOTPRINT
FOR 8 & 14 PIN DIL OSC. PACKAGES.
+3.3V
U26
OE
VDD
OE
VDD
GND
CLK
48MHz
USB_CLK
(Not socketed)
Default setting for jumper 26
is between pins 1 & 2.
+3.3V
JP26
USB MODE
U27
MODE
OE#
RCV
VP
VM
SUSPND
GND
VCC
VMO/FSEO
VPO
D+
D-
SPEED
NC
USB_TXEN
USB_RXD
USB_RP
USB_RN
USB_SUSP
USB_TN
USB_TP
USB_SPEED
USB TRANSCEIVER
PDIUSBP11APW
NOTE: please place U26 as close to the MPU (U6) pin G15 as possible.
NOTE: Possible external transceivers that match the PCB footprint
are the :- Philips PDIUSB11A or Fairchild USB1T11A. The USB
transceiver is configured for full speed (12Mbps) edges via the MODE
pin (1) default setting high.
MMBD301LT1
D29
MMBD301LT1
D30
R41
330
R42
1.5K
D31
BZX84C3V3LT1
R43
33
R44
33
C160
22pF
C161
22pF
C162
0.1uF
JR1
USB PORT B
C163
0.1uF
C164
0.1uF
C165
1nF
C166
1nF
Freescale Semiconductor - TSPG - TECD ColdFire Group
Title
M5275EVB
Size
A
Document Number
USB I/F
Rev
1.0
Date:
Monday, August 07, 2006
Sheet
14
of
14