

SECTION 1

M5272TEKC3 DAUGHTERBOARD SPECIFICATION

Revision 1.b, 10/20/00: Edited by Melissa Hunter

Revision 1.a, 09/15/00: Created by John Kelley

1.1 OVERVIEW

This M5272TEKC3 Daughterboard specification document describes the Tektronix Logic Analyzer connector daughterboard being developed for use with the M5272C3 evaluation board via the two expansion connectors. This includes available component information and specifications.

The intent of this document is to outline the requirements of the M5272TEKC3 Daughterboard. Suggestions are encouraged and should be sent to the author (j.kelley@Motorola.com).

1.2 BRIEF SUMMARY

Below is a brief summary of the M5272TEKC3 Daughterboard board specification. More detailed information can be found in following sections.

M5272TEKC3 Daughterboard Configuration:

- Two, 120 pin Surface-Mount Connectors that mate with the M5272C3 expansion connectors
- Five, 38 pin Mictor Connectors that allow connectivity to a Tektronix Logic Analyzer

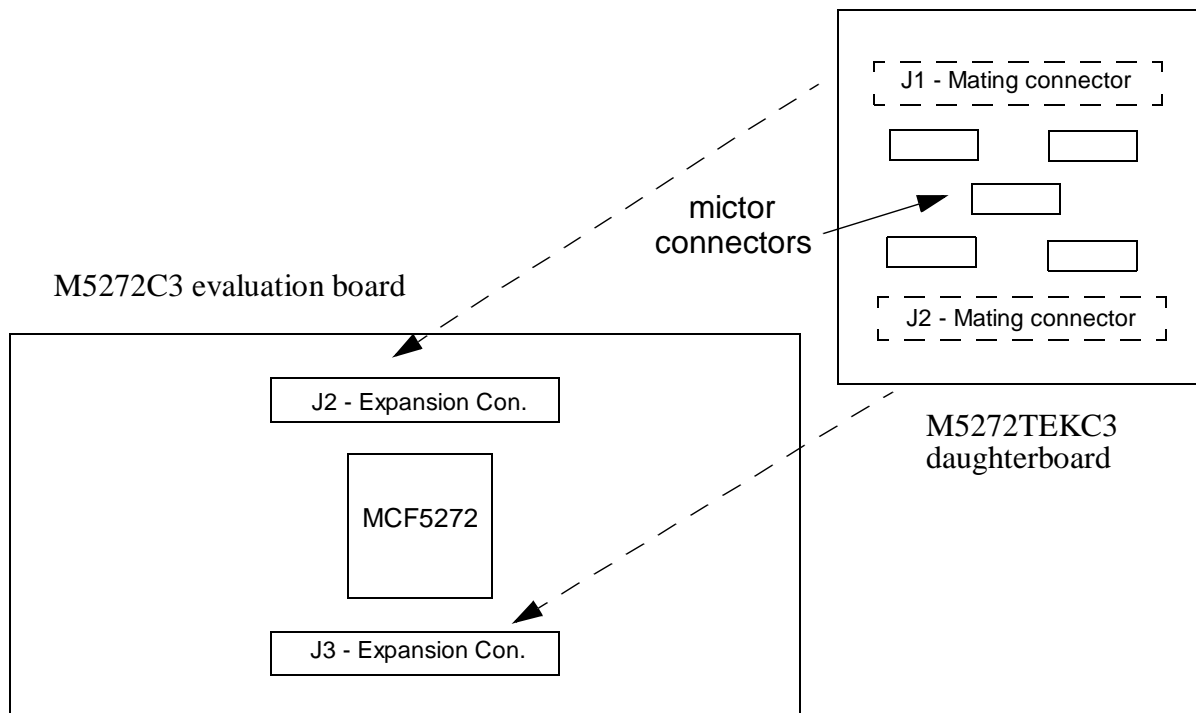


Figure 1. Block diagram view of M5272C3 and daughterboard M5272TEKC3.

Figure 1 shows a view of how the M5272TEKC3 daughterboard will be laid out and how it will connect with the M5272C3 board. The M5272C3 board has two 120 pin expansion connectors located on either side of the MCF5272 Processor as shown. The M5272TEKC3 will have two mating 120 pin connectors on its bottom side. Through these connectors, the M5272TEKC3 daughterboard will connect with the M5272C3 board signals and route them to the five mictor connectors on the top side. These mictor connectors will allow the user to easily access the signals from the M5272C3 board with a logic analyzer.

1.3 HARDWARE/PHYSICAL SPECIFICATION

1. All major components should be thoroughly labeled on the silkscreen.
 - A “dot” next to every 5th pin on a package (except mictors)
 - Pin 1(one) of every device will be labeled
 - All labels will be aligned to 0° or -90° for easy reading
2. The board name, “Motorola ColdFire® M5272TEKC3”, will be clearly visible on the board.
3. Special care should be made to allow all cables, while debugging the board, to be plugged in at the same time without interfering with nearby cables.

1.3.1 Headers/Connectors

In general, the headers/connectors on the M5272TEKC3 Daughter Board should be unique to minimize the potential of the user connecting to an incorrect expansion connection. Where possible, the connectors should be keyed and labeled. Signal loading and transmission effects must be taken in consideration.

1.3.1.1 MICTOR CONNECTORS

Five, 38-pin connectors (Matched Impedance Connectors AMP767054-1) will allow easy access to the M5272C3 board signals by the logic analyzer. We will base the signal assignment grouping on the assignments used by the M5307C3 board. So, for example, the signals that go to the Control mictor on the M5307C3 will also go to the Control mictor M5272C3. However, within the mictors, the signals may be rearranged to aid in layout and routing. Pinouts of the M5307C3 evaluation board may be found at “www.motorola.com/coldfire/”.

1.3.1.2 EXPANSION CONNECTORS

Two, 120-pin expansion connectors (120-way SMT Receptacle expansion connector, AMP179031-5) will provide access to all pins of the microprocessor by connecting with the M5272C3 board’s mating 120-pin expansion connectors (AMP 177983-5). The signals are determined by the existing mating connectors on the M5272C3 board.

(IMPORTANT: Do not ground or otherwise use those pins listed as empty in the below tables because the pin may be connected to a signal or power from the M5272C3 board)

Table 1-1. Expansion Port A Pin Assignment

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	GND	2	GND	61	D17	62	D18
3	CPU_Ext_CLK	4	-RESET	63	D19	64	GND
5	GND	6	-DRESETEN	65	GND	66	D20
7	-BS0	8	-BS1	67	D21	68	D22
9	-BS2	10	-BS3	69	D23	70	GND
11	-OE	12	GND	71	GND	72	D24
13	-CS0	14	-CS1	73	D25	74	D26
15	-CS2	16	-CS3	75	D27	76	GND
17	-CS4	18	-CS5	77	GND	78	D28
19	-CS6	20	GND	79	D29	80	D30
21	DRQ	22	DACK/HIZ	81	D31	82	GND
23	TC/BYPASS	24	GND	83	GND	84	A0
25	A10_PRECHG	26	-WE	85	A1	86	A2
27	SDBA0	28	SDBA1	87	A3	88	GND
29	-RAS0	30	-CAS0	89	GND	90	A4
31	SDCLK	32	-SDWE	91	A5	92	A6
33	SDCLKE	34	-CS7	93	A7	94	GND
35	GND	36	D0	95	GND	96	A8
37	D1	38	D2	97	A9	98	A10
39	D3	40	GND	99	A11	100	GND
41	GND	42	D4	101	GND	102	A12
43	D5	44	D6	103	A13	104	A14
45	D7	46	GND	105	A15	106	GND
47	GND	48	D8	107	GND	108	A16
49	D9	50	D10	109	A17	110	A18
51	D11	52	GND	111	A19	112	GND
53	GND	54	D12	113	GND	114	A20
55	D13	56	D14	115	A21	116	A22
57	D15	58	GND	117	+3.3	118	+3.3
59	GND	60	D16	119	+3.3	120	+3.3

Table 1-2. Expansion Port B Pin Assignment

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	GND	2	GND	61	GND	62	GND
3	DSO	4	DSI	63	USBEXTCLK	64	PB5/-TA
5	GND	6	-BKPT	65	GND	66	GND
7	CPU_CLK	8	DSCLK	67	PB6	68	USBLinH
9	GND	10	-DTEA	69	TIN1	70	USBLinL
11	-TEST	12	MTMOD	71	TOUT1	72	GND
13	GND	14	GND	73	-INT1	74	-INT2
15	DDATA0	16	DDATA1	75	-INT3	76	WSEL
17	DDATA2	18	DDATA3	77	+3.3	78	QSPI_DIN
19	PST0	20	PST1	79	BUSW1	80	BUSW0
21	PST2	22	PST3	81	+3.3	82	PWMOUT1
23	GND	24	GND	83	PWMOUT2/ TOUT2	84	PWMOUT3/ TIN2
25	PA0/USB_TP	26	PA1/USB_RP	85	+3.3	86	+3.3
27	PA3/USB_TN	28	PA2/USB_RN	87	ETXCLK	88	ETXD0
29	PA4/ USB_SUSP	30	PA5/ USB_TXEN	89	ECOL	90	ERXDV
31	PA6/USBRXD	32	-RSTO	91	ERXCLK	92	ERXD0
33	GND	34	GND	93	ETXEN	94	ETXD3
35	FSC0/FSR0	36	DGNT0	95	GND	96	GND
37	DCL0/ USRT2CLK	38	DIN0/ USRT2RXD	97	ETXD2	98	ETXD1
39	USRT2CTS/ SPI-CS2	40	USRT2RTS/ INT5	99	-CS6_RD	100	-CS5_RD
41	DOUT0/ USRT2TXD	42	DREQ0	101	ERXD3	102	ERXD2
43	SPI-CS1	44	GND	103	GND	104	GND
45	GND	46	DFSC2	105	ERXD1	106	ERXERR
47	DFSC3	48	FSC1-FSR1/ DFCS1	107	-CS6_WR	108	-CS5_WR
49	DCL1/ GEN_DCL_OUT	50	DREQ1	109	EMDC	110	EMDIO
51	DGNT1/-INT6	52	DOUT1	111	GND	112	GND
53	DIN1	54	SPI-CS3/ DOUT3	113	ETXERR	114	ECRS
55	DIN3/-INT4	56	USRT1TXD	115	+5	116	+5
57	USRT1RXD	58	USRT1CTS	117	+5	118	+5
59	USRT1RTS	60	USRT1CLK	119	+3.3	120	+3.3

1.3.2 Test Points

Test points will be installed for GND, +3.3V (+3.3 VDC), and +5V (+5 VDC).

1.3.3 Connection LEDs

Two green LEDs will be installed. One for the +3.3V signal on J1 and one for the +5V signal on J2. These LEDs will be on anytime the M5272TEKC3 is connected to the M5272C3 board, or to be precise, the LEDs will be on when the board is connected to the +3.3V, +5V and GND supplies.

1.3.4 Signal Noise Interference

Signal noise should be minimized to meet the requirements of this application, by implementing best layout design methodologies.

1.4 SPECIFICATION FEEDBACK

Once again, we are looking for suggestions and improvements to this board. Please send feedback to John Kelley at j.kelley@Motorola.com.