JN-RM-2080

K32W Hardware Design User Guide

Rev. 1.2 — 03 January 2022 User Guide

Contents

1 Introduction

This document describes the hardware design guidelines for reference designs that use NXP K32W061/41 wireless microcontroller. The K32W061/41 MCU is an ultra-low-power, high-performance, single-chip device that enables IEEE 802.15.4 standard and BLE 5.0 RF connectivity for portable and extremely low-power embedded systems.

The K32W061/41 SoC integrates a radio transceiver operating in the 2.4 GHz ISM band, supporting IEEE 802.15.4 / BLE 5.0 radio, an Arm® Cortex®-M4 processor, with 640 KB flash, even up to 1 MB flash on K32W041AM, 152 KB SRAM (and 128 KB ROM), BLE Link layer processing hardware, and peripherals optimized to meet the requirements of the target applications.

For application prototyping and demonstration of the K32W061/41 MCU, NXP provides its own K32W MCU based reference designs, which are small, low-power, and cost-effective evaluation and development boards.

This document covers the following K32W061/41-based reference designs from NXP:

- K32W-001-T10
- K32W-001-T16
- K32WA-001-T10
- K32WAM-001-T10

These reference designs are described in Table 1.

To complete a successful PCB design based on a K32W MCU, you should follow, as strictly as possible, the hardware design guidelines described in this document. For details on the K32W characteristics, see *K32W061/K32W041 Data Sheet* and *K32W041A/K32W041AM Data Sheet*.

The design considerations presented in this document are equally valid for bespoke solutions where the K32W061/41 device is placed directly onto the product PCB.

1.1 Regulatory approvals

The K32W-001-T10 reference design is compliant with:

- Radio Equipment Directive (RED) 2014/53/UE
- ETSI EN 300 328 V2.1.1, EN 301 489-1 V2.1.1, EN 301 489-3 V2.1.1, EN 301 489-17 V3.1.1
- Basic Safety Assessment (BSA) EN 60950-1:2006 (2006-06)
- CFR 47 FCC part 15
- Industry Canada Compliance statement

The K32W-001-T10 reference design is subject to a Notified Body Opinion.

The high-power K32W-001-T16 reference design is not approved for use in Europe. It is compliant for IEEE 802.15.4 with:

- CFR 47 FCC part 15

- Industry Canada Compliance statement

2 Reference designs

The table below provides details of the K32W061/41-based reference designs covered in this document. A complete manufacturing package with design files of these reference designs and other related modules is available for download at the following page on NXP website:

https://www.nxp.com/products/wireless/multiprotocol-mcus/k32w061-41-high-performance-secure-and-ultra-low-power-mcu-for-zigbeethread-and-bluetooth-le-5-0-with-built-in-nfc-option:K32W061_41?tab=Design_Tools_Tab

To download the package, click the above link to open the K32W061/41 **TOOLS & SOFTWARE** page, go to **Tools and Software > NXP > Design Tools & Files > Design Files - miscellaneous**, and download **K32W061 Manufacturing package** (JN-RD-6059_K32W061).

Table 1. Reference designs

Reference design	Description
K32W-001-T10 (OM15069)	K32W061 standard-power board with PCB antenna or µFL connector support
K32W-001-T16 (OM15072)	K32W061 high-power antenna diversity board with PCB antenna and µFL connector support
K32WA-001-T10	K32W041A board with PCB antenna and µFL connector support
K32WAM-001-T10	K32W041AM board with PCB antenna and µFL connector support

NOTE

These reference designs are approved for the operating temperature range of -40 ºC to +125 ºC.

The K32W061 manufacturing package (JN-RD-6059) includes the following design files of each of the above reference design packages, along with a copy of the current document (JN-RM-2080):

- Schematics
- Layout
- Bill of materials (BOM)

3 Block diagrams

The figure below shows the block diagrams of the K32W061/41A/41AM-based reference designs.

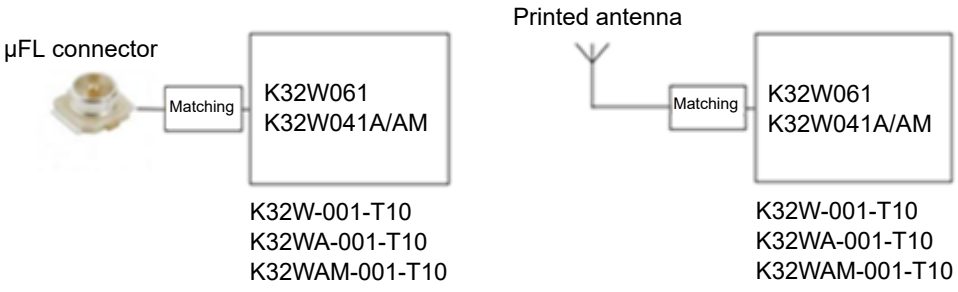


Figure 1. K32W-001-T10/K32WA-001-T10/K32WAM-001-T10 block diagrams

The figure below shows the K32W-001-T16 block diagram.

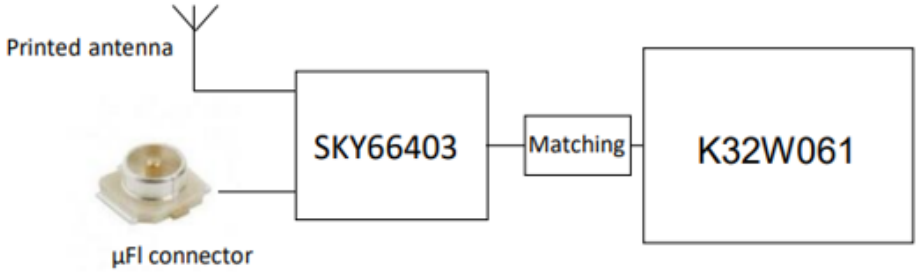


Figure 2. K32W-001-T16 block diagram

4 Design considerations

To develop wireless hardware successfully, the proper device footprint, RF layout, circuit matching, antenna design, and RF measurement capability are essential. RF circuit design, layout, and antenna design are specialties requiring investment in tools and experience. With available hardware reference designs from NXP, RF design considerations, and the guidelines contained in this document, hardware engineers can successfully design IEEE 802.15.4 radio boards with good performance levels. The following figures show the K32W reference designs, which contain the K32W device and all necessary I/O connections.

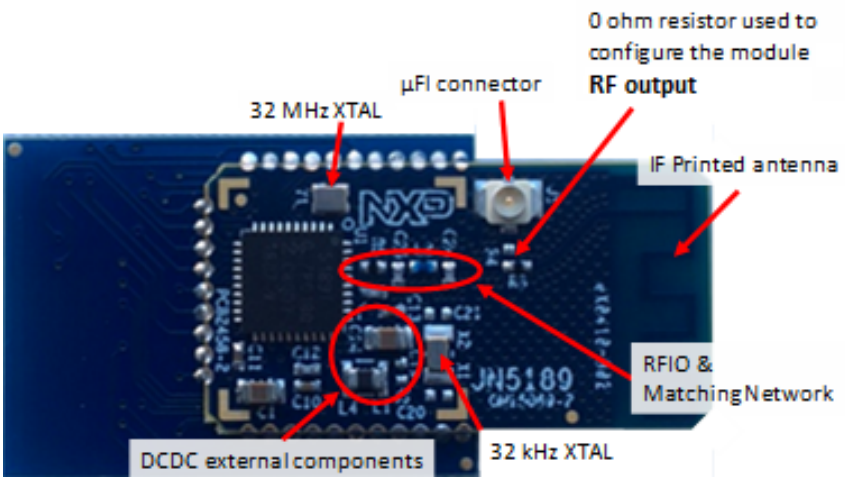


Figure 3. K32W-001-T10 reference design

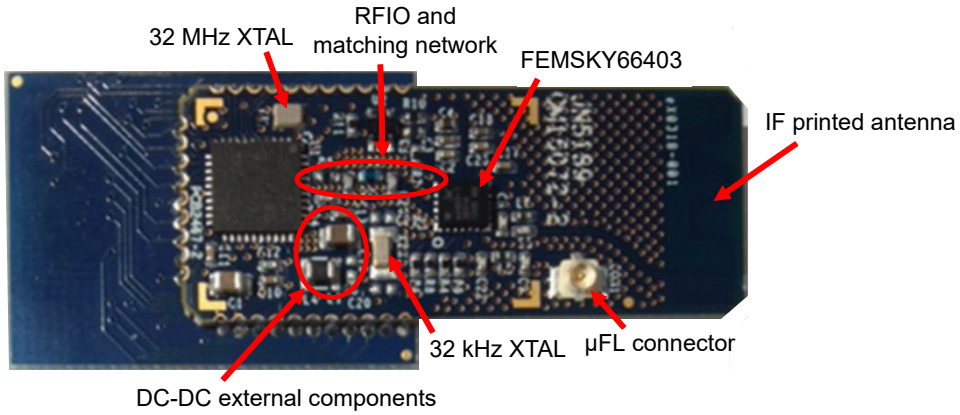


Figure 4. K32W-001-T16 reference design

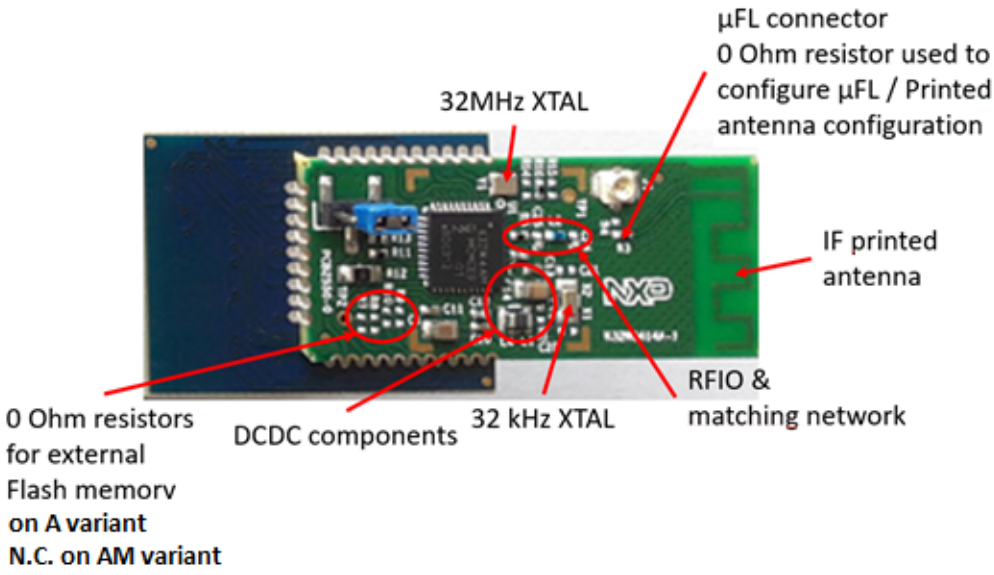


Figure 5. K32WA-001-T10/K32WAM-001-T10 reference design

The device footprint and layout are critical, and the design implementation impacts the RF performance. For these reasons, use of the NXP recommended RF hardware reference designs are important for successful board performance. Additionally, the reference platforms have been optimized for radio performance. Even small changes in the location of components can mistune the circuit. If the recommended footprint and design are followed exactly in the RF region of the board, then sensitivity, output power, harmonic and spurious radiation, and range are likely to deliver first-time success.

The following subsections describe important considerations when implementing a wireless hardware design, starting with the device footprint, PCB stack-up, RF circuit implementation, and antenna selection. Figure 6 shows an example of a typical layout with the critical RF section that must be copied exactly for optimal radio performance. The less critical layout area can be modified without reducing radio performance.

NOTE

You can find exact layout dimensions in the layout files included in the manufacturing package for K32W-based reference designs.

4.1 Schematics design

The devices in the K32W device family has the same footprint. The schematics based on different K32W devices also look very similar. As compared to K32W061-based schematics, the DC-DC inductor for K32W041A/AM-based schematics is 2.2 µH, instead of 4.7 µH.

Because K32W041 variant has no NTAG; therefore, pins 39 and 40 should be kept as N.C. for K32W041A. For K32W041AM, pin 40 is used for internal EEPROM flash reset; a pull-up resistor of 100 kΩ is connected to avoid flash reset.

Also for K32W041AM, PIO16, PIO18, PIO19, and PIO21 are internally connected to drive the embedded EEPROM; therefore, they are not available for external connections.

PIO20 on K32W041AM can still be used as the input for analog comparator (compare with the internal reference). See SDK driver example for details. This pin is not connected on the K32W041AM MCU. For this purpose, a 0 Ω resistor should be soldered.

4.2 K32W device footprint

The performance of the wireless link largely depends on the footprint of the device. Therefore, a footprint has been created carefully in such as manner that receiver sensitivity and output power are optimized to enable board matching and minimal component count. NXP strongly recommends creating die flag (including via locations) exactly same as shown in the figure below. Deviation from these parameters can cause performance degradation.

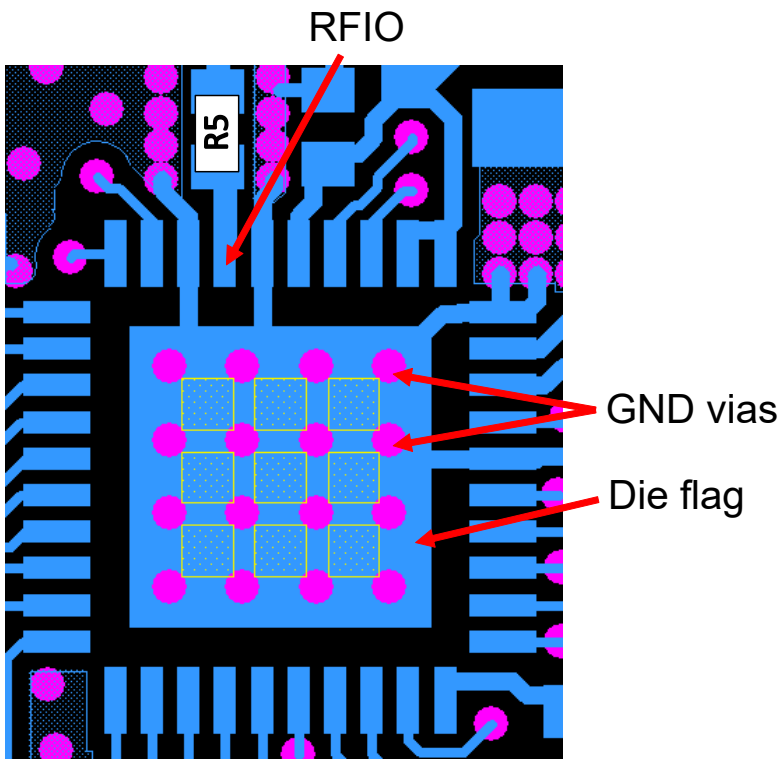


Figure 6. Critical layout of die flag area

The figure above shows the critical areas of the device die flag; these areas are given below:

- Ground vias and locations
- RF output and ground traces
- Die flag shape

4.3 PCB stack-up

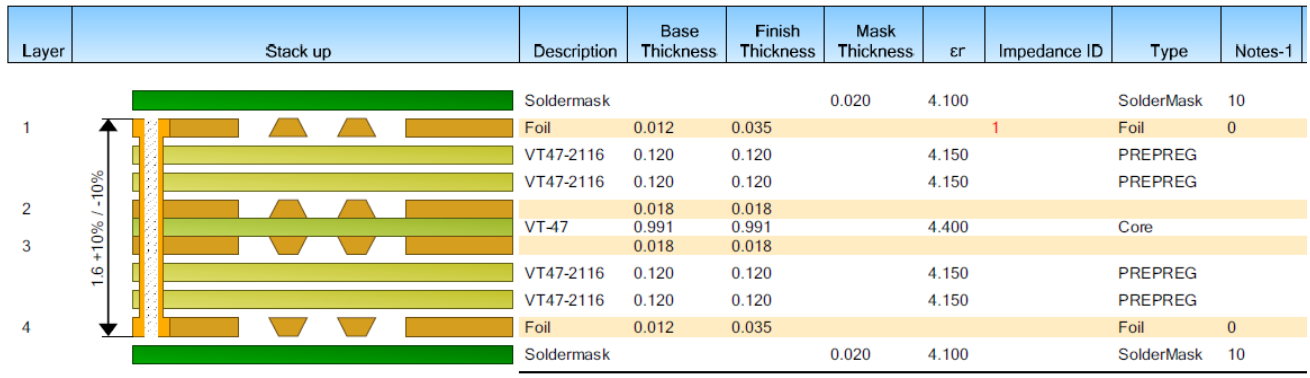
Complexity is the main factor that determines whether an application board should be designed as a two-layer board, four-layer board, or a board with more layers. From an RF point of view, a four-layer PCB is preferred to a two-layer PCB. Nevertheless, in a very simple application, designing a two-layer PCB should be possible.

The table below shows recommended four-layer and two-layer PCB stack-ups.

Table 2. PCB stack-ups

Four-layer PCB stack-up	Two-layer PCB stack-up
• Top: RF routing of transmission lines • L2: RF reference ground • L3: DC power • Bottom: Signal routing	• Top: RF routing of transmission lines, signals, and ground • Bottom: RF reference ground, signal routing, and general ground

The K32W-001-T10 (OM15069), K32W-001-T16 (OM15072), and K32W041A/AM-based reference designs are built on a standard four-layer PCB with the individual layers organized as shown in the figure below.



Layer	Stack up	Description	Base Thickness	Finish Thickness	Mask Thickness	εr	Impedance ID	Type	Notes-1
		Soldermask			0.020	4.100		SolderMask	10
1		Foil	0.012	0.035			1	Foil	0
		VT47-2116	0.120	0.120		4.150		PREPREG	
		VT47-2116	0.120	0.120		4.150		PREPREG	
2			0.018	0.018					
		VT-47	0.991	0.991		4.400		Core	
3			0.018	0.018					
		VT47-2116	0.120	0.120		4.150		PREPREG	
		VT47-2116	0.120	0.120		4.150		PREPREG	
4		Foil	0.012	0.035				Foil	0
		Soldermask			0.020	4.100		SolderMask	10

Figure 7. PCB stack-up

NOTE

NXP strongly recommends creating PCB layouts based on the layers defined above. If a different PCB stack-up is used, then NXP cannot guarantee performance.

Replicating PCB stack-up shown in the figure above, apart from replicating physical layout of the circuit, is also important from transmission line perspective. Any small change in the thickness of the dielectric substrate under the transmission line may change the impedance significantly; all this information can be found in the fabrication notes for each board design. For example, consider a 50 Ω microstrip trace that is 18 mils wide over 10 mils of FR4. If the thickness of FR4 is changed from 10 mils to 6 mils, then the impedance will only be about 36 Ω.

In any case, the width of the RF lines must be recalculated according to the PCB characteristics to ensure a 50 Ω characteristic impedance.

When the top-layer dielectric becomes too thin, the layers do not act as a true transmission line, even though all the dimensions are correct. There is no universal industry agreement at what thickness this happens, but NXP prefers to use a top-layer dielectric thickness of no less than 8-10 mils.

PCB fabricators are limited in their ability to control minimum width of a PCB trace and minimum thickness of a dielectric layer. A change of ±1 mil has less impact on an 18-mil-wide trace and a 10-mil-thick dielectric layer, than it has on a much narrower trace and thinner top layer.

This problem can particularly be an insidious problem. The design may appear to be optimized with the manufacturing of limited number of prototype and initial production boards, in which all the bare PCBs were fabricated in the same lot. However, variations in PCB fabrication from one lot to another may lead to degraded performance in mass production boards.

Using a correct substrate, such as the FR4 with a dielectric constant of 4.4 helps in achieving a good RF design.

Although no special measures are required for board design, NXP still recommends you to use Class 1 tolerances.

4.4 RF circuit topology and matching

NXP always recommends that designers start by copying the existing NXP reference design. This applies to both the circuit portion (schematic) of the design, and the PCB layout. For all RF designs, particularly for designs at frequencies as high as 2.4 GHz, the PCB traces are a part of the design itself. Even a very short trace has a small amount of parasitic impedance (usually inductive), which has to be compensated for in the remainder of the circuit.

What may seem like a minor change to the layout, or what would certainly be a minor change at a lower frequency of operation, can actually be a significant change at 2.4 GHz frequency. For example, a metal trace on a PCB (such as K32W-001-T10) has a parasitic impedance of 0.8 nH per mm. This may have no impact at lower frequencies, but at the 2.4 GHz frequency, this will cause a significant impact in any matching circuit.

NXP tunes and optimizes the circuits used on its reference designs according to the actual layouts of the reference design. It finalizes component values by considering the circuit board trace effects and other parasitic effects introduced by the PCB; such as parasitic capacitance between components, traces, and/or board copper layers; inductance of traces and ground vias; the non-ideal effects of components; and nearby physical objects.

The layout of the RF portion of a K32W-based design is critical. You should strictly follow the layout of the RF portion in the corresponding NXP reference design; otherwise, you may encounter the following issues:

- Reduction in RF output
- Excessive spurious RF outputs leading to RF compliance issues
- Unacceptable power slope across the full channel range
- Poor range
- Reduced Rx sensitivity

4.5 Transmission lines

Transmission lines have several shapes, such as microstrip, coplanar waveguide (CPW), and strip-line. For IEEE 802.15.4 applications built on FR4 substrates, the types of transmission lines typically take the form of microstrip or coplanar waveguide. These two structures are defined by the dielectric constant of the board material, trace width, and the board thickness between the trace and the ground.

Additionally, for CPW, the transmission line is defined by the gap between the trace and the top-edge ground plane. These parameters are used to define the characteristic impedance of the transmission line (trace) that is used to convey the RF energy between the radio and the antenna.

K32W has a single-ended RF output with a three-component matching network, composed of two shunt capacitors and one series inductor, which is placed between the shunt capacitors. In addition, a 0 Ω resistor has been placed between the RFIO port of the chip and the first shunt capacitor. These components transform the device impedance to 50 Ω. Depending on the board layout, the values of these components may vary. The recommended RF matching network is shown in the figure below.

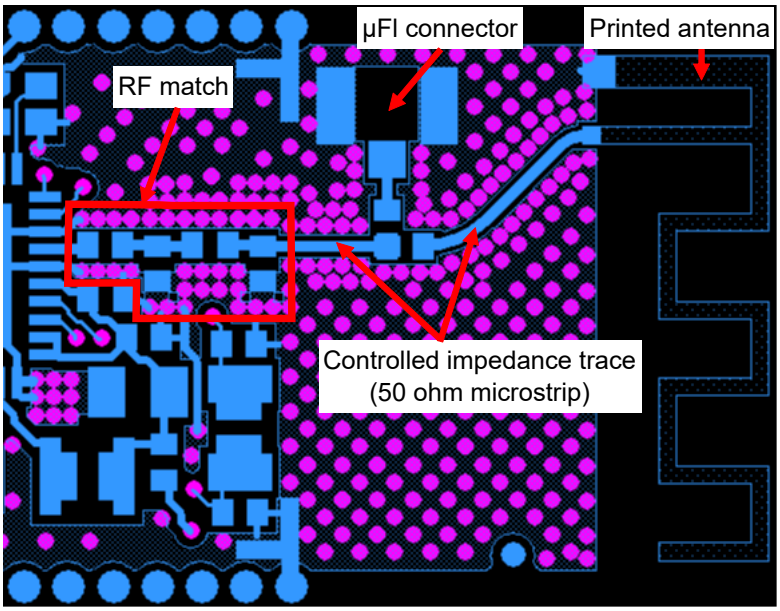


Figure 8. RF matching network

Avoid routing traces near or parallel to RF transmission lines or reference crystal signals. Maintaining a continuous ground under an RF trace is critical to maintaining the characteristic impedance of the trace. Avoid any routing on the ground layer that may result in disrupting the ground under the RF traces. Keep the RF trace as short as possible.

4.6 Components

All electronic components have parasitic characteristics. This causes a component (part) to act in a non-ideal way. Typically, these effects become worse as the frequency of operation is increased. Most component suppliers indicate this quality through self-resonant frequency (SRF) specification.

For example, a capacitor has parasitic inductance introduced by the metal leads of the components. As frequency increases, at some point, the impedance due to the parasitic inductance is greater than the impedance of the capacitor. At this frequency, the component no longer acts as a capacitor and starts acting as an inductor. At the point where the impedance from both inductive and capacitive components is same, the part resonates as an LC parallel resonant circuit. This frequency is known as self-resonant frequency. The figure below shows a typical frequency response curve.

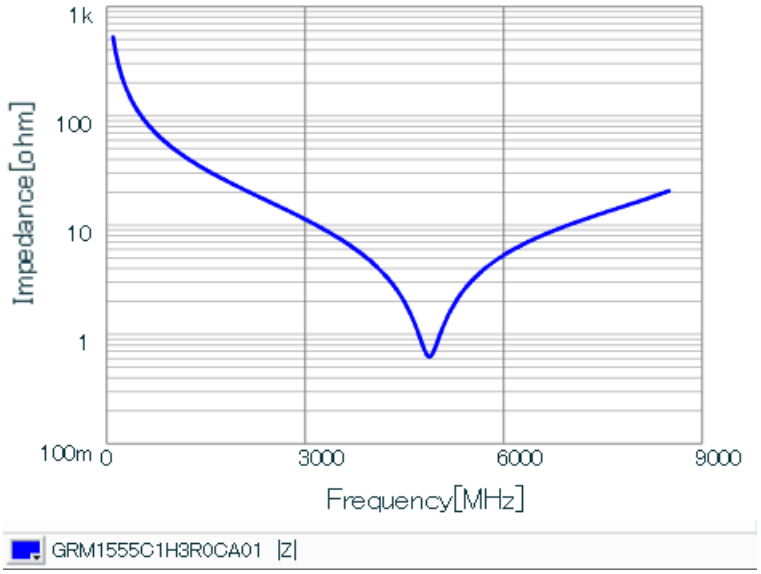


Figure 9. RF plot for 3 pF ceramic capacitor of Murata GRM1555 type

The same concept also applies to inductors. An inductor has parasitic capacitance, mainly due to the capacitive coupling between the turns of wire. As frequency increases, at some point, this capacitance has a higher impedance than the inductance of the part. Starting from this frequency, the part acts as a capacitor and not as an inductor.

The bill of materials (BOM) is available for all NXP reference designs. The BOM of a reference design shows the vendors and part numbers used in the design. Substituting a part with a part from a different vendor is possible, but it may impact the performance of the circuit. To avoid performance impact, you may need to use different component values when parts from different vendors are used.

If you face performance issues on a new design where you had substituted parts, then you are advised to place components, identical to those that are used in the NXP reference design, on the new design for testing purposes. After the design starts working correctly with components that are identical to those used by NXP, you can begin substituting components with components from other vendors, one at a time, and test the impact on circuit performance.

4.7 GND planes

You are recommended to use a solid (continuous) ground plane on Layer 2, assuming Layer 1 (top) is used for the RF components and transmission lines; avoid cut-outs or slots in that area.

Keep top ground continuous, as much as possible. This applies to other layers as well.

Connect ground on the component layer to the ground plane beneath with a large quantity of vias.

Ground pours or fingers can act as antennas that perform radiation, which is undesired. To avoid this undesired radiation, eliminate any finger that is not connected to the ground reference with a via; put a via in any trace that does not go anywhere.

4.8 Layer connections

Avoid vias in the RF traces. Typically, for a 1.6 mm thickness PCB material, a single via can add 1.2 nH of inductance and 0.5 pF of capacitance, depending on the via dimensions and PCB dielectric material.

Provide multiple vias for high-current and/or low-impedance traces.

Carefully connect all the ground areas of any layer to the reference GND plane.

4.9 DC-DC components

Ensure that the smallest value capacitors C12 and C10 are placed close to the VBAT pin.

The impedance of the GND connection between C10/C12 and C19 must be as low as possible — connect them directly on the component layer (see the red path in the figure below).

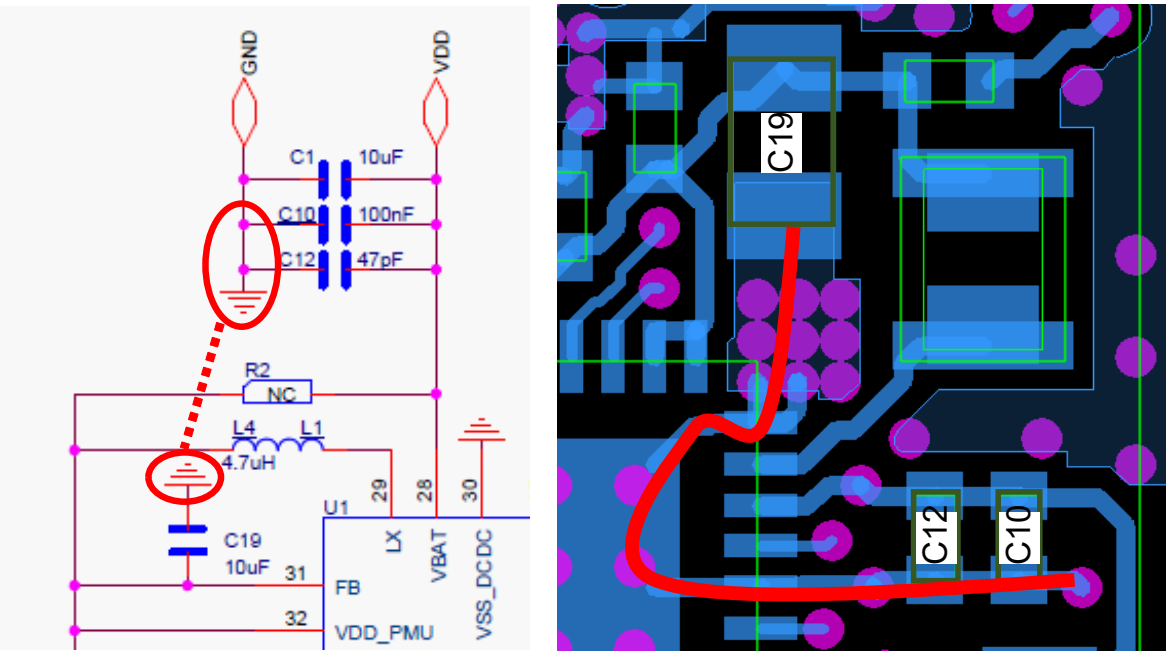


Figure 10. GND path between C10/C12 and C19

4.10 Reference crystal

The NXP K32W device contains the necessary on-chip components to build a 32 MHz reference crystal oscillator by adding an external reference crystal. There is no need to use external capacitors as the K32W device includes a bank of switchable capacitors that can be tuned to adjust the load capacitance (C_L) requirement of the reference crystal.

The reference crystal serves many purposes, for example, it provides a reference for the 32-bit Arm processor, PHY controller, radio synthesizer, and analog peripherals. It also provides timing references for external inputs/outputs (such as on-chip UARTs) and timer counters. Therefore, specifying crystal references correctly is important in ensuring that the system functions properly.

While selecting a reference crystal, you should consider the following points:

- Reference crystal tolerance: A number of parameters, ranging from on-chip timings to radio center-frequency, are derived directly from the tolerance of the reference crystal. NXP recommends you to use a total tolerance of less than ±25 ppm, as the maximum permissible offset specified in IEEE 802.15.4 is ±40 ppm. Also note that this tolerance should include both temperature effects and aging effects happened on the reference crystal.
- Reference crystal load capacitance: The active oscillator components on the K32W devices are designed for a reference crystal with load capacitance (C_L) of 6 pF. This is a standard load and this type of oscillators are widely available.

Layout recommendations

Route the connections from the 32 MHz reference crystal to the chip oscillator pins with traces as short as possible. The layout of the oscillator circuit is designed in such a way that tracks between components are as short as possible. It improves the performance of the oscillator by reducing stray capacitance that can introduce frequency errors.

The reference crystal should be placed away from high-frequency devices and traces to reduce the capacitive coupling between crystal pins and PCB traces.

Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far as possible from the crystal connections.

CAUTION

To ensure correct operation of your design, you should adhere to the guidelines mentioned in this document. You are recommended not to substitute components, as this may lead to both oscillator startup and frequency tolerance issues.

4.11 Decoupling

4.11.1 General considerations

Decouple the power supplies or regulated voltages as close as possible to the supply pin of the chip. The decoupling capacitors must be connected to a localized ground pad on the top layer, which is connected to the main ground plane layer through multiple vias.

Ensure that each decoupling capacitor has its own via connection to the ground. If possible, use two vias to connect a capacitor to the ground layer, as shown in the figure below.

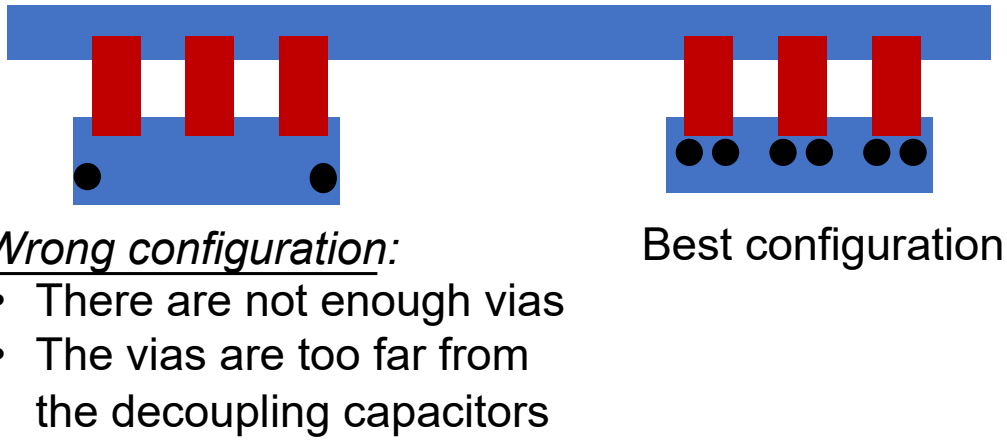


Figure 11. Placement of GND vias

Decoupling capacitors with smaller capacitance values must be placed nearer to the chip. A decoupling capacitor must be placed between the main supply line and the supply pin, as shown in the figure below.

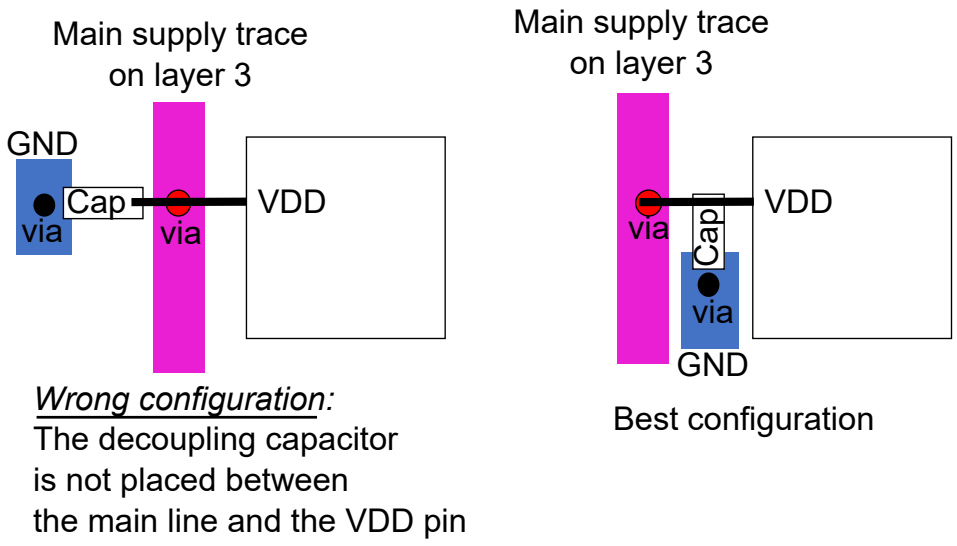


Figure 12. Decoupling capacitor placement

4.11.2 VDD (radio), FB, VDD_PMU, VDDE, and VBAT decoupling

The figures below show the recommended placement of the decoupling capacitors for the VDD (radio), FB, VDD_PMU, VDDE, and VBAT supplies. For your own reference design, you should replicate the capacitor placement from these figures, as closely as possible.

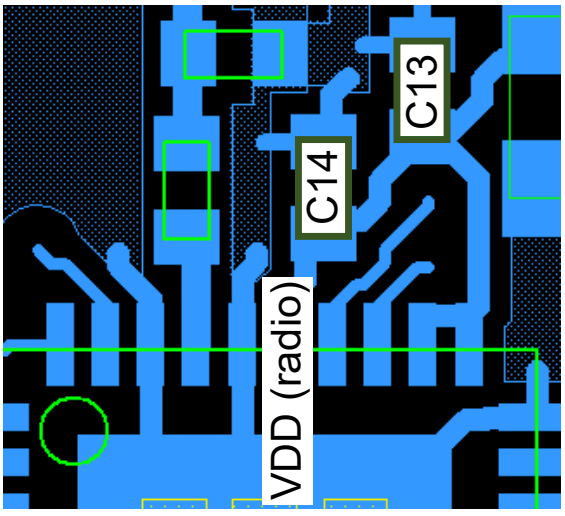


Figure 13. VDD (radio) decoupling

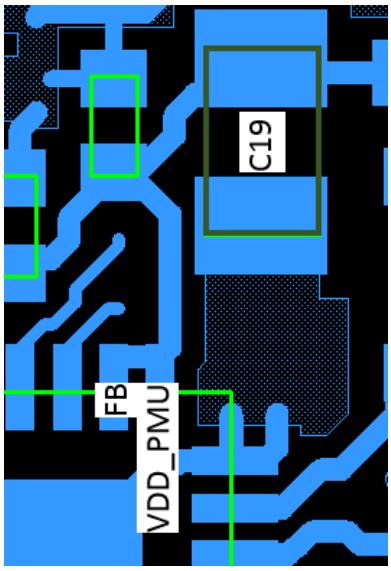


Figure 14. FB and VDD_PMU decoupling

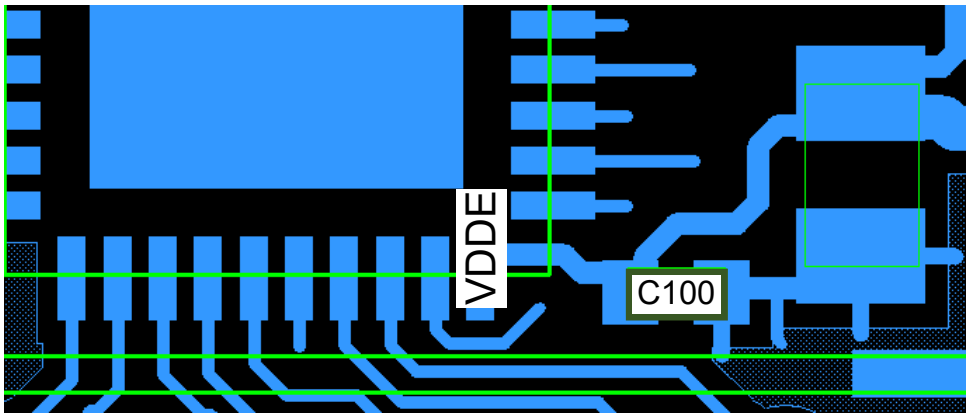


Figure 15. VDDE decoupling

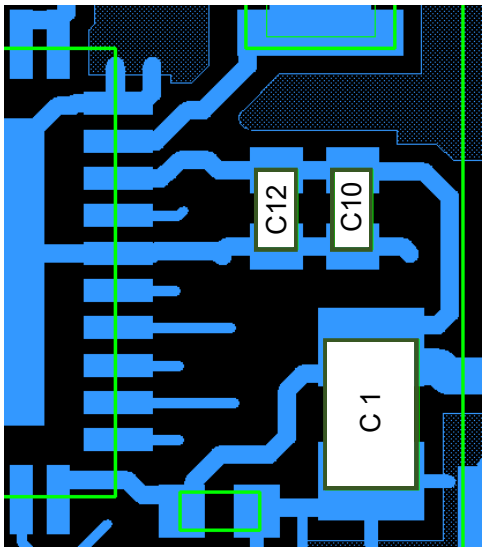


Figure 16. VBAT decoupling

4.12 Trace isolation

When PCB traces are in close proximity, they can talk to each other through the capacitor created by these traces.

To minimize the effect of this parasitic coupling, identify the most sensitive traces or areas (for example, RF trace, oscillator, power lines) and make them separate from any signal that is likely to couple with them through parasitics.

Separation can be achieved between two lines by increasing the distance between them.

4.13 GPIOs

GPIO traces are usually long lines that can cover long distances. They can carry undesirable signals that are likely to radiate in any direction. Routing of these signals should be avoided.

4.14 Screening can

The K32W device does not radiate high spurs, and it is very robust against electromagnetic interference. Therefore, in principle, there is no need for a screening can (or shielding can). Nevertheless, a footprint for a can has been added on the NXP reference designs, and NXP recommends you to add this footprint to any PCB. In some specific cases, such as in a very noisy environment, adding a can might be helpful.

5 Optimal PCB placement of a module

In case the K32W device is mounted on a design similar to NXP K32W-001-T10, care must be taken when mounting this design as a module onto another PCB.

The area around the antenna, for an absolute minimum of 20 mm, must be kept clear of conductors or other metal objects. This is true for all layers of the PCB and not just the top layer. Any conductive objects close to the antenna could severely disrupt the antenna pattern, resulting in deep nulls and high directivity in some directions.

The diagrams below show various possible scenarios. The top three scenarios are correct; ground plane may be placed beneath the K32W-001-T10 reference design, as long as, it does not extend beyond the edge of the top-layer ground plane on the main PCB.

The bottom three scenarios are incorrect because:

- The left-hand side example has ground plane underneath the antenna

- The middle example has insufficient clearance around the antenna (ideally, no conductors should be present anywhere near the antenna)
- The right-hand side example has the metal casing of a battery in the recommended keep-out area

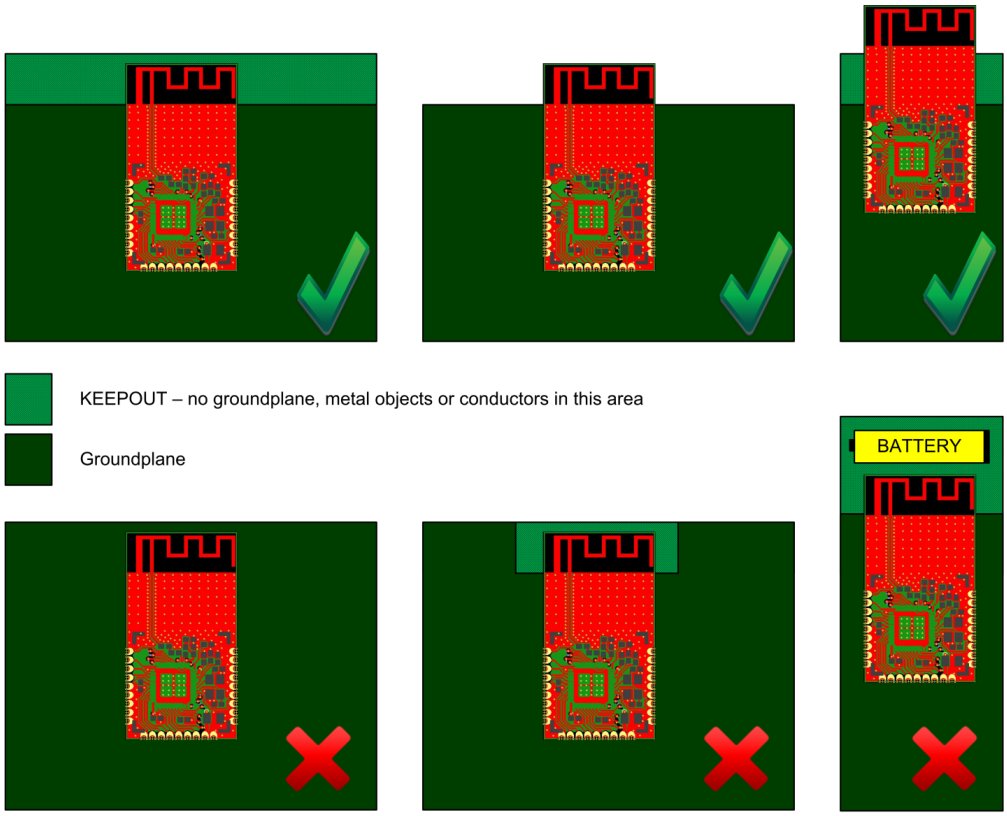


Figure 17. PCB placement of a K32W-based design with a printed antenna

6 Manufacturing considerations

When using reflow solder techniques, you should consider using the HVQFN package, which is a 40-pin QFN package. You can find footprint information of the package in the K32W data sheet.

The figure below shows the recommended PCB decal for the HVQFN40 package. The pad stacks used are 0.25 mm by 1 mm for the smaller pads, and a 6.4 mm square pad for the paddle.

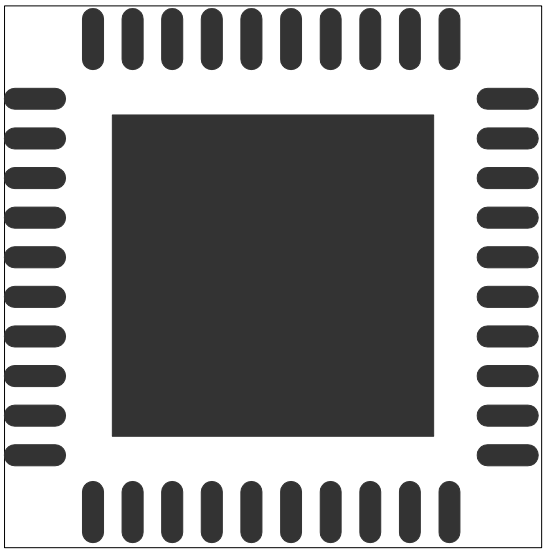


Figure 18. Recommended PCB decal for HVQFN40 package

The figure below shows the solder paste mask for the HVQFN40 package. The pad stacks used are 0.25 mm by 1 mm for the smaller pads, and four 1.6 mm square pads to apply paste to the paddle. The solder paste mask has a thickness of 6 thou (0.152 mm). If you need a different paste thickness, then you may need to change the number of pads the paste is applied to. Paste thickness may be dictated in a design by adding additional components.

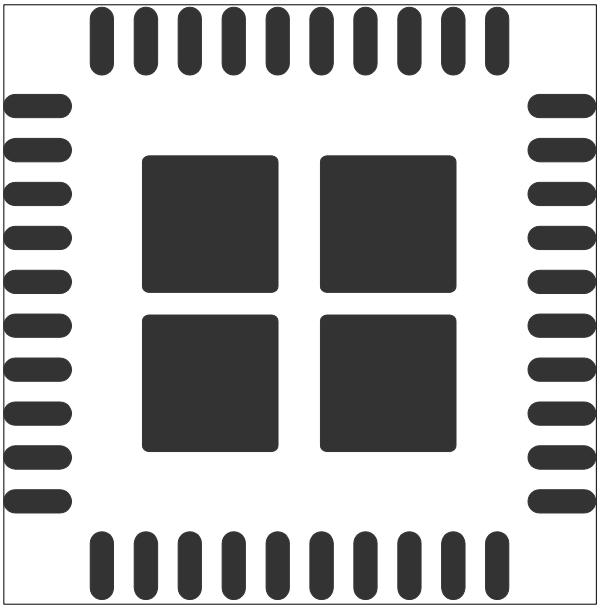


Figure 19. Solder paste mask for HVQFN40 package

The figure below shows vias on the paddle of the HVQFN40 package; 25 vias are applied to the paddle. These vias allow excess solder paste and heated air to be vented away from the device, preventing the device from being lifted during soldering. In addition, these vias ensure that a low-impedance ground is maintained, which is vital for optimum RF performance.

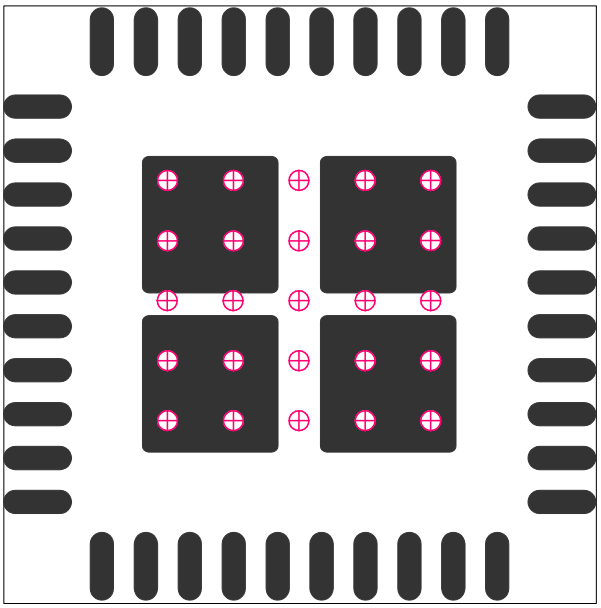


Figure 20. Vias on paddle of HVQFN40 package

7 Schematics design checklist

The table below describes checklist for schematics design.

Table 3. Schematic design checklist

Check number	Checklist item	Y/N/NA	Customer comments and/or actions	Check done by	NXP feedback
1	General				
1.1	Have you checked the schematics against NXP reference schematics and Hardware Design User Guide (JN-RM-2080)?				
1.2	Have you got the schematics reviewed by all the concerned stakeholders?				
1.3	Does the application use non-standard components (for example, components that were not used previously for such applications)?				
1.4	Have the non-standard components been qualified so that they can be used in the application?				
1.5	Are recommendations for layout / form factor written on the schematics?				
1.6	Are the components sized for the desired current drive capability?				

Table continues on the next page...

Table 3. Schematic design checklist (continued)

Check number	Checklist item	Y/N/NA	Customer comments and/or actions	Check done by	NXP feedback
1.7	Have you connected the K32W exposed pad to the ground?				
2	**RF input/output**				
2.1	Is the characteristic impedance of the RF input/output line 50 Ω over the full RF range?				
2.2	Have components with the correct types and values been connected to the RF port of the K32W device?				
2.3	For modules with external front-end module (FEM), does harmonic rejection require extra filtering?				
3	**32 MHz reference crystal**				
3.1	Is the reference crystal external configuration in accordance with the recommendations in Hardware Design User Guide (JN-RM-2080)?				
3.2	Have you followed the reference crystal model recommended by NXP?				
3.3	If you did not follow the NXP-recommended crystal model, have you checked all the parameters (load capacitance, pulling sensitivity, equivalent resistance, frequency tolerance, temperature range, frequency drift versus temperature, and aging) to ensure that NXP, standard, and application-specific requirements are met?				
4	**32 kHz reference crystal**				
4.1	Have you discussed and closed if a 32 kHz reference crystal is required (Zigbee specifications can be met without an external reference crystal)?				
4.2	If you implemented 32 kHz reference crystal, did you follow the reference crystal model recommended by NXP?				
4.3	If you did not follow the NXP-recommended crystal model, have you checked all the parameters (load capacitance, pulling sensitivity, equivalent resistance, frequency tolerance, temperature range, frequency drift versus temperature, aging) to ensure that NXP, standard, and application-specific requirements are met?				

Table continues on the next page...

Table 3. Schematic design checklist (continued)

Check number	Checklist item	Y/N/NA	Customer comments and/or actions	Check done by	NXP feedback
5	**Power supply**				
5.1	Have all the VDD pins been connected according to NXP recommendations?				
5.2	Are the power supply regulators / battery well sized?				
5.3	Have you implemented the decoupling of the supply regulators / battery output?				
5.4	Have you decoupled the power supply pins of the chip properly (according to Hardware Design User Guide (JN-RM-2080) and reference design schematics?)				
5.5	Have the recommendations for the values and models of DC-DC converter components been considered?				
5.6	Have you connected the exposed die pad to GND?				
6	**Programmed inputs/outputs (PIOs)**				
6.1	Have you checked the compatibility of the logic levels with other components?				
6.2	Does the maximum source/sink current fit the application?				
7	**ADC**				
7.1	Do the ADC characteristics fit the application?				
8	**Programming and debug**				
8.1	Have you connected the flash programming connector to the correct input/output on the MCU?				
8.2	Have you added a connector to put the MCU into programming mode (using RSTN and PIO5/ISP pins) for debugging?				
8.3	Is the reset pin RSTN connected properly?				
8.4	Add a test point at an unused digital input/output (DIO) such that a trigger signal can be output from the pin for sensitivity measurements				
8.5	For printed and chip antennas: Have you implemented the RF transmission line in such a manner that the hardware can easily be modified to serve both the following purposes:				

Table continues on the next page...

Table 3. Schematic design checklist (continued)

Check number	Checklist item	Y/N/NA	Customer comments and/or actions	Check done by	NXP feedback
	• Used for real application • Used for debugging purposes For example, 0 Ω resistors can be used to connect/disconnect the K32W RF port to the antenna (for real application) and an SMA or a µFL connector (for debugging).				
8.6	If I2C is used, are the I2C lines pulled up?				
9	**External memory**				
9.1	If you have used an external flash memory, is it the correct type of memory and is it connected to the MCU correctly?				
9.2	Have you verified flash memory connections?				

8 Layout design checklist

The table below describes checklist for layout design.

Table 4. Layout design checklist

Check number	Checklist item	Y/N/NA	Customer comments and/or actions	Check done by	NXP feedback
1	**General**				
1.1	Have you discussed and closed how many layers are needed?				
1.2	Have you checked the layout against NXP reference board?				
1.3	Have the hardware recommendations of the K32W Hardware Design User Guide (JN-RM-2080) been followed?				
1.4	Have you specified the correct PCB material in the layout?				
1.5	Have you specified the correct PCB thicknesses in the layout?				
2	**RF input/output (RFIO)**				
2.1	Is the RF input/output line well-sized for 50 ohm? The line width must be calculated based on the board thickness and PCB material.				

Table continues on the next page...

Table 4. Layout design checklist (continued)

Check number	Checklist item	Y/N/NA	Customer comments and/or actions	Check done by	NXP feedback
2.2	Are the RF wires as short as possible (wires behave as antennas so shortening them helps to increase immunity against electromagnetic interference)?				
2.3	Have vias been avoided in the RF line?				
2.4	Have you copied exactly the placement of the RFIO matching network from the NXP reference design?				
3	**Reference crystal**				
3.1	Have you placed the 32 MHz reference crystal close to the MCU?				
3.2	Are there GND vias around the 32 MHz reference crystal?				
4	**Power supply**				
4.1	Have all the VDD capacitors been placed as close as possible to the power pins and voltage regulator outputs?				
4.2	If power is routed on several layers, have you provided multiple vias in the power lines?				
4.3	For low-supply-voltage (close to 2.0 V) application, ensure that the supply track is well-dimensioned to avoid IR drop and resulting false brownout trigger (IR drop is the voltage drop occurring due to the supply current flowing into the supply track resistance)				
4.4	Have the VDD lines been isolated from potential interferences?				
4.5	Is GND plane continuous around and near all signals?				
4.6	Have you connected the die pad to GND?				
4.7	Are vias implemented in the die pad?				
5	**EMC and misc.**				
5.1	In case more than two layers are used, does one layer act as a continuous ground plane (GND reference plane)?				
5.2	Are several vias added near capacitors, near fingers, and so on?				
5.3	Remove small GND areas and isolated fingers that cannot be connected to the reference GND plane through vias				

Table continues on the next page...

Table 4. Layout design checklist (continued)

Check number	Checklist item	Y/N/NA	Customer comments and/or actions	Check done by	NXP feedback
5.4	Have you added silkscreen text with relevant information (such as component reference, logo, board name)?				
5.5	Is all silkscreen text readable when the board is populated?				
5.6	Have traces been avoided underneath noisy or sensitive components?				
5.7	Ensure that traces do not cut across power or ground planes, unnecessarily				
5.8	Does the K32W footprint in your design match exactly with the footprint in the NXP reference design?				
5.9	If more than two layers are used, then the inner layers must be left empty under the RF components and the antenna				
5.10	Each connection between a component and GND must be doubled with a via to the GND plane				
5.11	Have you separated the soldering / non-soldering areas properly? Have you ensured that the solder resist layer only covers the empty areas?				
5.12	Have you implemented can/shield in a design unit to be shipped soon?				

9 Acronyms

The table below lists the acronyms used in this document.

Table 5. Acronyms

Acronym	Meaning
BOM	Bill of materials
CFR	Code of Federal Regulations
CPW	Coplanar waveguide
EMC	Electromagnetic compatibility
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FEM	Front-end module
PCB	Printed circuit board
RED	Radio Equipment Directive (EU directive 2014/53/EU)

Table continues on the next page...

Table 5. Acronyms (continued)

Acronym	Meaning
RF	Radio frequency
SRF	Self-resonant frequency

10 References

For more information on the K32W device, see the following documents:

- *K32W061/K32W041 Data Sheet* (IEEE 802.15.4 and Bluetooth LE 5.0 wireless microcontroller)
- *K32W041A/K32W041AM Data Sheet* (IEEE 802.15.4 and Bluetooth LE 5.0 wireless microcontroller)

11 Revision history

The table below summarizes the revisions to this document.

Table 6. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 1.2	03 January 2022		• Replaced "K32W-001-M10" and "K32W-001-M13" each with "K32W-001-T10" throughout the document • Replaced "K32W061-001-M16" with "K32W-001-T16" throughout the document
Rev. 1.1	17 March 2021		Added K32W041-related details
Rev. 1.0	01 February 2018		Initial document release

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