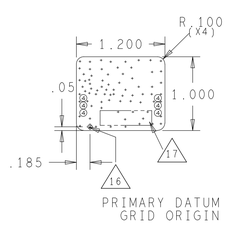
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	11-11-15	F.L.
	A1	UPDATED THE LOGO TO NXP	12-11-15	F.L.
	A2	UPDATED THE COPYRIGHT	02-22-16	F.L.

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - NOT APPLICABLE
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.005"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
   2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - ORANGE COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. TWO SOLDER SAMPLES TO BE PROVIDED.
16. BASIC GRID INCREMENT AT 1:1 IS .0001.
17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN,
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (94)
19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
    ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125"NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER.PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
22. INTENTIONAL SHORTS AT:
    SH1 5VDC_IN & 5VDC
    SH2 AOUT_5V & ANALOG5V
    SH3 GND_S & GND

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	8.0	+0.0/-8.0	PLATED	75
⊙	40.0	+3.0/-3.0	PLATED	6
⌖	25.0	+2.0/-2.0	NON-PLATED	1

(8)



PRIMARY DATUM
GRID ORIGIN

		FINISHED Cu WEIGHT
LAYER 1	L1_PS	1 oz.
LAYER 2	L2_SS	1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

___ PUBI (PUBLIC INFORMATION)
_X_ IUO (NXP INTERNAL USE ONLY)
___ CP (NXP CONFIDENTIAL PROPRIETARY)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX .01 .0-30'
.XXX .005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN FRANK L	02-22-16
CHECKED KRITHI S	02-22-16
DESIGN ENGINEER FRANK L	02-22-16

PART NO. 170-28987

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
BRKTSTBCDP5004

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-28987	FAB-28987	A2

SCALE 1/1 | DO NOT SCALE DRAWING | SHEET 1 OF 1