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Revisions & Change Log

Rev	Description	Date	Approved
X1	First Release	12/20/18	
X2	J39 added for CAN/LIN DIR pin	01/08/19	
A	Prototype Release	01/24/19	
B	Sensor VDD to 3V3 Layout implementations RF matching update	07/08/19	M.Baudry
B1	RF optimization (BOM)	10/15/19	

FREEDOM KW38

Bluetooth Smart/Generic FSK

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: ANTONIO QUIROZ	Drawing Title: X-FRDM-KW38A	
Drawn by: ANTONIO QUIROZ	Page Title: TITLE PAGE	
Approved: Matthieu Baudry	Size C / Document Number SCH-43110_B PDF: SPF-43110_B	Rev B1
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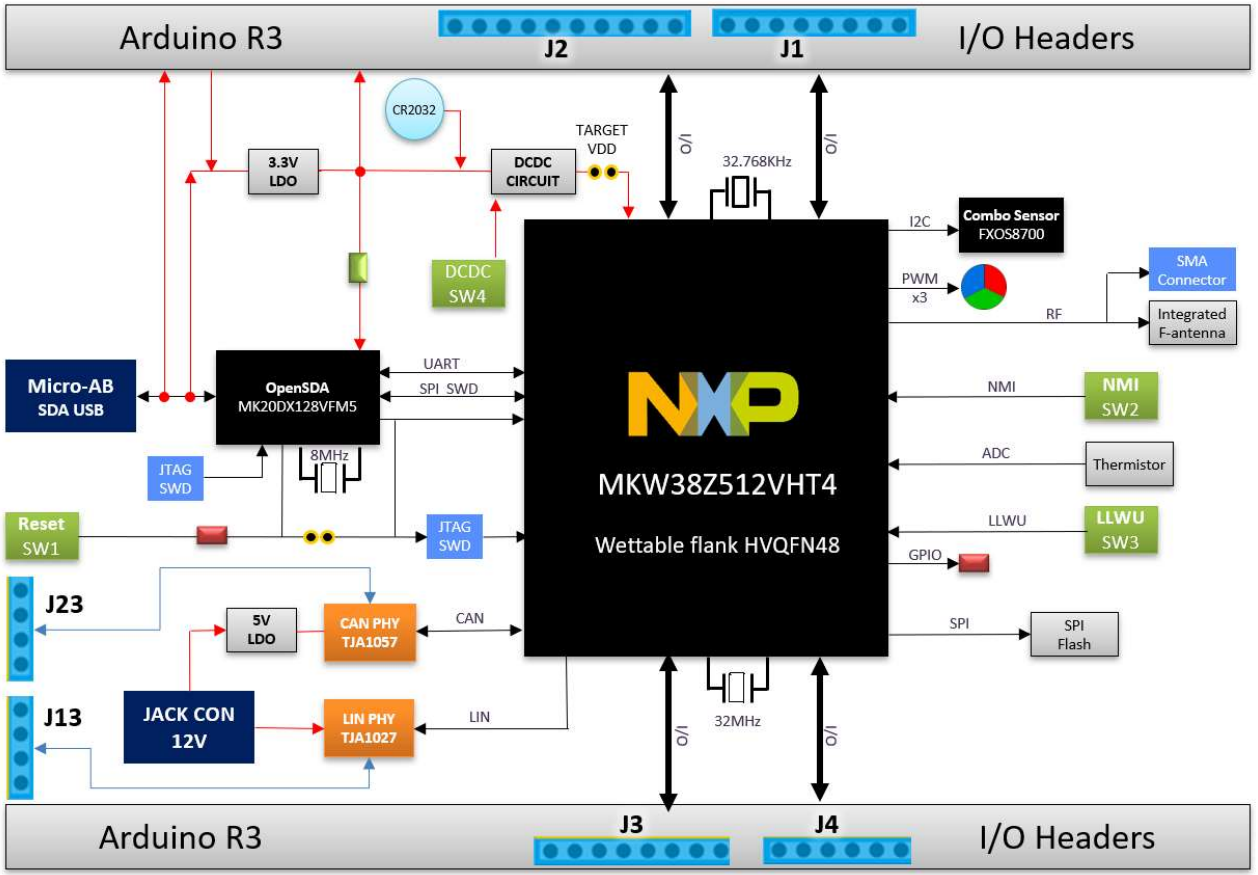
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



ICAP Classification: CP: ___ IUO: X PUBI: _

Drawing Title: **X-FRDM-KW38A**

Page Title: **BLOCK DIAGRAM**

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Power Configuration

Default: Buck Mode (auto start).

	PSW_CFG J38	REG_CFG J27, J30
Bypass Mode (auto start) VDCDC_IN (1.71 to 3.6V) Operation 1.8V - 3.6 V	1~2	J27-on J30-on
Buck Mode (manual start) VDCDC_IN (1.8V to 3.6V) Coin Cell Battery Operation	1~2 press SW4 to start	J27-off J30-off
Buck Mode (auto start) VDCDC_IN (1.8V to 3.6V) Coin Cell Battery Operation	2~3	J27-off J30-off

V_BATTshould NOT exceed 3.6V.

Default 1-2.

PSW_CFG

SHORTING 2-3 ON BOTTOM LAYER

REG_CFG

Default J27-off, J30-off.

Default: on.

SHORTING HEADER ON BOTTOM LAYER

Default: on.

SHORTING HEADER ON BOTTOM LAYER

Place caps close to VDD_RF pins

Place caps close to VDD0/VDD1 pins

VCO leakage decoupling capacitors.

Place cap close to VDCDC_IN

MKW38A512VFT4

Custom shield.

Place components close to DUT

Place ind close to DUT

POWER MANAGEMENT

32MHz XTAL & 32kHz XTAL

RF

CAD NOTE: SMA - F-Antenna: Place both capacitor sharing pin 1

CAD Note: 50 ohm controlled impedence line

CAD NOTE: Open Solder Mask Bottom below F-Antenna on "feedpoint" via

COIN CELL HOLDER

LED_PWR_CFG

SHORTING 1-2 ON BOTTOM LAYER

SWD CONNECTOR

SHORTING HEADER ON BOTTOM LAYER

Jumper is shorted by a cut-trace on bottom layer. Cutting the trace will effectively isolate the on-board MCU from the OpenSDA debug interface.

IN CIRCUIT TEST GND PROBING

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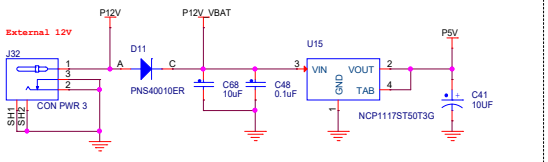
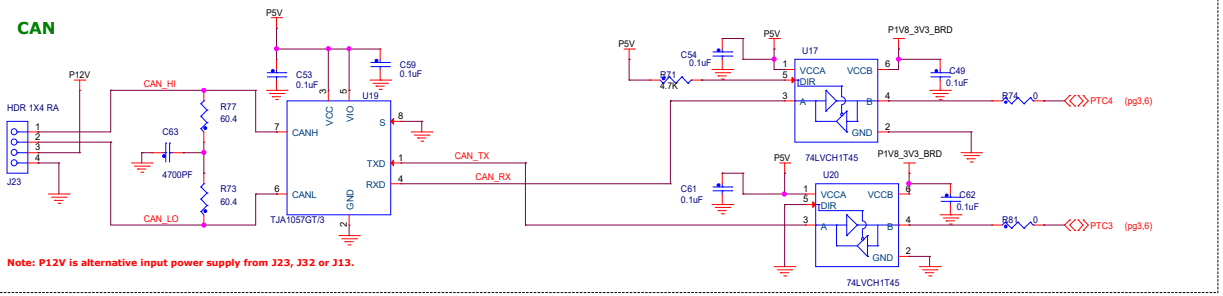
OpenSDA Interface

CAN/LIN Power

Note: P12V is alternative input power supply from J23, J32 or J13.

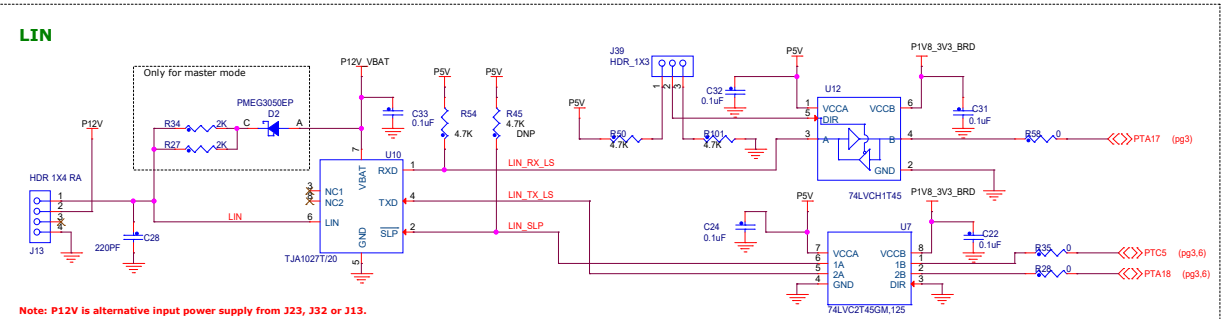


CAN



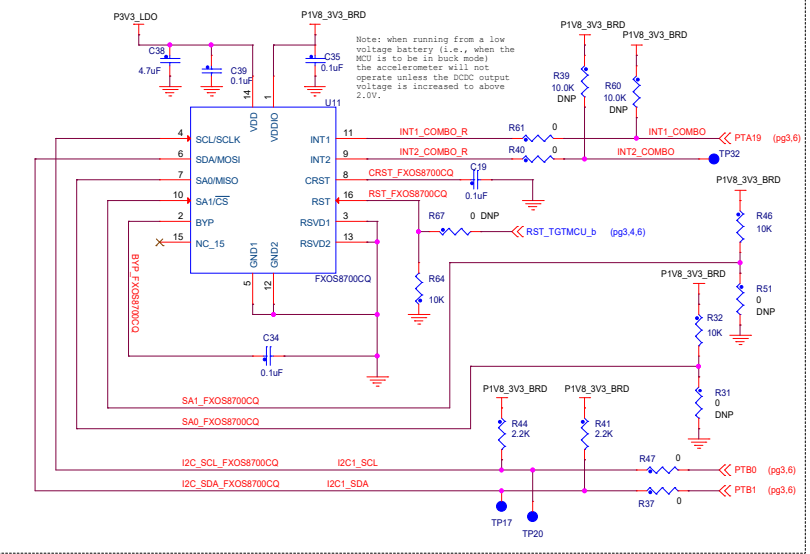
Note: P12V is alternative input power supply from J23, J32 or J13.

LIN

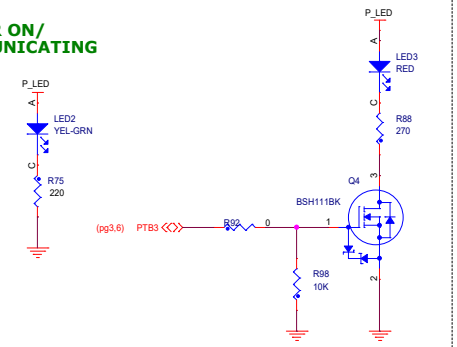


Note: P12V is alternative input power supply from J23, J32 or J13.

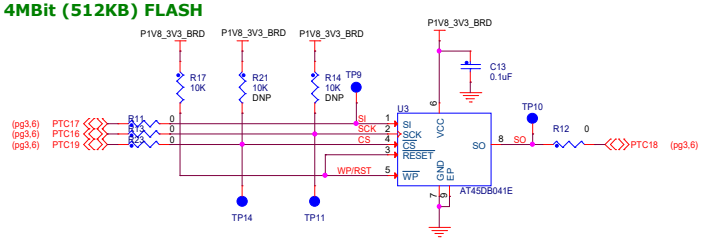
FXOS8700CQ COMBO SENSOR



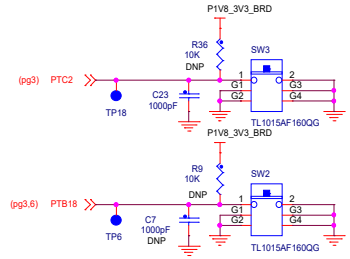
POWER ON/ COMMUNICATING



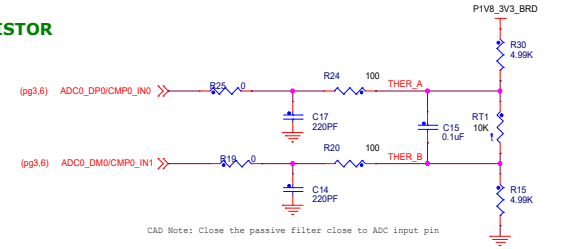
4MBit (512KB) FLASH



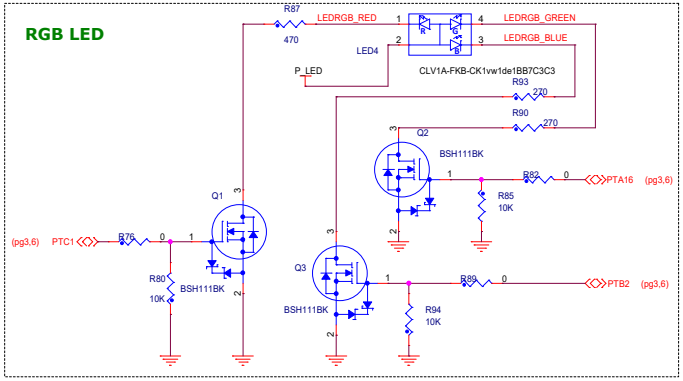
INTERRUPT PUSH BUTTONS



THERMISTOR



RGB LED



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ARDUINO COMPATIBLE HEADERS