ART FILM - FAB.art

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	10-22-20	D.V.

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .003"/.003"

7. PLATING FINISH: A. BOTH SIDES ENIG: TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
   GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
   TYPE: LPI OR EQUIVALENT.
   A. LOCATION = +/-.002" OF PLATED PADS.
   B. DIAMETER OR SIZE = +/-.002 OF ORIGINAL DATA

10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.

11. ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (PG)

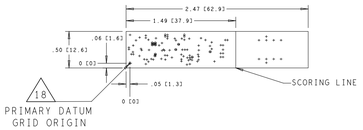
17. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

18. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.

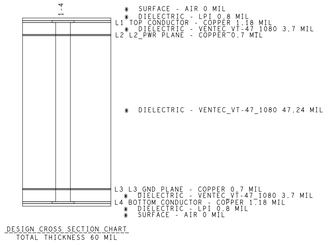
19. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

20. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS, KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.

21. THIS BOARD USES VIA-IN-PAD: SEE FAB_VIAFILL.ART
   A. ALL VIAS USING X.1 DRILL SIZES ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL, LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.
   B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.
   C. DIMPLE OR PROTRUSION ON VIA-IN-PADS MUST BE NO GREATER THAN .001".



DETAIL A
LAYER STACKUP
SCALE: NONE
BOARD THICKNESS TOLERANCE +/-10%



DESIGN CROSS SECTION CHART
TOTAL THICKNESS 60 MIL

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

LAYERS	SE		DIFF			
	TRACE WIDTH	IMPEDANCE	TRACE WIDTH	TRACE SPACING	IMPEDANCE	REFERENCE LAYER
L1_PS	5.98	50.00	5.90	5.90	90.00	2
L4_SS	5.98	50.00	5.90	5.90	90.00	3

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
+	8.0	+0.0/-8.0	PLATED	88
⊖	8.1	+0.0/-8.1	PLATED	11
8	47.24x19.68	+3.0/-3.0	PLATED	2

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ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL MEET THE RoHS COMMISSION DELEGATED DIRECTIVE (EU) 2015/863 OF 31 MARCH 2015 AMENDING ANNEX II TO DIRECTIVE 2011/65/EU. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL NOT CONTAIN ANY OF THE SUBSTANCES OF VERY HIGH CONCERN (SVHC) ABOVE THE THRESHOLD VALUE PER THE CURRENT ECHA LIST OF SVHC'S AND WITH ANNEX XIV AND ANNEX XVII OF REACH DIRECTIVE 76/769/EEC. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

___ COMPANY PUBLIC
_X_ COMPANY INTERNAL
___ COMPANY CONFIDENTIAL

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN, PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX .01 .0-30'
.XXX .005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS, REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN W. MEAD	10-22-20
CHECKED DELEEP VADLAMUDI	10-22-20
DESIGN ENGINEER HELEN XU	10-22-20

PART NO. 170-47770

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
X-PTN38007-BASE

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-47770	FAB-47770	A

SCALE 1/1 | DO NOT SCALE DRAWING | SHEET 1 OF 2

ART FILM - FAB.art

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2 THIS FAB_VIAFILL.ART SHOWS LOCATIONS OF VIA-IN-PAD TO BE FILLED.

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6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

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D	LAY-47770	FAB-47770	A

SCALE 1/1 | DO NOT SCALE DRAWING | SHEET 2 OF 2