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Revisions & Change Log			
Rev	Description	Date	Approved
X1	First Release	05/13/21	
X2	J7 replaced for U.FL connector 22pF Ser caps added to RF ports 1x2,1x3 headers replaced for 2MM	05/28/21	
X3	U6 changed for 100pin version	06/02/21	
X4	Matching network optimized RF switch updates	07/13/21	
A	Released files	08/04/21	
A1	Antenna Control Table updated Matching network updated	10/25/21	
A2	L2 updated to 15nH Pulldown for MCULink HW VER PWR jumpers updated CAN support U1 changed for 48-pin version C30 changed for 10uF MCULink HW VER config updated 100K pul-up TGTMCU TX line Block diagram updated SH19 added	12/02/21 12/20/21 01/14/22 01/25/22	
B	Matching values updated (C10, C12, R2, R3) Net HW VER renamed to HW_VER_8 Added JP13 & JP14 PTA16 & PTA17 for LPUART0 C1 & L10 updated, R5 Removed C100-C102 changed to 100pF PTD2 & PTD3 to J2 connector LED2 drive through PTC6 JP22 & JP23 added R107, R108 & L13 added R109 added C38, C32, C34 values updated BOOT CONFIG section updated	03/30/22 04/08/22 04/21/22 04/25/22 04/29/22 05/25/22	M.R.
C	R92 to DNP Replace C96 and populate R110 PSV CAN tied to PSV JP2* added for RST disable @U11 JP2 replaced for a 2x2 header Swap CAN from PTC0/1 to PTC4/5 U1 update MPN according DS U21 added to RF path - DNP	12/20/22 01/20/23	E.L.
C1	RF matching updated C1,C2,L10	02/24/22	M.R.
C2	RF matching updated C1,C2,L10	08/01/23	M.R.

KW45B41Z-LOC

Bluetooth Smart/Generic FSK

(KW45 Localization Kit)

		BL Edge Processing 6501 William Cannon Drive West Austin, TX 78735-8598	
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<small>© NXP SEMICONDUCTORS</small>		<small>Classification: <FCP> <FIUD></small>	
<small>Designer: ANTONIO QUIROZ</small>		KW45B41Z-LOC	
<small>Drawn by: ANTONIO QUIROZ</small>		TITLE PAGE	
<small>Approved: Miguel Reyes</small>	<small>Size C</small>	<small>Document Number SCH-50702 PDF: SPF-50702</small>	<small>Rev C2</small>
<small>Date: Tuesday, August 01, 2023 Sheet 1 of 8</small>			

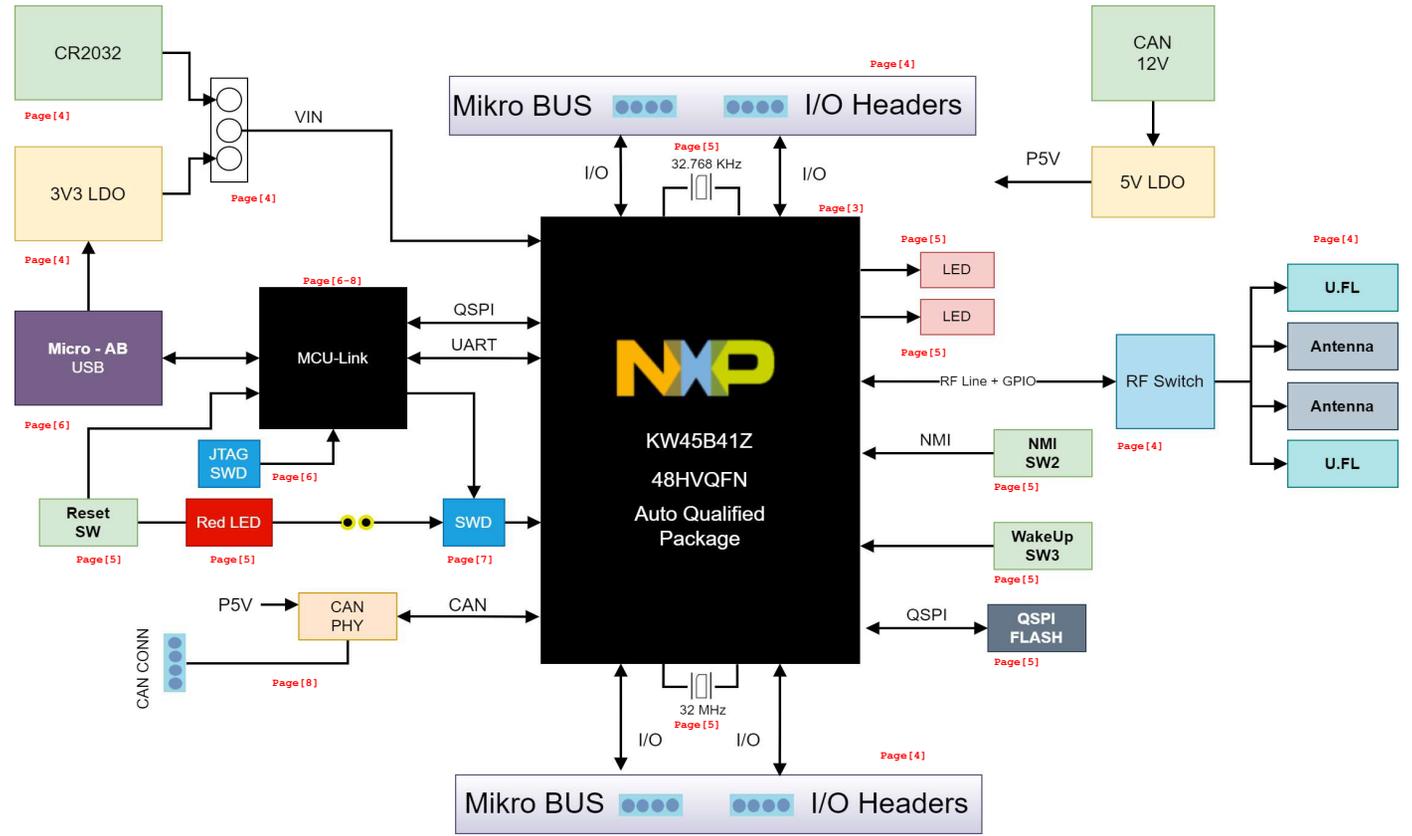
NOTES

- Unless Otherwise Specified:
 - All resistors are in ohms, 5%, 1/8 Watt
 - All capacitors are in uF, 20%, 50V
 - All voltages are DC
 - All polarized capacitors are aluminum electrolytic
- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- Device type number is for reference only. The number varies with the manufacturer.
- Special signal usage:
 - _B Denotes - Active-Low Signal
 - <> or [] Denotes - Vectored Signals
- Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

NOTES

- This Color is for User Notes
- This Color is for CAD/LAY Notes
- This Color is custom Shield Notes
- This Color is for Silk
- This Color is for DNP components

Target MCU: KW45B41Z p[3]
 Debug MCUlink: LPC55S69 p[6]

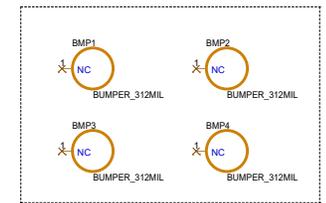


REF DES	SHORTED(DEFAULT)	PAGE NAME
SH1,SH2,SH3,SH4,SH5,SH6,SH7,SH8,SH9,SH10,SH11,SH12,SH13,SH14,SH19	CLOSED	04. PWR MANAGEMENT
JS1,JS2	CLOSED	05. LED, MEMORY, MISC
SH15	CLOSED	07. MCU Link SWD

REF DES	JUMPER(DEFAULT)	PAGE NAME
JP1,JP3,JP4,JP6,JP7,JP8,JP9,JP10	1-2	04 - PWR MANAGEMENT
JP23,JP24	1-2	04 - PWR MANAGEMENT
JP2	2-4	04 - PWR MANAGEMENT
JP11	1-2	05 - LED, MEM & MISC
JP12,JP21,JP22	OPEN	06 - MCU LINK
JP16	1-OPEN	07 - MCU LINK SWD
JP17	OPEN	07 - MCU LINK SWD
JP18,JP25	1-2	07 - MCU LINK SWD
JP13, JP14	1-2	08 - MCU LINK IO

REF DES	ASSY_OPT	PAGE NAME
C1,C4,C10,C12,C16,C21,C22	DNP	03 - MKW45B41Z MCU
R89,C27,C29,C37,C38,BT1	DNP	04 - PWR MANAGEMENT
R9,R10,R11,R15,R17,R18,R21,C48,C49,C50,Y3,JS1,JS2	DNP	05 - LED, MEM & MISC
R41,R42,R55,R56,R87,R88,C77,C78,J4	DNP	06 - MCU LINK
R65,R66,C113	DNP	07 - MCU LINK SWD

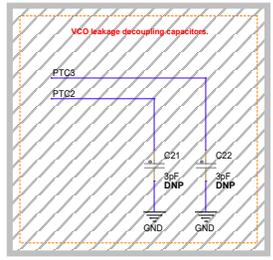
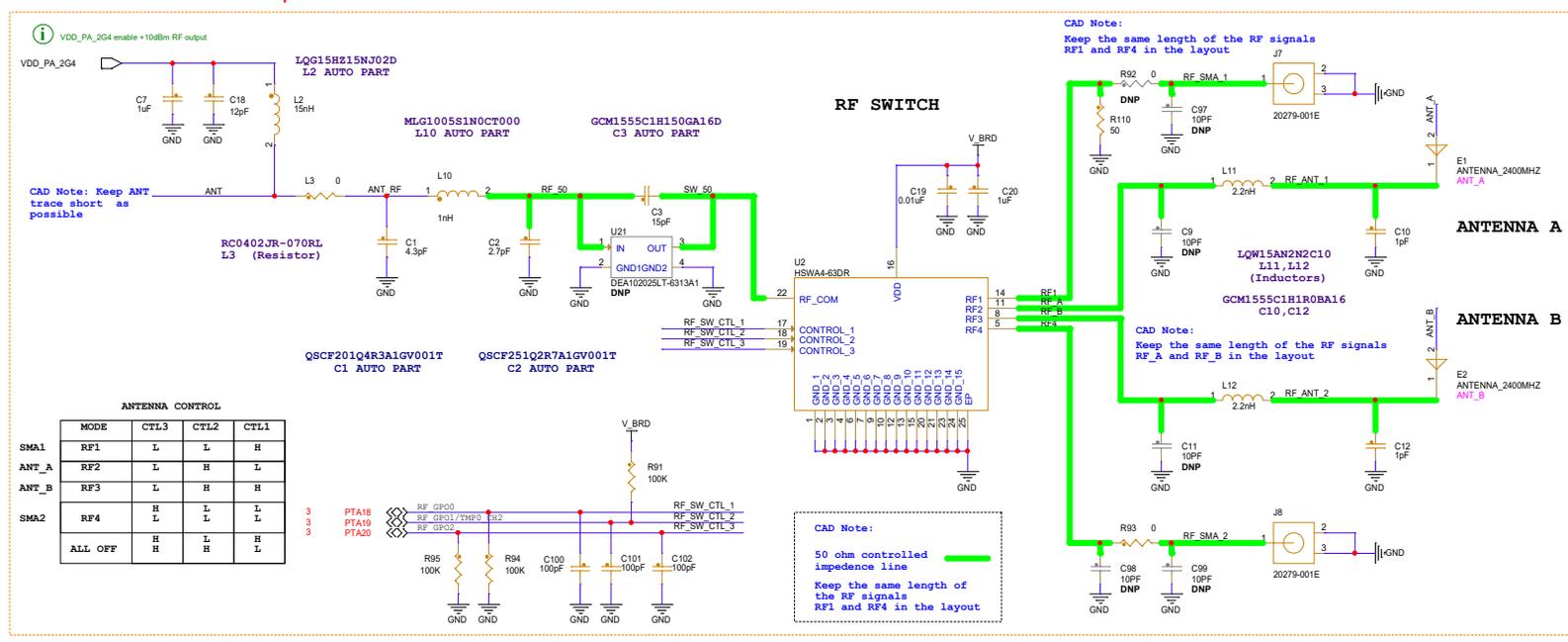
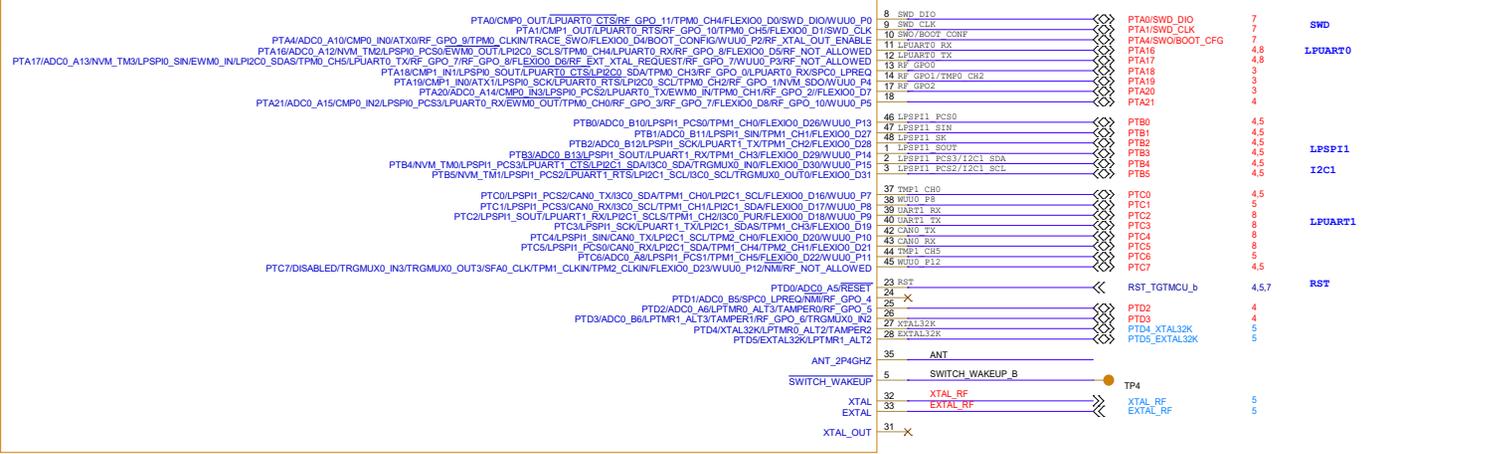
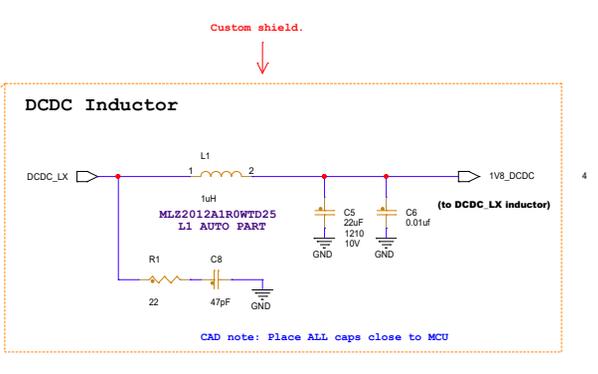
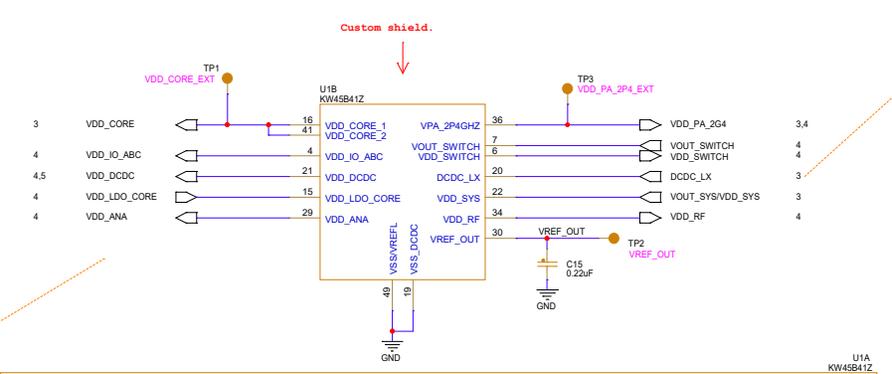
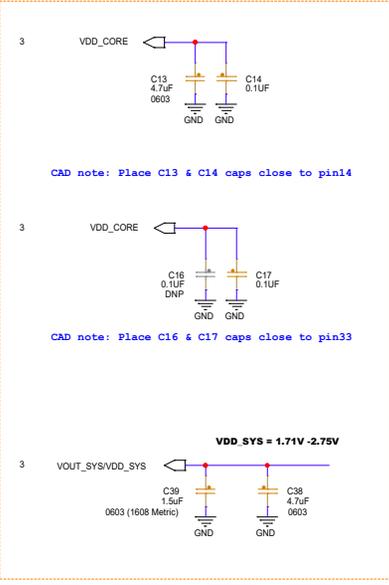
BUMPON added to each bottom side corner



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ICAP Classification: CP: IUC: X PUBL: _____
 Drawing Title: **KW45B41Z-LOC**
 Page Title: **BLOCK DIAGRAM**

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Antenna Matching Alt Parts
 L11 & L12 MPN:L-07C2N2S5V6T
 C10 & C12 MPN:L-500R07S1R0BV4T

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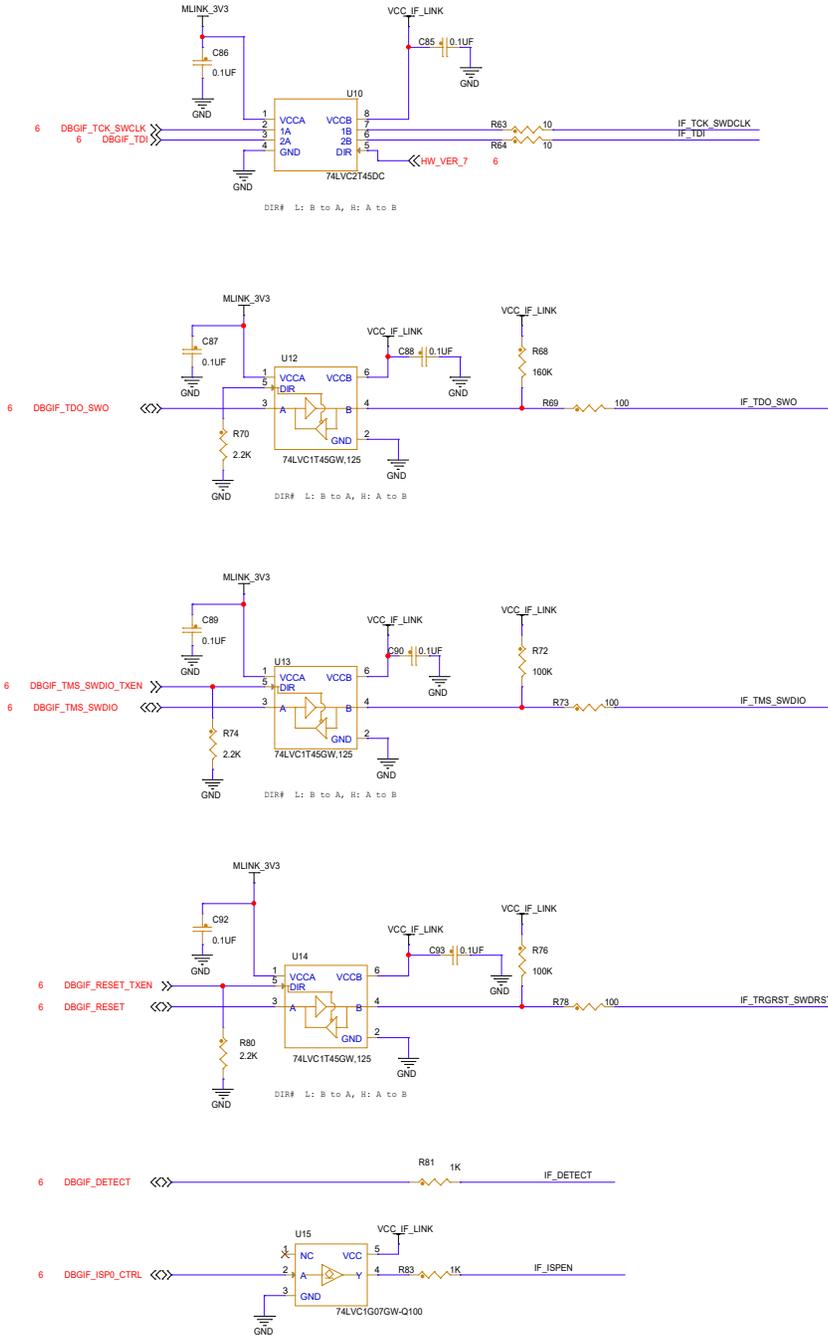
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 Page Title: **MKW45B41Z MCU**

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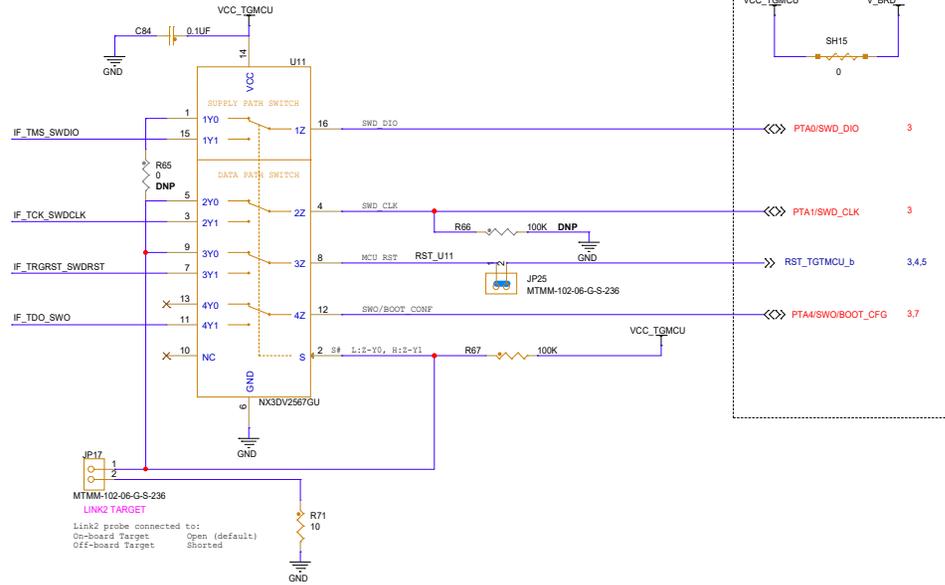
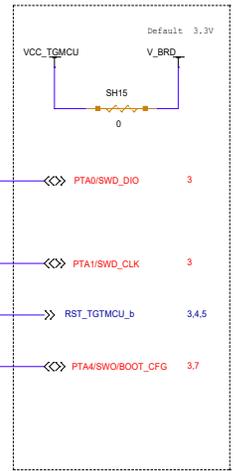
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MCU LINK

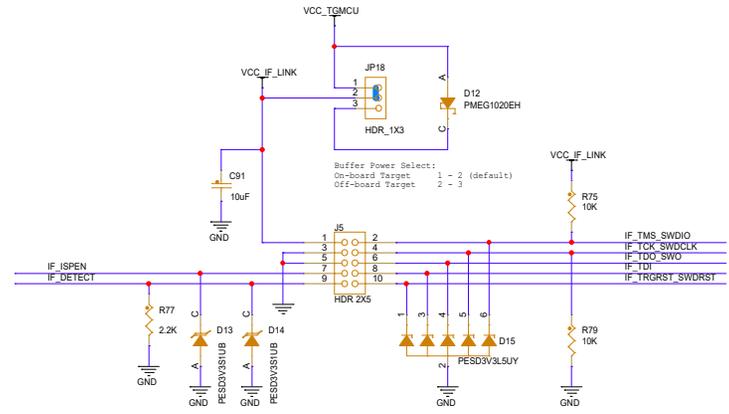
Debug Interface



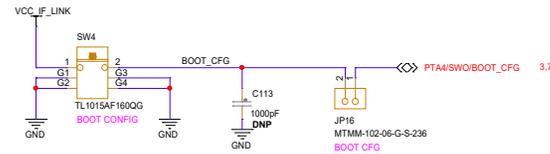
Target MCU



10pin JTAG/SWD



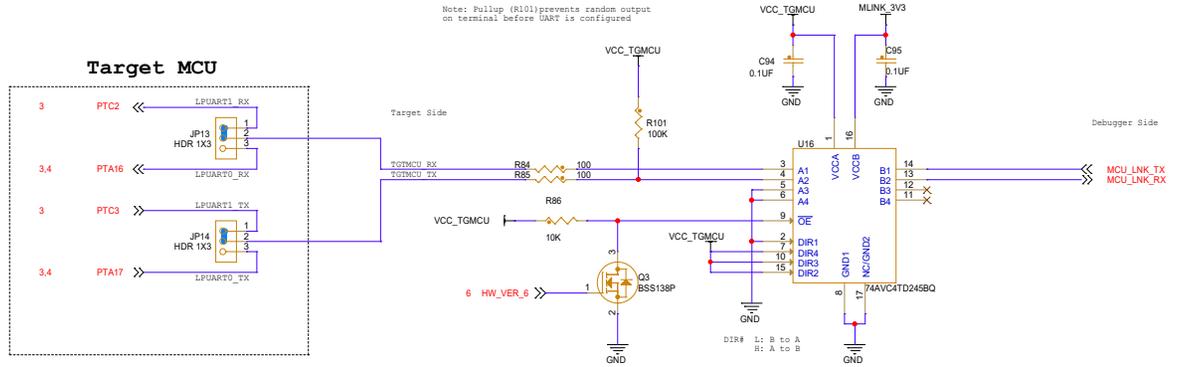
BOOT CONFIG



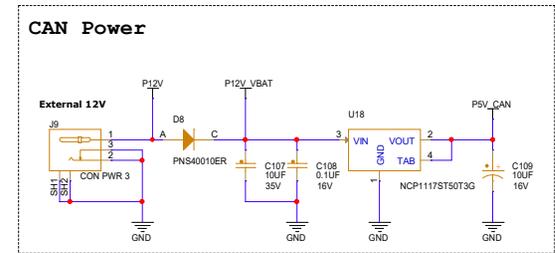
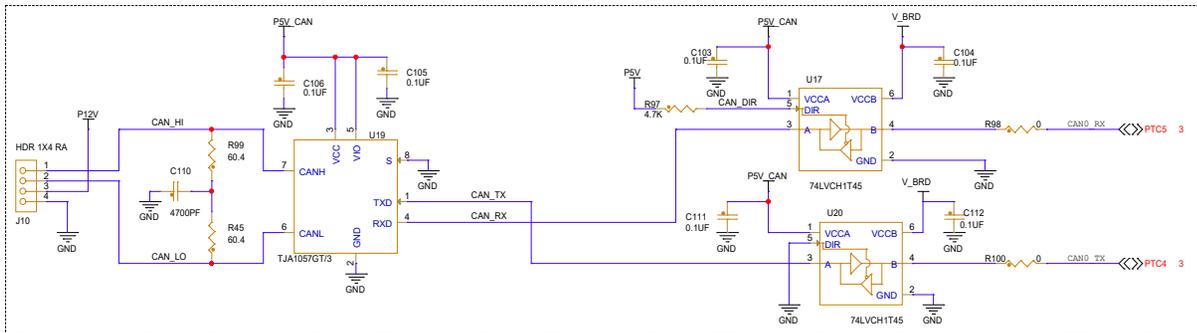
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Drawing Title: KW45B41Z-LOC					
Page Title: MCU LINK DEBUGGER					
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MCU LINK

Voltage Translation Buffers



CAN SUPPORT



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Page Title: MCU LINK IO					
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