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NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .004"/.005"

7. PLATING FINISH: A. BOTH SIDES ENIG: TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).

8. FAB VENDOR IS NOT ALLOWED TO USE ODB FOR FABRICATION. CAN BE USED ONLY FOR REFERENCE.

9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
   GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
   TYPE: LPI OR EQUIVALENT.
   A. LOCATION = +/-.002" OF PLATED PADS.
   B. DIAMETER OR SIZE = +/-.002 OF ORIGINAL DATA

10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.

11. ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)

18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.

20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

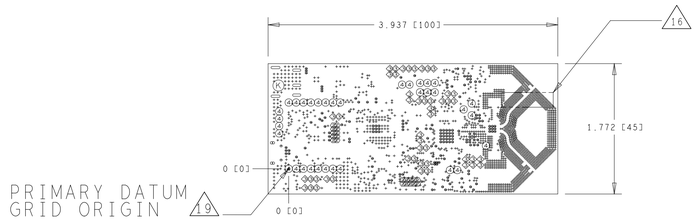
21. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS, KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.

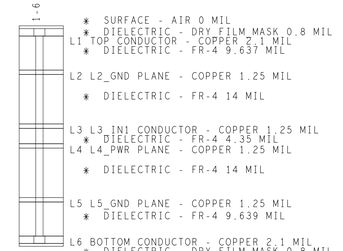
22. THIS BOARD USES VIA-IN-PAD: SEE FAB_VIAFILL.ART
    A. ALL VIAS USING X.1 DRILL SIZES ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL, LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.
    B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.
    C. DIMPLE ON VIA-IN-PADS MUST BE NO GREATER THAN .003" AND PROTRUSION NO GREATER THAN .002"

23. INTENTIONAL 18 SHORTS AT:

LocationStart	LocationEnd	RefDes	Net 1	Net 2
(100.00 110.00)	(100.00 70.00)	SH5	PTC7	LLWU/NMI_B
(40.00 -70.00)	(0.00 -70.00)	SH3	PTD2/TMP1_CH0	PWM/TMP1_CH0
(0.00 833.00)	(0.00 793.00)	SH2	ADC_IN	ADC0_A13
(100.00 833.00)	(100.00 793.00)	SH1	RESET	RST_TGTMCU_B
(300.00 110.00)	(300.00 70.00)	SH9	PTA17	LPUART0_TX
(200.00 110.00)	(200.00 70.00)	SH7	PTA16	LPUART0_RX
(300.00 833.00)	(300.00 793.00)	SH6	LPSPI1_SCK	PTB2
(200.00 833.00)	(200.00 793.00)	SH4	LPSPI1_PSC0	PTB0
(521.26 -140.00)	(600.00 -140.00)	J52	P_LED	V_BRD
(460.00 -73.03)	(500.00 -73.03)	SH13	PTD3/I2C1_SDA	LPI2C1_SDA
(400.00 110.00)	(400.00 70.00)	SH11	PTB5	LPI2C1_SCL
(400.00 833.00)	(440.00 833.00)	SH8	LPSPI1_SIN	PTB1
(500.00 833.00)	(540.00 833.00)	SH10	LPSPI1_SOUT	PTB3
(600.00 110.00)	(600.00 70.00)	SH14	P5V	5V_MIKROE
(1652.41 275.60)	(1692.41 275.60)	SH15	V_BRD	VCC_TGMCU
(1642.41 1012.71)	(1642.41 933.97)	J51	VDD_MEM	V_BRD
(1969.89 1280.00)	(1906.89 1280.00)	SH19	P3V3_LDO	V_BRD
(2483.41 955.97)	(2483.41 995.97)	SH12	3V3_MIKROE	V_BRD

REVISIONS					
ZONE	REV	DESCRIPTION	DATE	APPROVED DE	PE	CAD
	A	ORIGINAL RELEASE	08-24-21	A.Q.	J.C.	E.L.
	B	SECOND RELEASE	05-25-22	A.Q.	J.C.	E.L.
	C	THIRD RELEASE	02-02-23	A.Q.	J.C.	E.L.





DESIGN CROSS SECTION CHART
TOTAL THICKNESS 62.426 MIL
BOARD THICKNESS TOLERANCE +/-10%

DETAIL A
LAYER STACKUP
SCALE: NONE

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

LAYERS	SE		DIFF								COPLANAR		
	TRACE WIDTH	IMPEDANCE	TRACE WIDTH	TRACE SPACING	IMPEDANCE	REFERENCE LAYER	TRACE WIDTH	TRACE SPACING	IMPEDANCE	REFERENCE LAYER	TRACE WIDTH	GAP	IMPEDANCE
L1_PS	N/A	N/A	9.50	6.50	90.00	2	11.00	12.00	100.00	2	11.00	6.00	50.00
L3_INT_1	5.00	50.00	4.00	7.00	100.00	2/4	N/A	N/A	N/A	N/A	N/A	N/A	N/A
L4_INT_2	5.00	50.00	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
L6_SS	N/A	N/A	9.50	6.50	90.00	5	11.00	12.00	100.00	5	N/A	N/A	N/A

*IMPEDANCE TABLE VALUES ARE BASED ON THE FAB VENDOR SUPPLIED STACK-UP
IF ANY IMPEDANCE IS NOT FOUND ON A SPECIFIC LAYER, PLEASE IGNORE IT

22

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
⊗	100.0	+2.0/-2.0	NON-PLATED	1
+	8.0	+0.0/-8.0	PLATED	1832
⊗	8.1	+0.0/-8.1	PLATED	164
⑫	26.0	+2.0/-2.0	PLATED	20
㉔	35.0	+2.0/-2.0	PLATED	48
④	40.0	+2.0/-2.0	PLATED	4
④	40.0	+3.0/-3.0	PLATED	30
⑦	33.0x26.0	+3.0/-3.0	PLATED	2
⑤	59.0x32.0	+3.0/-3.0	PLATED	2
▭	111.0x32.0	+2.0/-2.0	PLATED	3
▭	122.0x32.0	+2.0/-2.0	PLATED	2

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL MEET THE RoHS COMMISSION DELEGATED DIRECTIVE (EU) 2015/863 OF 31 MARCH 2015 AMENDING ANNEX II TO DIRECTIVE 2011/65/EU. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL NOT CONTAIN ANY OF THE SUBSTANCES OF VERY HIGH CONCERN (SVHC) ABOVE THE THRESHOLD VALUE PER THE CURRENT ECHA LIST OF SVHC AND WITH ANNEX XVII OF REACH DIRECTIVE. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±0-30'
.XXX ±.005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

___ COMPANY PUBLIC
_X_ COMPANY INTERNAL
___ COMPANY CONFIDENTIAL

PART NO. 170-50702

APPROVALS	DATE
DRAWN EDUARDO LOPEZ	08-24-21
CHECKED JEEVANANTH C.	08-24-21
DESIGN ENGINEER ANTONIO QUIROZ	08-24-21

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
X-KW45B41Z-LOC

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-50702	FAB-50702	A

SCALE 1/1 | DO NOT SCALE DRAWING | SHEET 1 OF 2

ART FILE - fab.art

NOTES (UNLESS OTHERWISE SPECIFIED):

ZONE	REV	DESCRIPTION	DATE	APPROVED DE	APPROVED PE	APPROVED CAD
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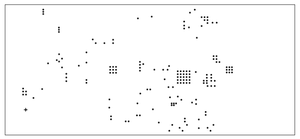
	B	SECOND RELEASE	05-25-22	A.Q.	J.C.	E.L.
	C	THIRD RELEASE	02-02-23	A.Q.	J.C.	E.L.

(22) THIS FAB_VIAFILL.ART SHOWS LOCATIONS OF VIA-IN-PAD TO BE FILLED.



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UNLESS OTHERWISE SPECIFIED
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D	LAY-50702	FAB-50702	A

SCALE 1/1 | DO NOT SCALE DRAWING | SHEET 2 OF 2