REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	02-19-21	D.V.
	B	CHANGES PER ECO141058	02-19-21	D.V.

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE. WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .005"/.005"

7. PLATING FINISH: A. BOTH SIDES ENIG: TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
   GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
   TYPE: LPI OR EQUIVALENT.
   A. LOCATION = +/-.002" OF PLATED PADS.
   B. DIAMETER OR SIZE = +/-.002 OF ORIGINAL DATA

10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.

11. ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

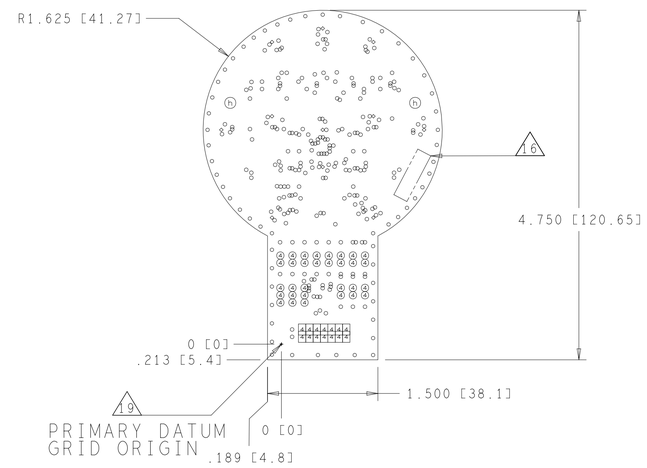
17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (PB)

18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.

20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

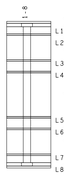
21. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS, KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
○	10.0	+0.0/-10.0	PLATED	250
○	18.0	+0.0/-18.0	PLATED	58
④	40.0	+3.0/-3.0	PLATED	31
⊡	41.0	+3.0/-3.0	PLATED	14
◇	15.0	+2.0/-2.0	NON-PLATED	11
ⓝ	250.0	+2.0/-2.0	NON-PLATED	2

8

DETAIL A
LAYER STACKUP
SCALE: NONE



★ SURFACE - AIR 0 MIL
★ DIELECTRIC - DRY FILM MASK 0.8 MIL
L1 TOP CONDUCTOR - 1OZ COPPER 1.4 MIL
L2 L2_GND_1 PLANE - 1/2OZ_COPPER 0.63 MIL
★ DIELECTRIC - FR-4 10 MIL

L3 L3_INNER_1 CONDUCTOR - 1/2OZ_COPPER 0.63 MIL
★ DIELECTRIC - FR-4 4.13 MIL
L4 L4_PWR_1 PLANE - 1/2OZ_COPPER 0.63 MIL

★ DIELECTRIC - FR-4 18 MIL

L5 L5_PWR_2 PLANE - 1/2OZ_COPPER 0.63 MIL
★ DIELECTRIC - FR-4 4.13 MIL
L6 L6_INNER_2 CONDUCTOR - 1/2OZ_COPPER 0.63 MIL
★ DIELECTRIC - FR-4 10 MIL

L7 L7_GND_2 PLANE - 1/2OZ_COPPER 0.63 MIL
★ DIELECTRIC - FR-4 0.8 MIL
L8 BOTTOM CONDUCTOR - 1/2OZ_COPPER 1.4 MIL
★ DIELECTRIC - DRY FILM MASK 0.8 MIL
★ SURFACE - AIR 0 MIL

DESIGN CROSS SECTION CHART
TOTAL THICKNESS 60.38 MIL
BOARD THICKNESS TOLERANCE +/-10%

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

LAYERS	SE		
	TRACE WIDTH	IMPEDANCE	REFERENCE LAYER
L1_PS	5.00	50.00	2
L3_INNER_1	5.00	50.00	2,4
L6_INNER_2	5.00	50.00	5,7
L8_SS	5.00	50.00	7

PART NO. 170-48278

___ COMPANY PUBLIC
_X_ COMPANY INTERNAL
___ COMPANY CONFIDENTIAL

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±0-30°
.XXX ±.005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN W.MEAD	08-13-21
CHECKED DELEEP VADLAMUDI	08-13-21
DESIGN ENGINEER AL MORROW	08-13-21

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD 8CH-DMIC

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-48278	FAB-48278	B

SCALE 1/1 | DO NOT SCALE DRAWING | SHEET 1 OF 1