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Revision History

Rev.	Date	Description
X1	2021.2.11	Preliminary schematic
A	2021.2.25	Rev A Release. Change J1, Updated U35 part number, Change VDD_1V8 to VDD Updated System Block Diagram to match
AX1	2021.07.16	Rev AX1 update - changed J5 and added J14 and J15 to allow more flexibiltiy in setting Clk / Data combinations
B	2021.08.17	Rev B Release

8CH DMIC

GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC

2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.

3. Interrupted lines coded with the same letter or letter combinations are electrically connected.

4. Device type number is for reference only. The number varies with the manufacturer.

5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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Designer: Al Morrow	Drawing Title: 8CH-DMIC		
Drawn by: Al Morrow	Page Title: TITLE PAGE		
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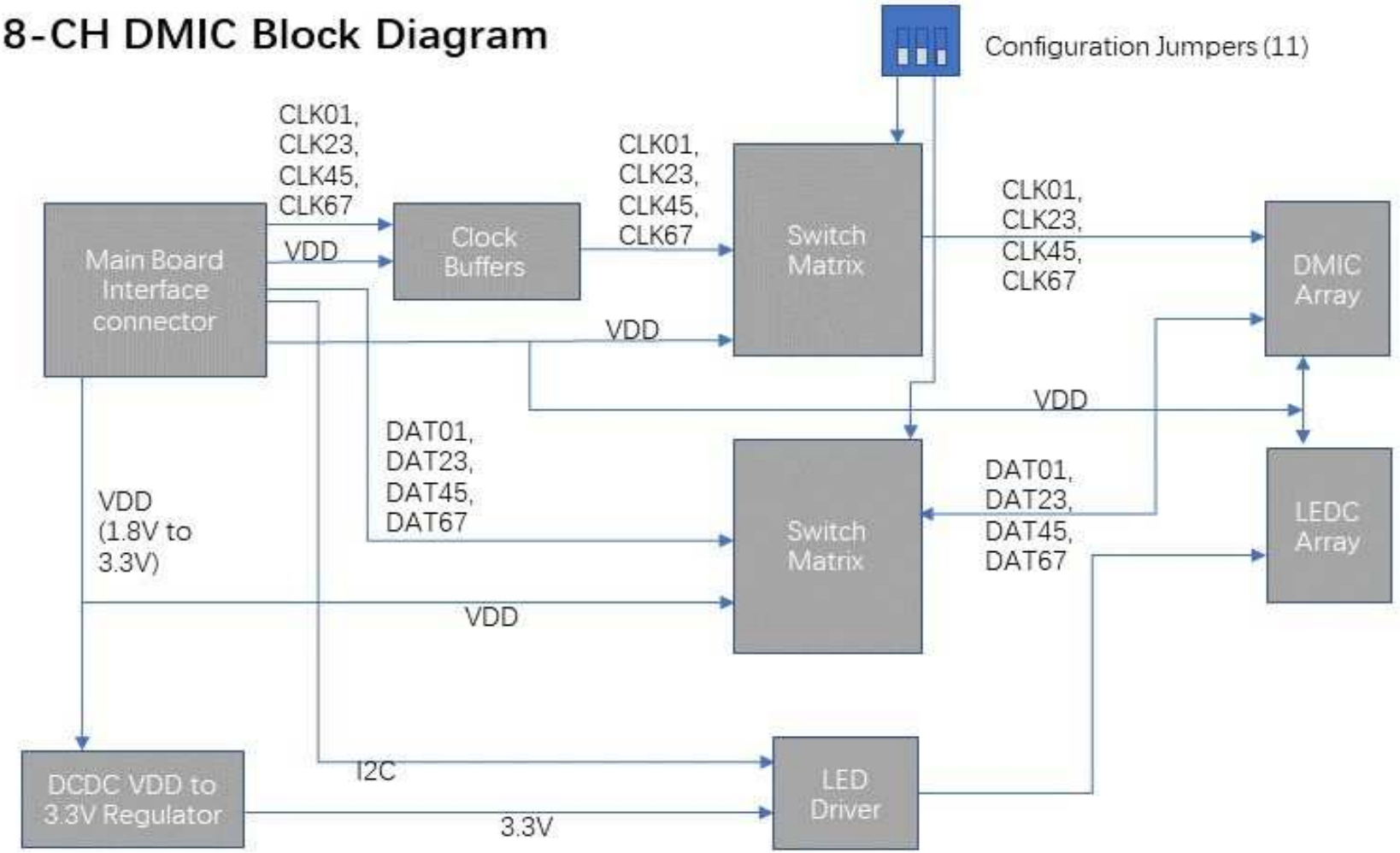
8-CH DMIC Block Diagram



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Drawing Title:	8CH-DMIC		
Page Title:	BLOCK DIAGRAM		
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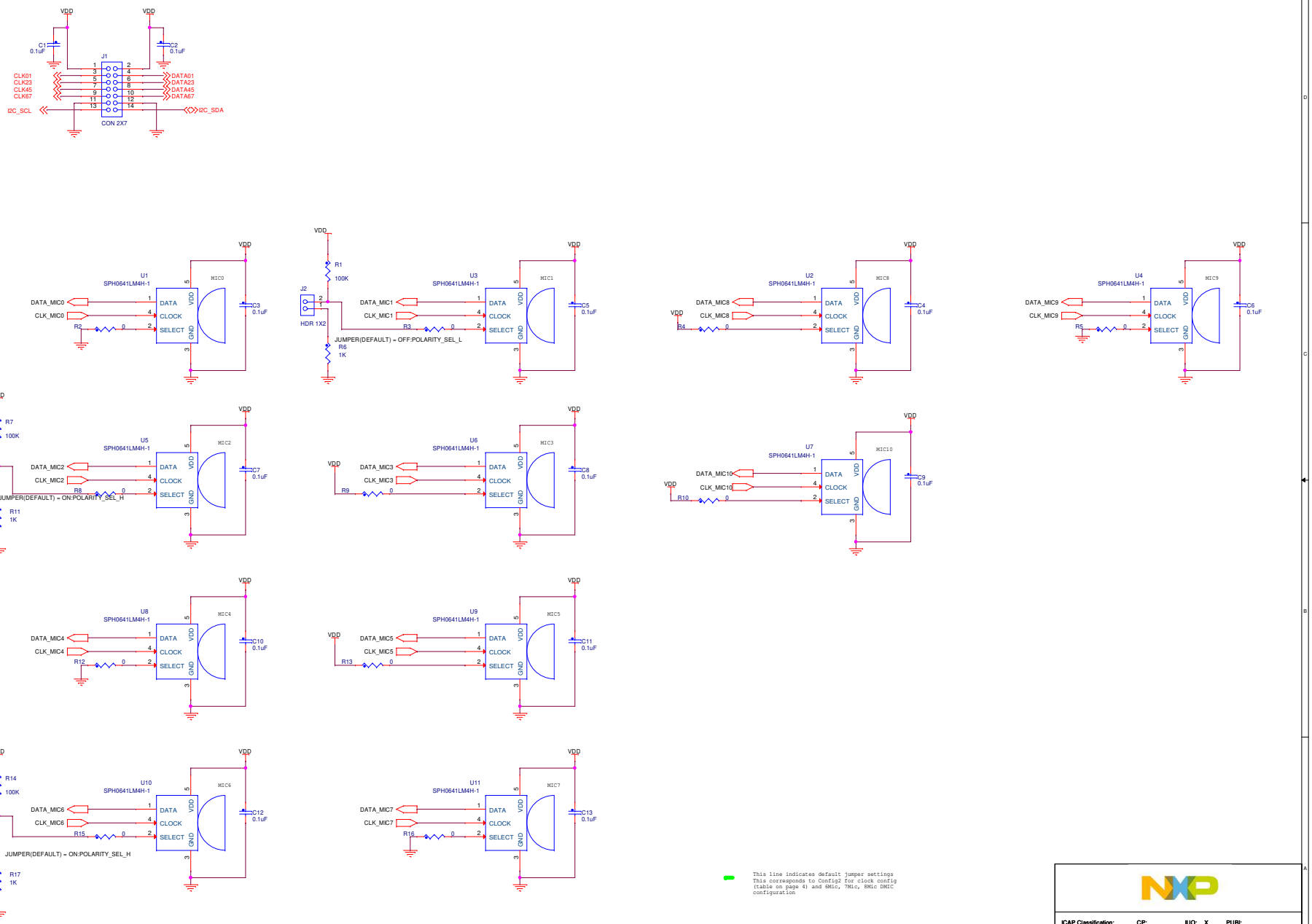
VDD
C1 0.1uF
C2 0.1uF
J1
CON 2X7
CLK01
CLK23
CLK45
CLK67
DATA01
DATA23
DATA45
DATA67
I2C_SCL
I2C_SDA
U1 SPH0641LM4H-1
MIC0
DATA_MIC0
CLK_MIC0
R2 0
C3 0.1uF
R1 100K
J2
HDR 1X2
R6 1K
U3 SPH0641LM4H-1
MIC1
DATA_MIC1
CLK_MIC1
R3 0
C5 0.1uF
JUMPER(DEFAULT) = OFF:POLARITY_SEL_L
U2 SPH0641LM4H-1
MIC8
DATA_MIC8
CLK_MIC8
R4 0
C4 0.1uF
U4 SPH0641LM4H-1
MIC9
DATA_MIC9
CLK_MIC9
R5 0
C6 0.1uF
R7 100K
J3
HDR 1X2
R8 0
R11 1K
JUMPER(DEFAULT) = ON:POLARITY_SEL_H
U5 SPH0641LM4H-1
MIC2
DATA_MIC2
CLK_MIC2
C7 0.1uF
U6 SPH0641LM4H-1
MIC3
DATA_MIC3
CLK_MIC3
R9 0
C8 0.1uF
U7 SPH0641LM4H-1
MIC10
DATA_MIC10
CLK_MIC10
R10 0
C9 0.1uF
U8 SPH0641LM4H-1
MIC4
DATA_MIC4
CLK_MIC4
R12 0
C10 0.1uF
U9 SPH0641LM4H-1
MIC5
DATA_MIC5
CLK_MIC5
R13 0
C11 0.1uF
R14 100K
J4
HDR 1X2
R15 0
R17 1K
JUMPER(DEFAULT) = ON:POLARITY_SEL_H
U10 SPH0641LM4H-1
MIC6
DATA_MIC6
CLK_MIC6
C12 0.1uF
U11 SPH0641LM4H-1
MIC7
DATA_MIC7
CLK_MIC7
R16 0
C13 0.1uF
DATA
CLOCK
SELECT
VDD
GND
This line indicates default jumper settings
This corresponds to Config2 for clock config
(table on page 4) and 6Mic, 7Mic, 8Mic DMIC
configuration
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8CH-DMIC
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INTERFACE AND MIC ARRAY
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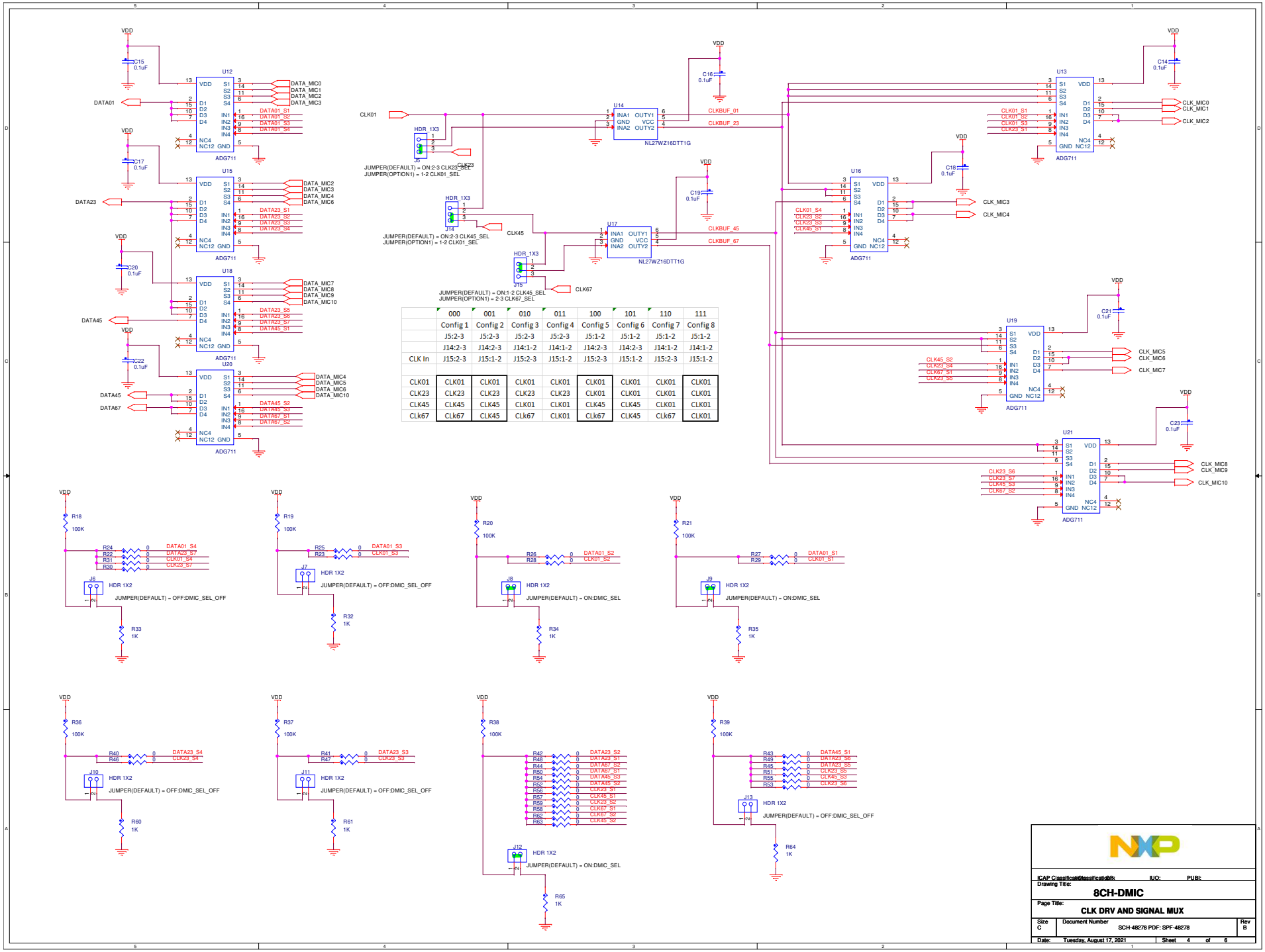

	000	001	010	011	100	101	110	111
	Config 1	Config 2	Config 3	Config 4	Config 5	Config 6	Config 7	Config 8
	J5:2-3	J5:2-3	J5:2-3	J5:2-3	J5:1-2	J5:1-2	J5:1-2	J5:1-2
	J14:2-3	J14:2-3	J14:1-2	J14:1-2	J14:2-3	J14:2-3	J14:1-2	J14:1-2
CLK In	J15:2-3	J15:1-2	J15:2-3	J15:1-2	J15:2-3	J15:1-2	J15:2-3	J15:1-2
CLK01	CLK01	CLK01	CLK01	CLK01	CLK01	CLK01	CLK01	CLK01
CLK23	CLK23	CLK23	CLK23	CLK23	CLK01	CLK01	CLK01	CLK01
CLK45	CLK45	CLK45	CLK01	CLK01	CLK45	CLK45	CLK01	CLK01
CLK67	CLK67	CLK45	CLK67	CLK01	CLK67	CLK45	CLK67	CLK01

ICAP Classification:	IUO:
Classification:	PUBI:
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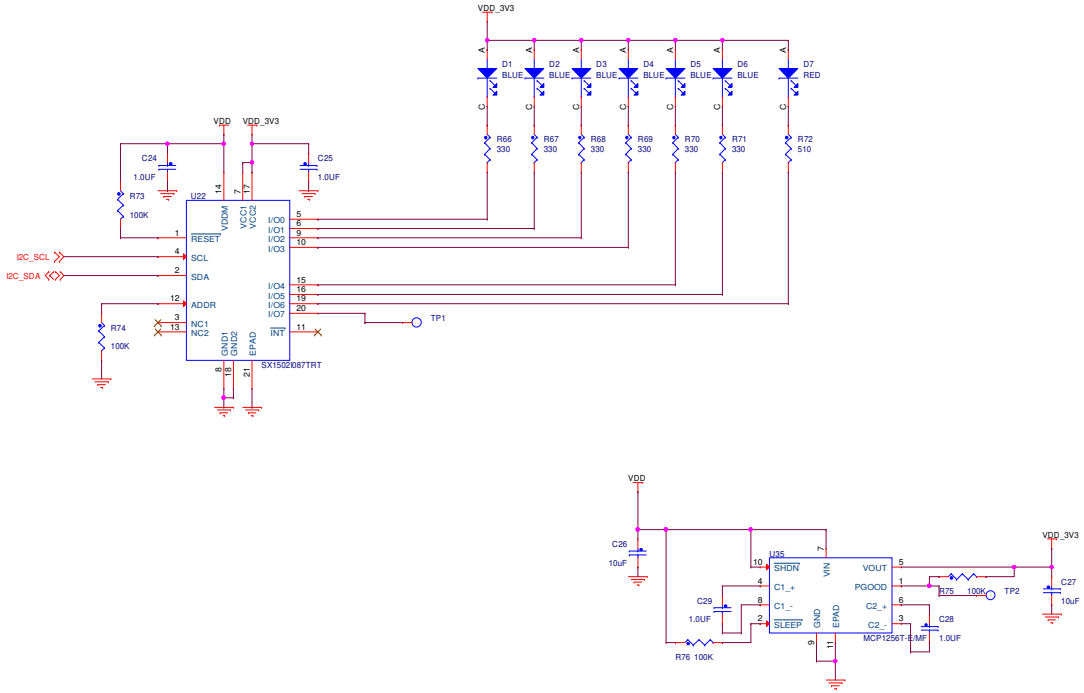

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REF DES	JUMPER(DEFAULT)	JUMPER(OPTION1)	PAGE NAME
J2	OFF:POLARITY_SEL_L		003: Interface and Mic Array
J4,J3	ON:POLARITY_SEL_H		003: Interface and Mic Array
J10,J7,J13,J11,J6	OFF:DMIC_SEL_OFF		004: Clk Drv and Signal MUX
J15	ON:1-2 CLK45_SEL	2-3 CLK67_SEL	004: Clk Drv and Signal MUX
J5	ON:2-3 CLK23_SEL	1-2 CLK01_SEL	004: Clk Drv and Signal MUX
J14	ON:2-3 CLK45_SEL	1-2 CLK01_SEL	004: Clk Drv and Signal MUX
J9,J8,J12	ON:DMIC_SEL		004: Clk Drv and Signal MUX

6Mic, 7Mic, 8Mic	J3	J4	J8	J9	J12	
2Mic, 3MicA, 3MicC			J6	J9	J10	
3MicB, 4MicA			J7	J9	J10	J11
4MicB, 5Mic	J2		J7	J8	J13	

```
Single: Any
2MIC- 0 - 3  (70mm)
3MICA: 0, 3, 9
3MICB: 0, 2, 4 (62mm)
3MICC: 0, 3, 6
4MICA: 0-2-4 + 6
4MICB: 1-2-7-8 (35mm)
5MIC: 1-2-7-8 + 10
6MIC: 0-1-2-3-4-5 (62mm)
7MIC: 0-1-2-3-4-5, 6
8MIC: 0-1-2-3-4-5, 6 + 10
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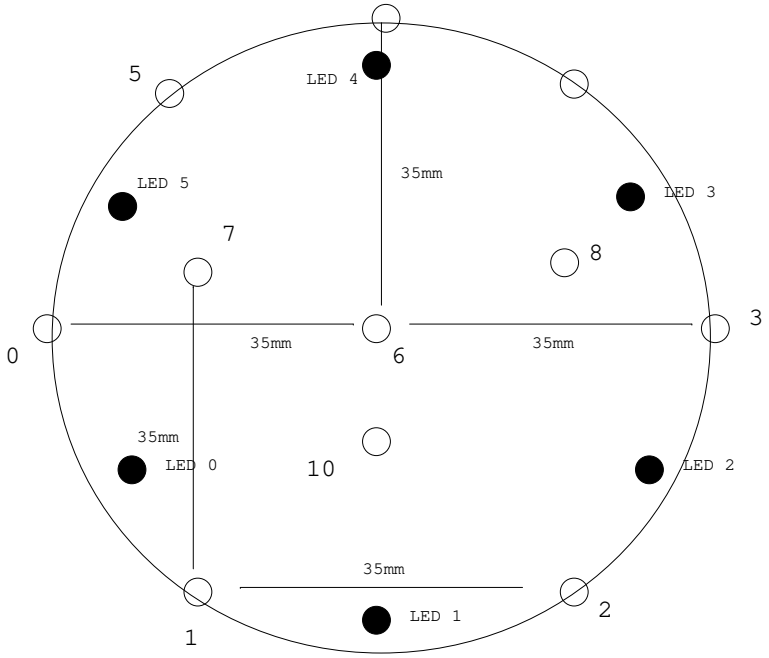

ICAP Classification:	CP:	IUO: X	PUBI:
Drawing Title:	8CH-DMIC		
Page Title:	Mechanical		
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