i.MX Applications Processors automotive roadmap and overview featuring the i.MX 95

车用i.MX系列路线图与i.MX 95亮点简介

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INTELLIGENT EDGE

75 BILLION
SMART CONNECTED DEVICES BY 2030

1999 — 2009 — 2020 — 2030

~$150 BILLION
Total semiconductors

~$250 BILLION
Total semiconductors

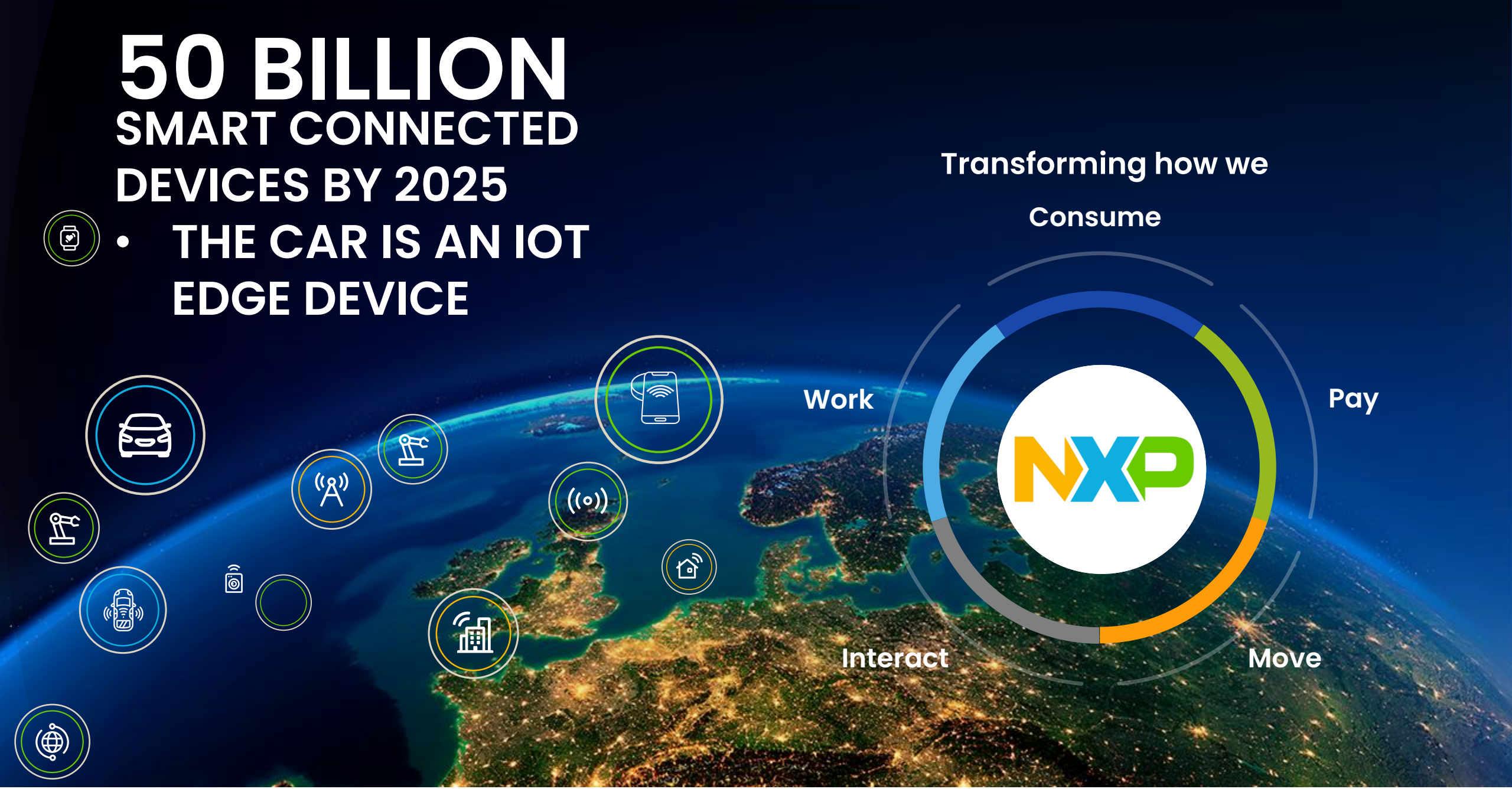
~$550 BILLION
Total semiconductors

~$1 TRILLION
Total semiconductors

Source: IDC, Gartner, NXP

50 BILLION
SMART CONNECTED DEVICES BY 2025

- THE CAR IS AN IOT EDGE DEVICE



Automotive market dynamics

Greener

- The BEV switchover
- Getting to carbon-neutral

Safer & secure

- FuSa becoming more important in the cockpit
- Cybersecurity
- Privacy & data protection

Edge processing

- Software-defined vehicle
- Cloud-native apps
- Subscription model

i.MX 9 Series of Applications Processors
adding to NXP's portfolio

Software Compatible

Pin-to-pin Compatible

- i.MX 6QuadPlus
- i.MX 6Quad
- i.MX 6DualPlus
- i.MX 6Dual
- i.MX 6DualLite
- i.MX 6Solo
- i.MX 6SoloX
- i.MX 6SoloLite
- i.MX 6SLL
- i.MX 6UltraLite
- i.MX 6ULL
- i.MX 6ULZ

Arm® v7-A

A9 | A9 M4 | A7

i.MX 8 Family
Advanced graphics, vision & performance
A72 A53 M4

i.MX 8M Family
General purpose Edge processing
A53 M4/M7 NPU

i.MX 8ULP Family
Ultra low power with graphics
A35 M33

i.MX 8X Family
Safety certifiable & efficient performance
Arm® v8-A (32-bit/64-bit)
A35 M4

i.MX 7 Family
Flexible efficient connectivity
A7 M4

i.MX 7ULP Family
Ultra Low Power with Graphics
Arm v7-A (32-bit)
A7 M4

i.MX 95 Family
ML Vision, Safety Enabled Platforms, HMI, Powerful Android/Linux Platforms
FuSa A55 M33 M7 NPU ISP GPU

i.MX 93 Family
Automotive & Industrial Vision, Industrial HMI, IoT Smart Appliances, Gateways
A55 M33 NPU

i.MX 91 Family
Secure Linux Controller Platforms, IoT & Industrial RTOS, Connected IoT & Industrial
A55

Future i.MX 9 Families
Scalable Platform
Arm v8.2-A (32-bit/64-bit)

Scalable Software

Winning in connected cockpits with full system solutions

NXP i.MX Auto Families

Fully Scalable Apps Processor Family

Designed in at 19 of top 20 OEMs

i.MX 8/9 SoCs: Simplifying Cockpit Applications

Up to 4K resolution

Cockpit | Multimedia | Media Source

NXP Car DSP Family

Radio/Audio Car DSPs and 1-Chips

Designed in at 20 of top 20 OEMs

Software defined radio: 6 ICs into 1

Advanced audio processing

Radio | Audio

NXP Wireless Connectivity

Wi-Fi and Bluetooth Solutions

Designed in at 14 of top 20 OEMs

Wi-Fi 6 and Bluetooth 5 / BLE

2x2 Combo Solutions

Wireless Connectivity

NXP Audio Amplifier

Scalable advanced Audio Amplifiers

Designed in at 15 of top 20 OEMs

Class D Audio Amplifiers

Amplifier

Power Management Solutions

i.MX 95 Family enables edge platforms with AI, safety and connectivity

Differentiated, scalable platforms designed for the next-generation of edge processing with safety, security and accelerated performance

- AI/ML accelerated by NXP eIQ® Neutron NPU
- Premium Graphics powered by Arm® Mali™ GPU
- Vision Processing enabled by new NXP ISP
- Real-time and Safety Domains designed for ASIL-B/SIL 2 compliant platforms
- Connectivity and expandability: 10GbE, PCIe®, USB 3
- EdgeLock® Secure Enclave + V2X Cryptographic Acceleration

Targeting edge uses such as:

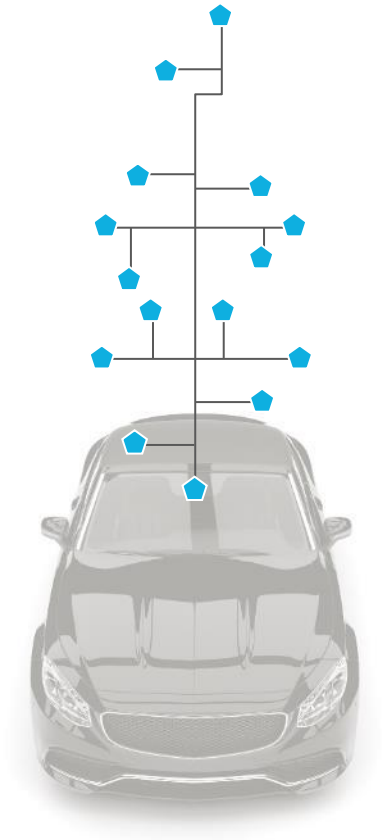
- Automotive Edge eCockpit and Connectivity domains;
- Industry 4.0 automation, control, and HMI;
- IoT smart home/appliance/office, and more!

Build with NXP portfolio of wireless connectivity, and NXP power management solutions, to simplify platform design, integration, and adoption.

General availability expected 1H25

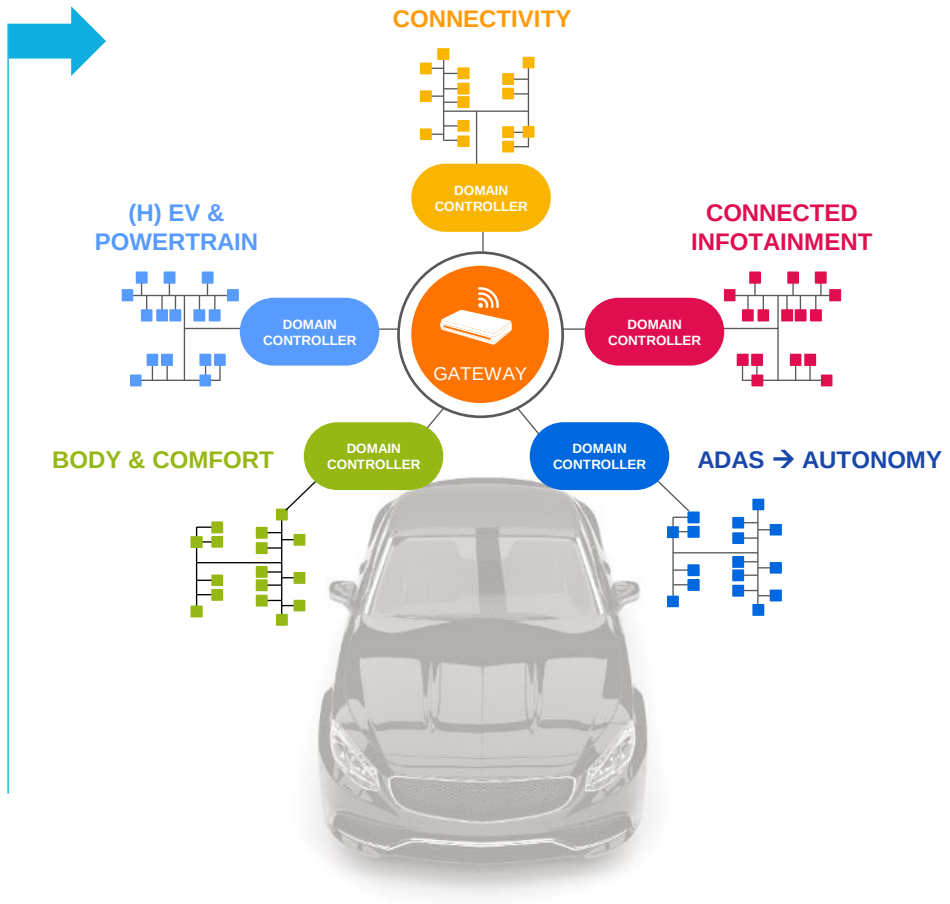
- Alpha & Beta Program details to follow

Vehicle architecture transformation



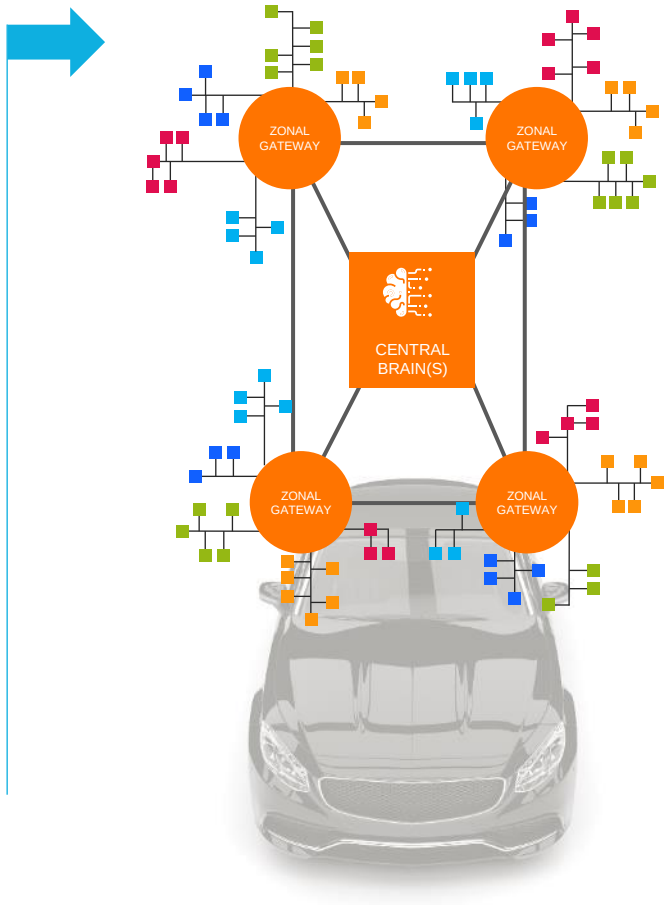
Today | flat

Unfit to future mobility



Logical restructure | domains

Enabling autonomous car



Physical restructure | zones

Enabling user-defined car

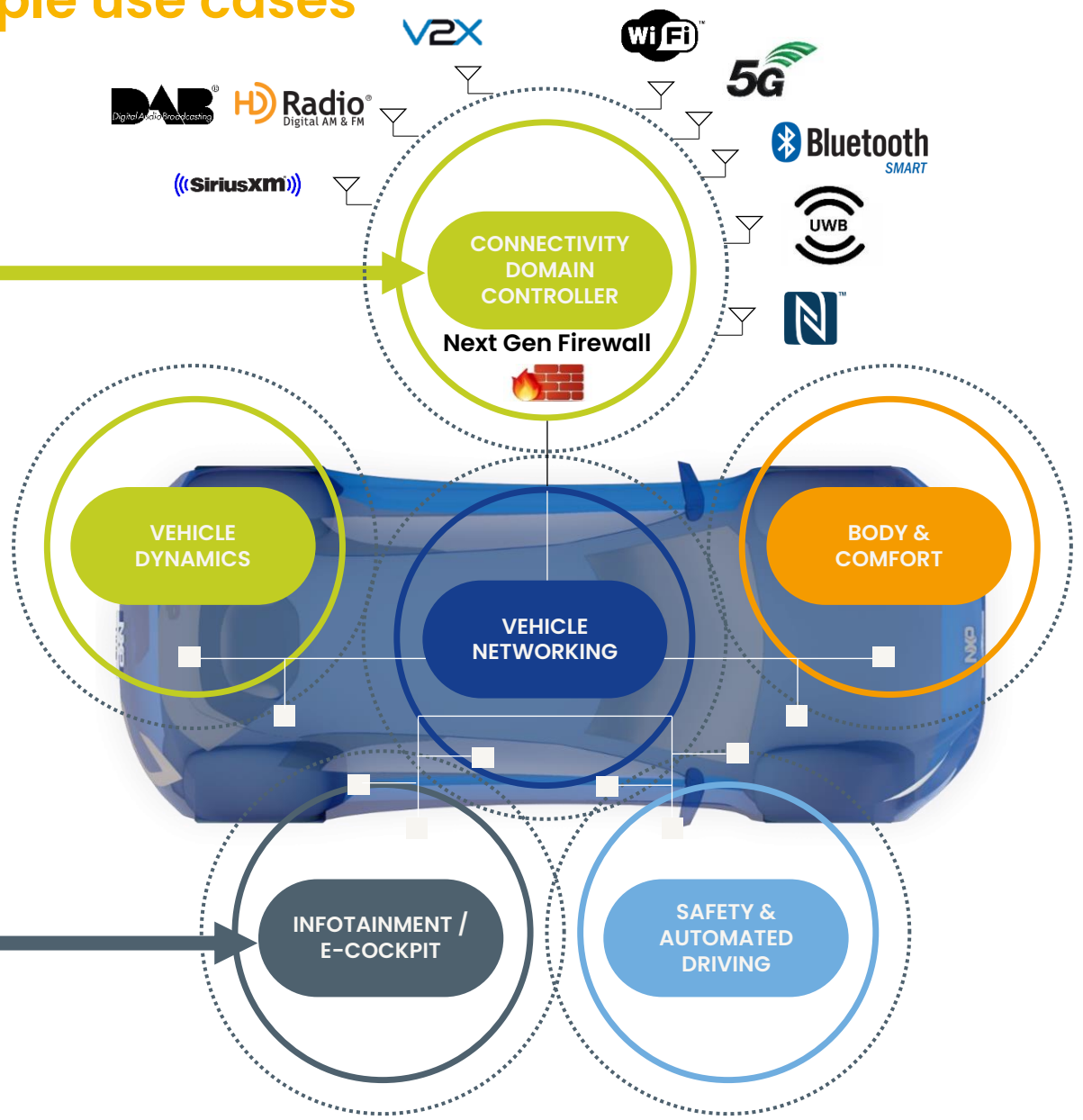
i.MX 95 Family automotive edge example use cases

Connectivity domain controller

- Consolidates all external wireless interfaces in one domain managed by single high-performance processor, providing vehicle network interfaces
  - Security - consistent security policy and state-of-art IPS filtering applied to all wireless data entering the car
  - Cloud-managed – over-the-air SW updates for connectivity, orchestrated from the cloud
  - Modular – provides a modular connectivity subsystem for zonal car architecture

eCockpit in-vehicle infotainment & digital cluster

- Integrates real time capabilities into single platform to lower power and reduce system cost
  - Safety - safe rendering of tell-tales, audio, rear-view camera, offloaded from main application cores
  - Integration – value-added functions such as driver/occupant monitoring, surround view park assist, navigation, and in-car architecture



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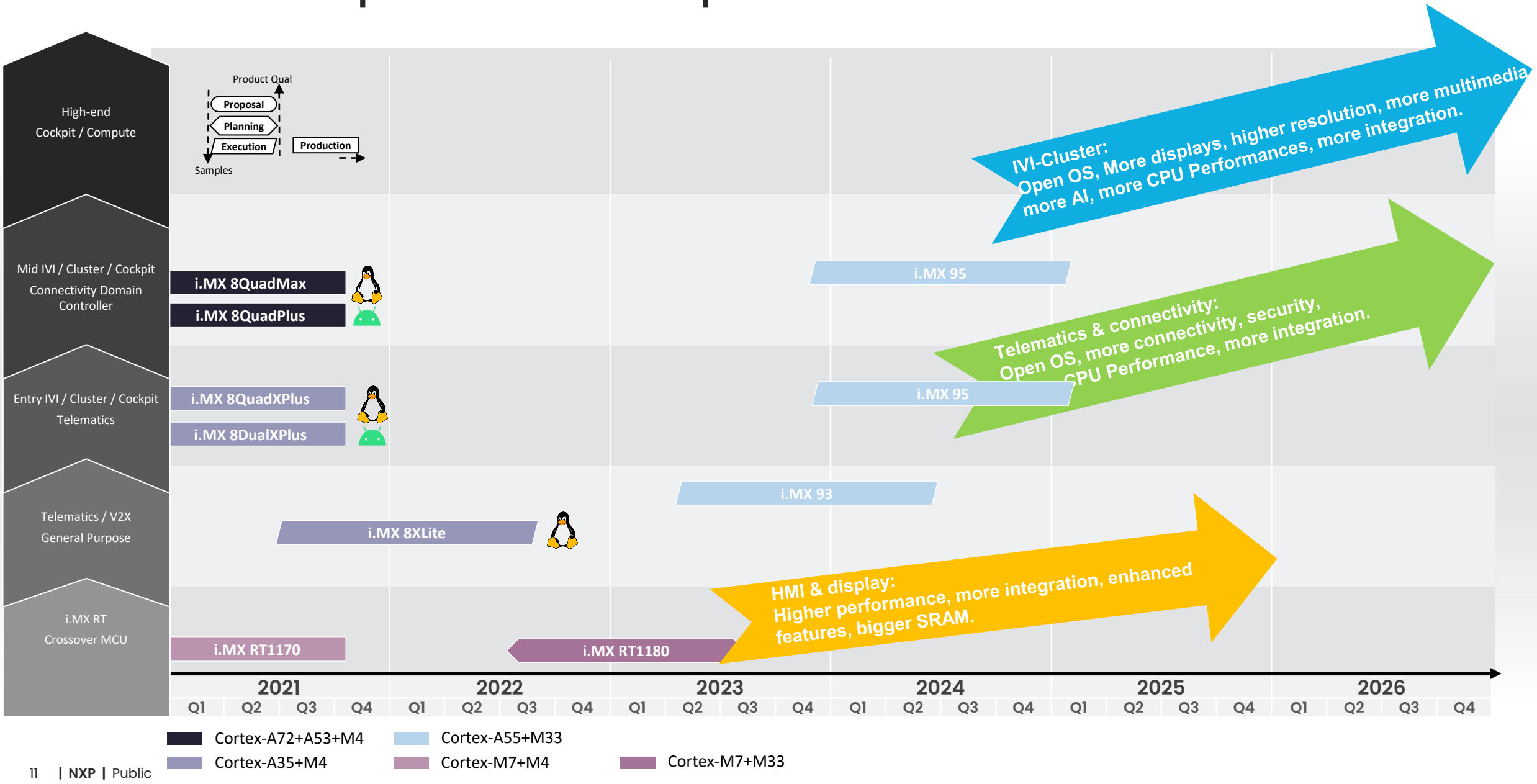
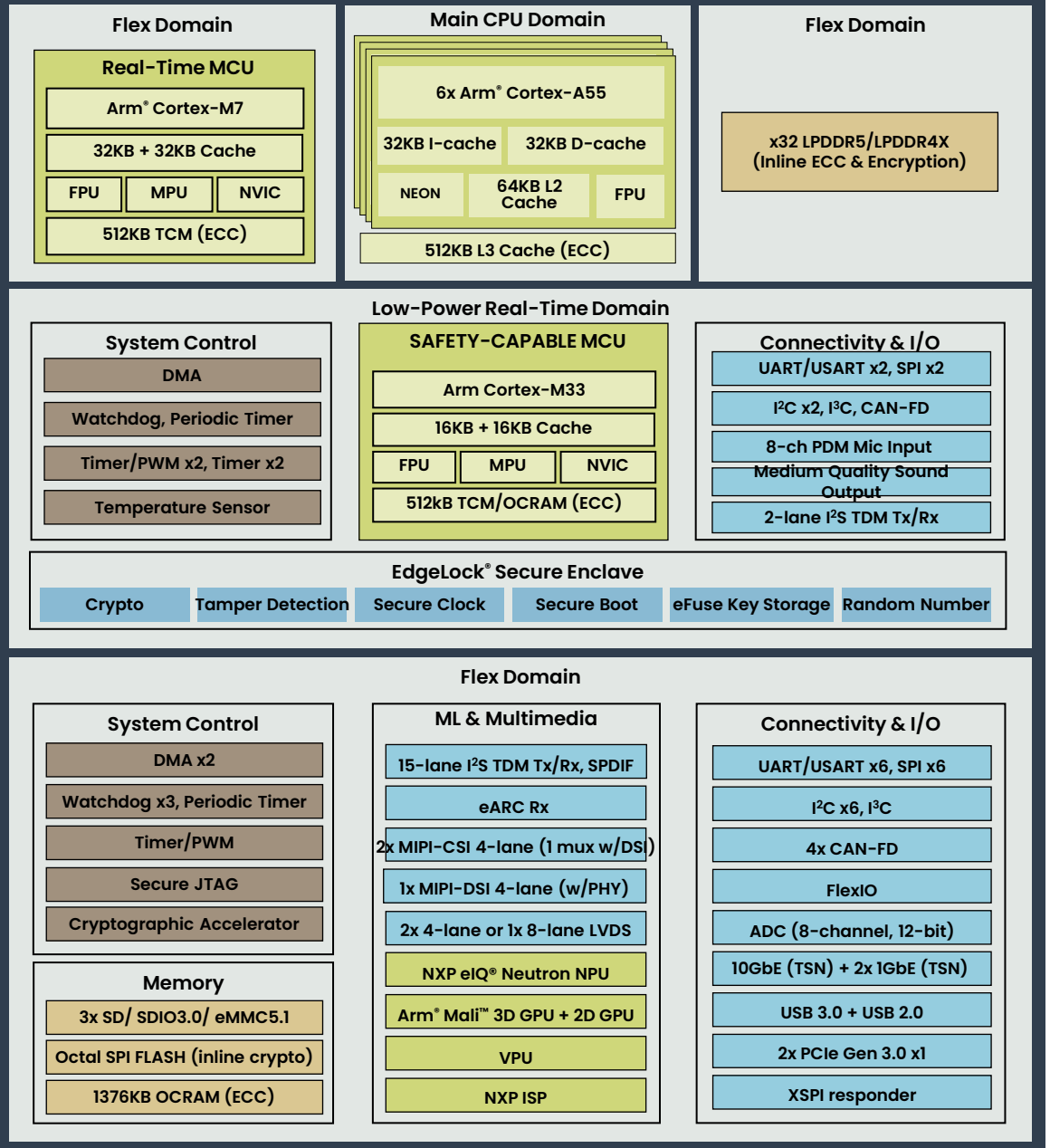
i.MX 95 Family overview

i.MX automotive processor roadmap





*Depopulated array or hybrid sphere placement allow PCB routing technologies normally reserved for larger pitch packages, e.g., standard plated through-hole (PTH) PCB that may not require micro-via, laser-drill, HDI blind or buried vias, or via in pad

i.MX 95 Applications Processor Family

- **Application Domain**: **6x Arm® Cortex™-A55** @ Up to 2.0 GHz (Arm v8.2 64-bit capable)
- **Real-Time Domains**: **1x Cortex-M7** @ 800 MHz, 32KB + 32KB Cache (ECC) w/512KB TCM SRAM (ECC)
  - **1x Arm Cortex-M33** @ 333 MHz, 16KB + 16KB cache (ECC) w/ 512KB TCM SRAM (ECC)
    - Arm v8-M supporting TrustZone-M

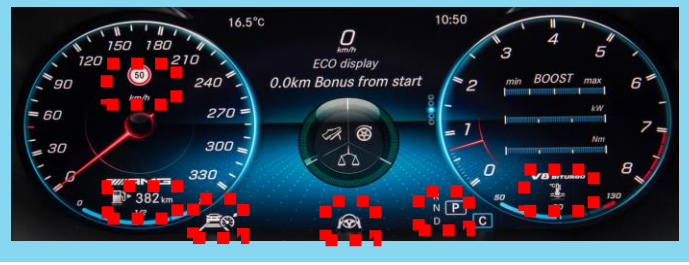
Feature Highlights

- **Safety**: NXP **SafeAssure® for ISO 26262 ASIL-B** & **IEC 61508 SIL-2** compliant platforms
- **Machine Learning**: **NXP eIQ® Neutron NPU**
- **Security**: **EdgeLock® Secure Enclave + V2X Cryptographic Accelerator**
- **Internal Memory**: 1376KB SRAM
- **External Memory**: **Up to 6.4 GT/s x32 LPDDR5/4X (Inline ECC & inline memory encryption)**
  - 3x SD 3.0/ SDIO3.0/ eMMC5.1
  - 1x Octal SPI, including support for SPI NOR and SPI NAND memories
- **3D Graphics**: **Arm® Mali™ G310 GPU** (OpenGL® ES 3.2, Vulkan ® 1.2, OpenCL 3.0)
- **Display Controllers** (up to 3 simultaneous displays):
  - 1x 333Mpixel/s MIPI-DSI (4-lane, 2.5 Gbps/lane) supporting 4K30 or 3840x1440P60 display resolution
  - Up to 1080P60 LVDS Tx (2x 4-lane or 1x 8-lane)
- **Camera & Image Signal Processing**: **NXP ISP with RGB-IR support**
  - Up to 500 Mpixel/s throughput MIPI-CSI (2x 4-lane, 2.5 Gbps/lane) with PHY (1 mux with DSI)
  - Up to 2x4K30, 4x1080P60, or 8x1080P30 cameras with MIPI virtual channels
- **Video Processing**:
  - 4K60 H.265/H.264 decode or encode (4K30 H.265/H.264 simultaneous encode & decode)
  - up to 32 streams
- **Audio**: 17-lane I²S TDM (32-bit @ 768 KHz), SPDIF Tx/Rx, eARC Rx
  - 8 channel PDM microphone input + MQS: Medium Quality Sound output
- **Connectivity & I/O**: **2x PCIe Gen 3.0 (1-lane)**
  - **1x10GbE + 2x Gb Ethernet (w/TSN);** AVB & IEEE 1588 for sync; and EEE
  - 1x USB 3.0 Type C with PHY, 1x USB 2.0 with PHY
  - 5x CAN-FD
  - 8x UART/USART/Profibus, 8x I2C, 8x SPI, 2x I3C, XSPI responder
  - 1x 8-ch, 12-bit ADC
  - 2x 32-pin FlexIO interfaces (bus or serial I/O)
- **Package**:
  - Large: 19x19 mm FCBGA 0.7 mm pitch, de-populated array* (AEC-Q100 G2)
  - Small: 15x15 mm FCBGA 0.5 mm pitch, de-populated array*
- **OS targets**: Linux®, Android™, FreeRTOS
- **Qualification**: Auto / Ext. Industrial (-40C to +125C) / Consumer (Tj=0C to +95C)

i.MX processor automotive target applications

Cluster and Infotainment

- Low/mid eCockpit
- Standalone infotainment
- Standalone cluster



Telematics and Connectivity

- Low to high Telematics
- Smart Antenna systems
- Connectivity Domain Controllers

Display and HMI

- DMS / OMS
- Standalone touch / displays
- MCU expansion (off-chip memory)

i.MX 9 series objectives for low-mid eCockpit solutions

1. Reduce system cost
   - Integrated real-time MCU
   - Comprehensive connectivity
   - Support adjacent use-cases e.g. parking assistant

2. Enable state-of-the-art Functional Safety solutions
   - Integrated ASIL-B FuSa island
   - SafeAssure® software framework

3. Optimize performance and efficiency
   - Latest-generation multimedia cores
   - Scalable product families
   - Low-power modes for EV use-cases

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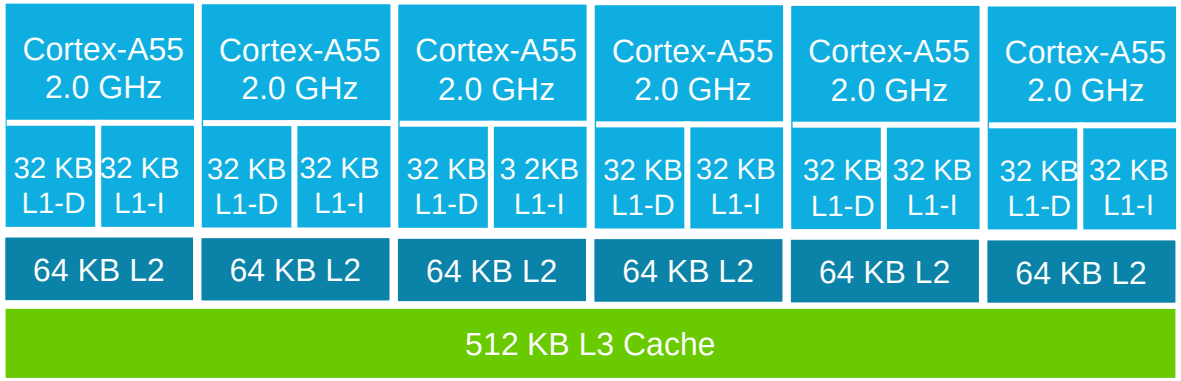
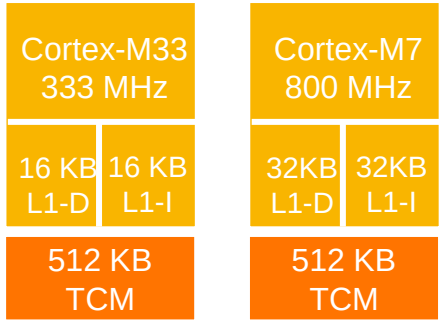
i.MX 95 SoC highlights

Technology inside the SoC

i.MX 95 CPU and on-chip memory

- Up to 6x Arm® Cortex™-A55 @ 2.0 GHz§
  - Single cluster ensures coherency across all cores
  - Each core has private L2 cache running at CPU speed
  - Total 896 KB L2+L3 caches
  - Independent frequency control of each core
- Cortex-M7 @ 800 MHz
  - High-performance real-time processing
- Cortex-M33 @ 333 MHz
  - Optimized for low-power, real-time processing
  - Can be configured as functional safety island





1376 KB On-chip SRAM*

* up to 1024KB may be used by NPU

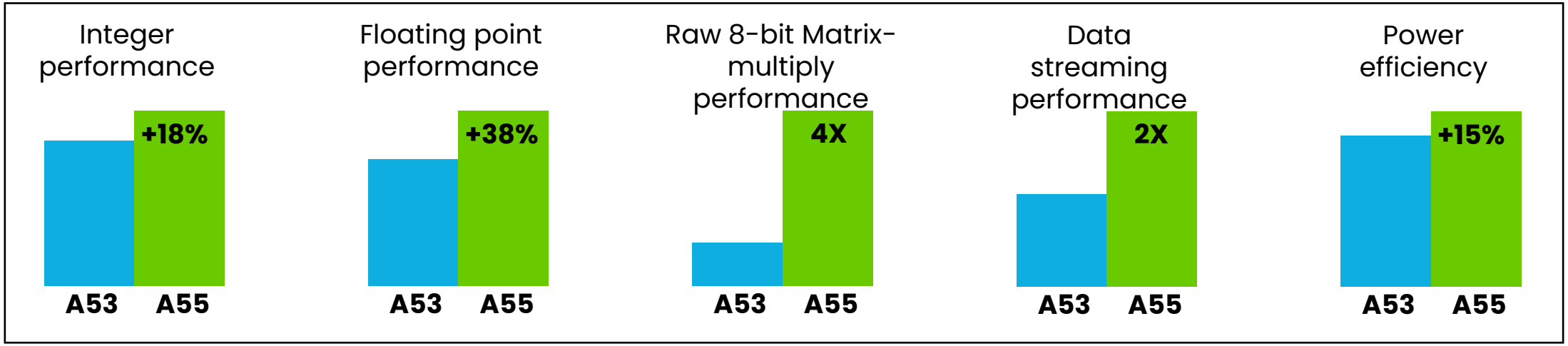
§ max 1.8GHz for Automotive

Arm® Cortex™-A55 highlights and improvements versus Cortex-A53

- A55 is Arm's most efficient 64-bit Cortex-A core
- A55 supports Arm's DynamIQ technology:
  - New dot-product instructions deliver Machine Learning performance up to 4X higher than A53
  - Up to 8-core, heterogeneous clusters
  - Per-core performance and power control
- Arm v8.2 ISA improves support for virtualization & reliability

A55 key architecture changes vs. A53

- Armv8.2 Instruction Set
  - Dot product & half-precision float (for ML)
  - Virtualized Host Extensions (for KVM)
  - Cache stashing & atomic operations
- 2nd 64-bit NEON/floating point unit
- Two-level branch prediction
- Double L1 data cache bandwidth
- Private L2 cache running at CPU speed
- Double TLB sizes



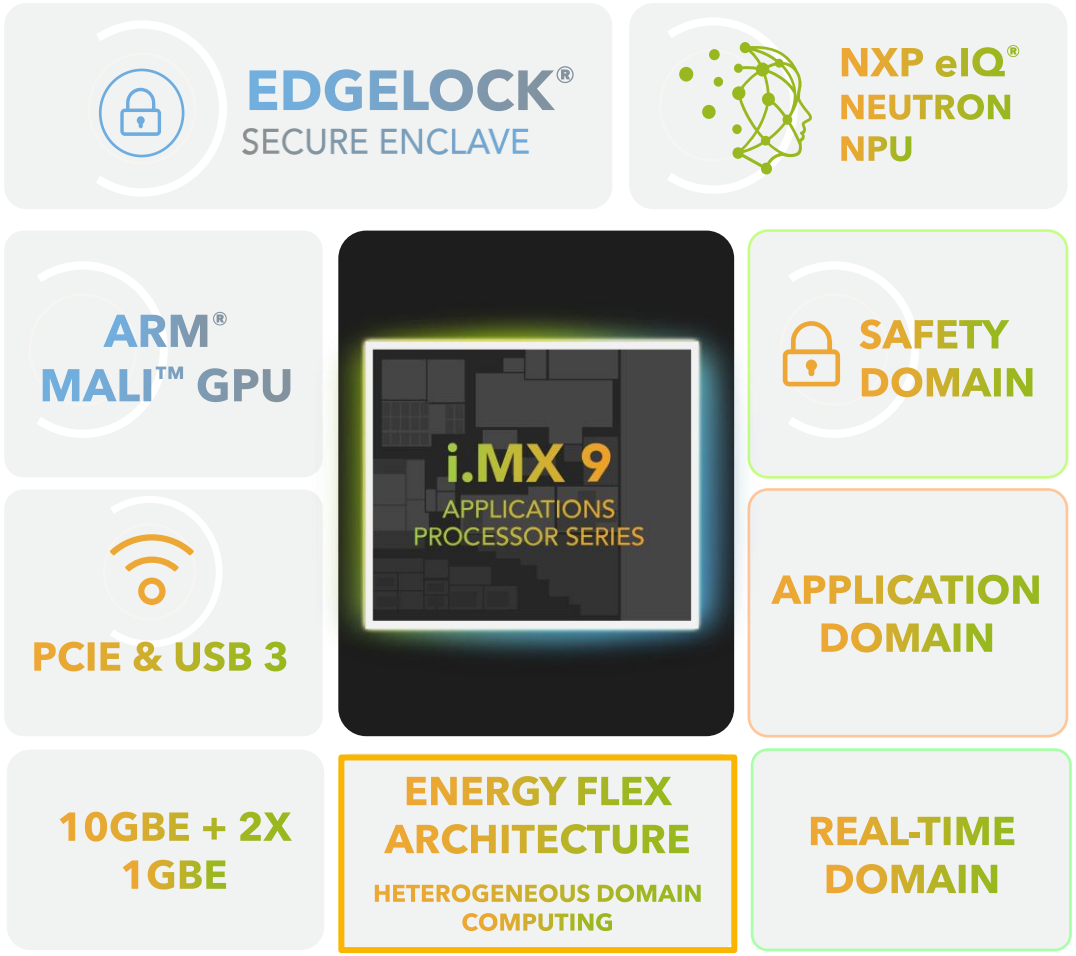
Energy Flex architecture with three compute domains

- Multiple power islands enable fine-grained control of dynamic power and low-power operating modes with large portion of SoC powered off
- Variable SoC Logic power supply and frequency control of processing cores for reduced power consumption under light load
- Support for multiple power power modes including suspend-to-DRAM (STR)

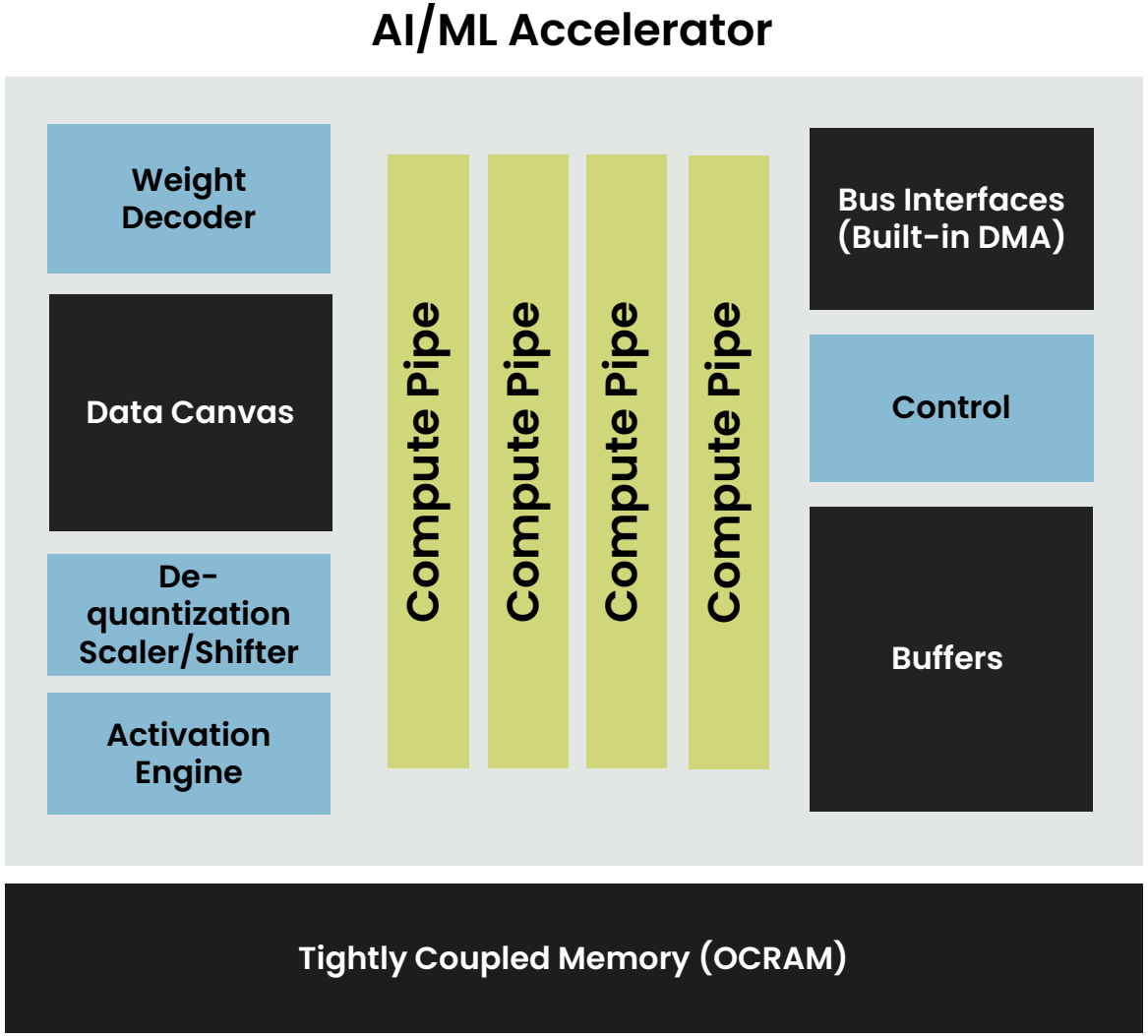
- **Up to 6x Arm® Cortex™-A55 @ Up to 2.0 GHz**
  - **Single cluster ensures coherency across all cores**
  - **Each core has private L2 cache running at CPU speed**
  - **Per Core L1 I/D & L2 Cache; Shared 512 KB L3 Cache**
  - **Independent frequency control of each core**

- **Arm Cortex-M7 @800 MHz**
  - **High-performance real-time processing domain**

- **Arm Cortex-M33 @333 MHz**
  - **Optimized for low-power System Manager**
  - **Enables Functional Safety domain**



i.MX 95 SoC: NXP eIQ® neutron Neural Processing Unit (NPU)



Single architecture with great scalability

- Optimized for performance and power efficiency
- ML solution development support with eIQ® ML SW Development Environment
  - Supports major NN structures (CNN, MLP, RNN, LSTM, TCN, and more)
- Internal development provides flexibility to tune solution to better meet our customer needs and the ability to provide ongoing support and generational improvements for changing applications and operator support needs
- Hardware scales from performance efficient 32 Ops/cycle to 2k Ops/cycle and beyond for portfolio coverage with a single architecture, and potential to provide future expansion
- Software support is unified over multiple generations and device portfolio, creating consistent enablement and support solutions for our customers

EDGELOCK®
SECURE ENCLAVE

Beyond crypto
Evolved on-die security with run-time attestation, silicon root of trust, trust provisioning, fine-grain key management augmented by extensive crypto services and simpler path to security certifications

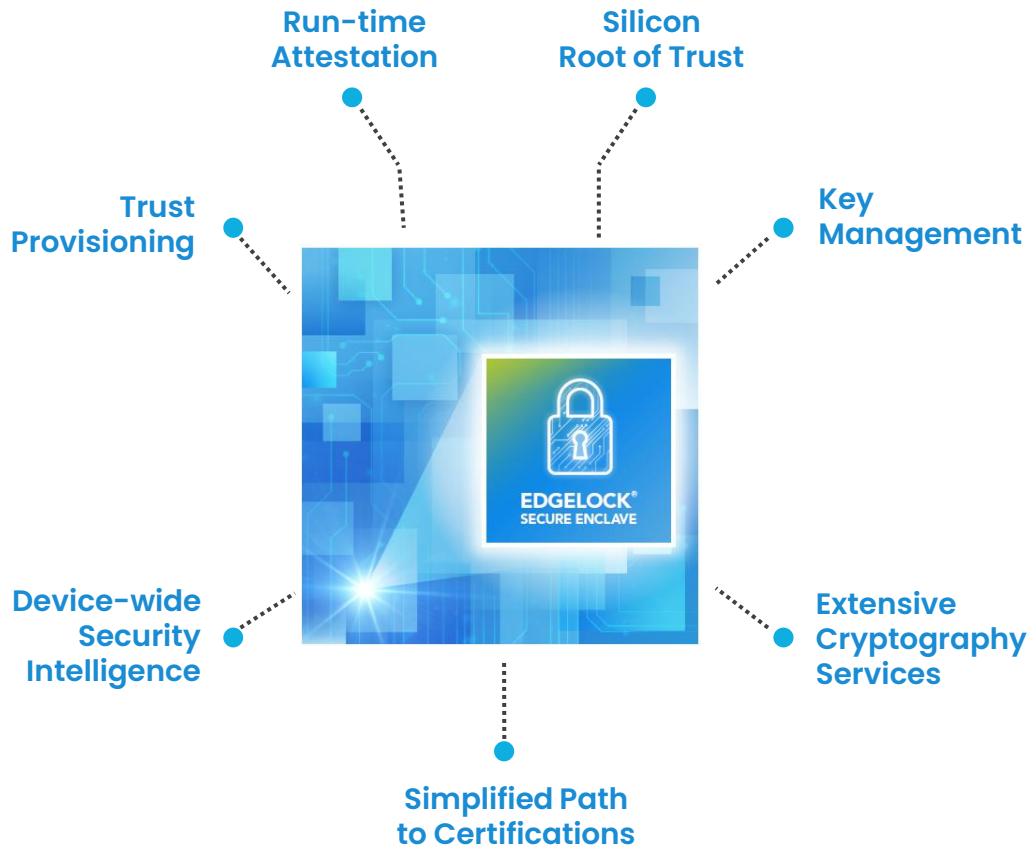
Security "HQ"
Where security is governed – this fortress inside the chip oversees security functions to protect the system against attacks

Managed agents
Agents extend security across the chip – distributed outside of the central HQ – to establish and maintain trust of security capabilities

Intelligent
Tracks power transitions to help prevent attack surfaces from emerging on heterogeneous multicore devices

Ready to go
Preconfigured security policies reduce the complexity and help avoid costly errors for faster time to market

nxp.com/SecureEnclave



i.MX 95 SoC: Optimized to seamlessly extend security beyond the integrated EdgeLock Secure Enclave to work with the EdgeLock SE05x secure element and EdgeLock A5000 secure authenticator. These discrete security components with optionally pre-injected keys and certificates provide a Common Criteria EAL6+ certified, turnkey plug-in solution, bringing additional tamper resistance and support for additional security use cases.

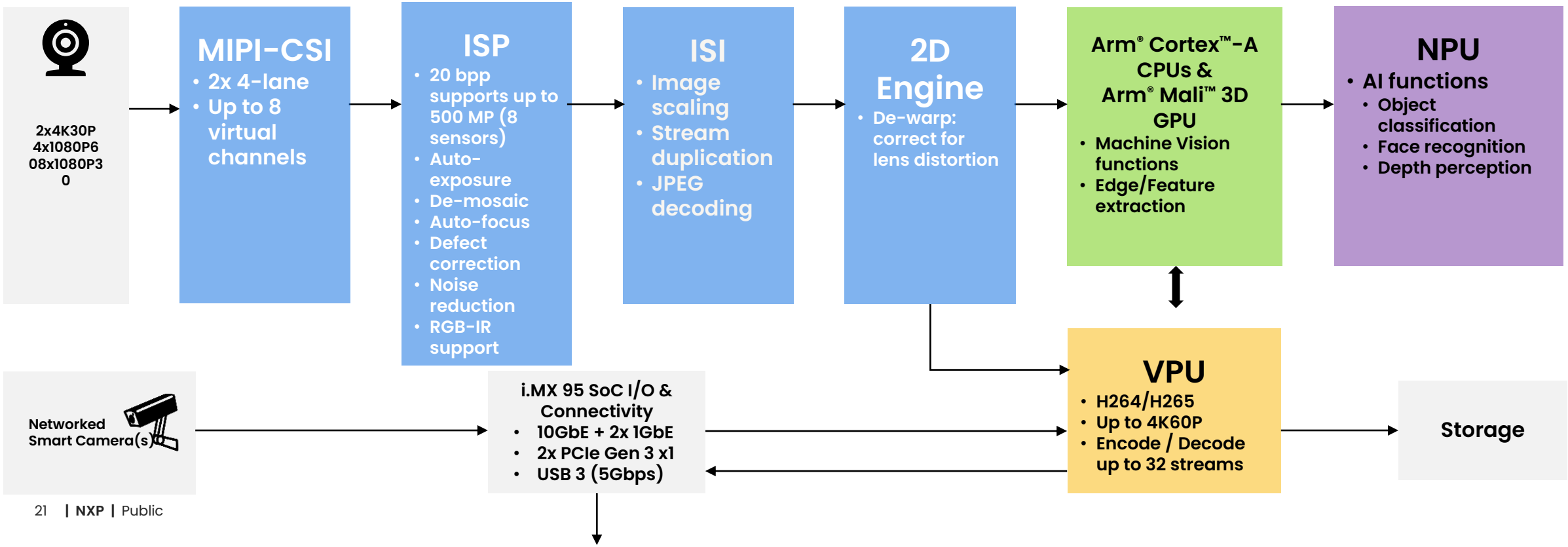
i.MX 95 SoC vision processing pipeline

Camera support

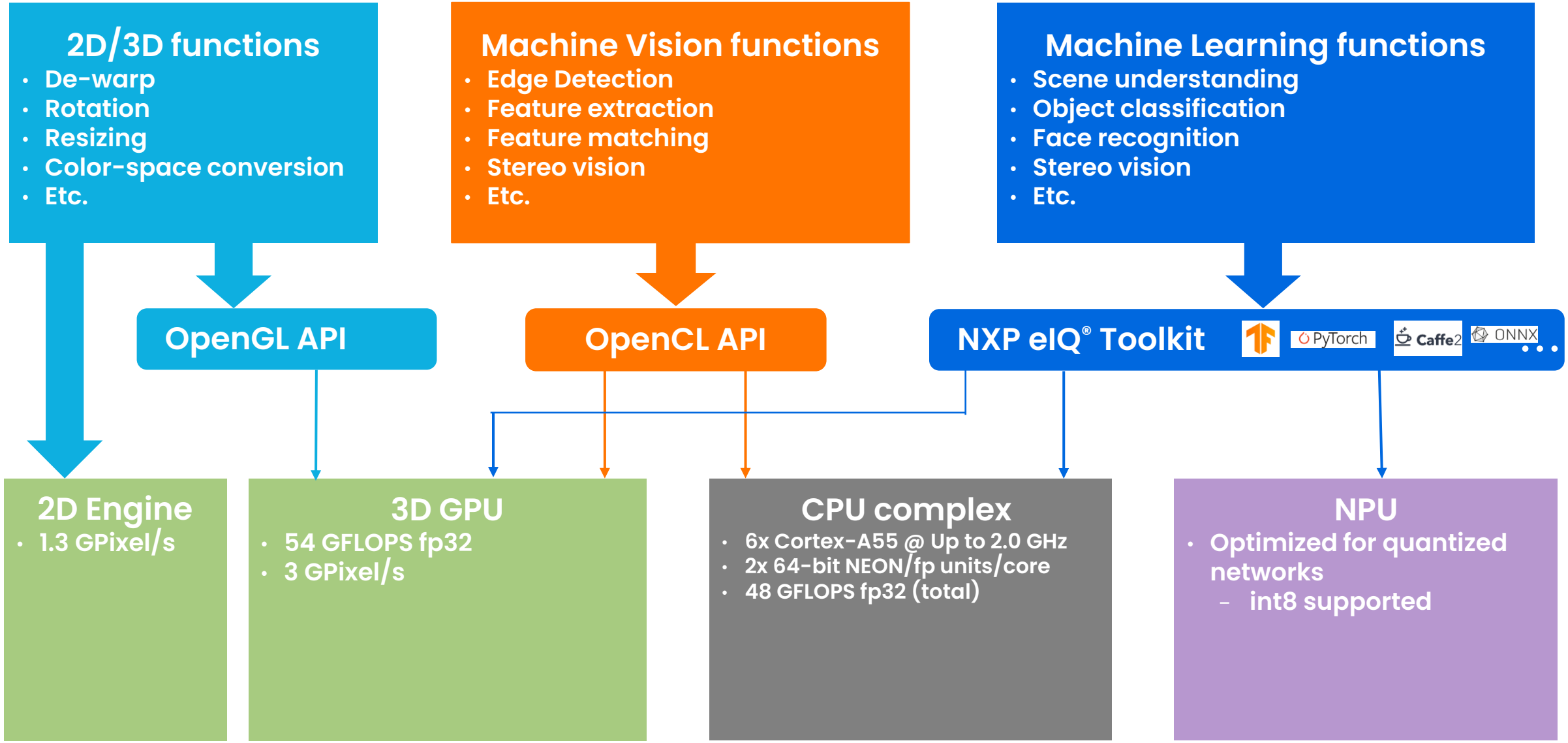
- 2x MIPI-CSI2 x4 lanes
  - Supports up to 8 raw cameras via Virtual Channels
  - Single 4K60P MIPI Camera with Overdrive mode
- Networked "Smart" Cameras
  - Up to 32 streams from Ethernet, PCIe, USB, or Wi-Fi connections

NXP Image Signal Processor (ISP)

- Optimized for Machine Vision applications
- 20 bpp pipeline supports up to 8 sensors w/aggregate 500 MPixel/s
- HDR combining of 2 exposures
- Support color, monochrome & RGB-IR sensors
- Advance de-noising and edge enhancement for low-light conditions
- Supports 2 Regions of Interest



i.MX 95 SoC embedded vision function mapping



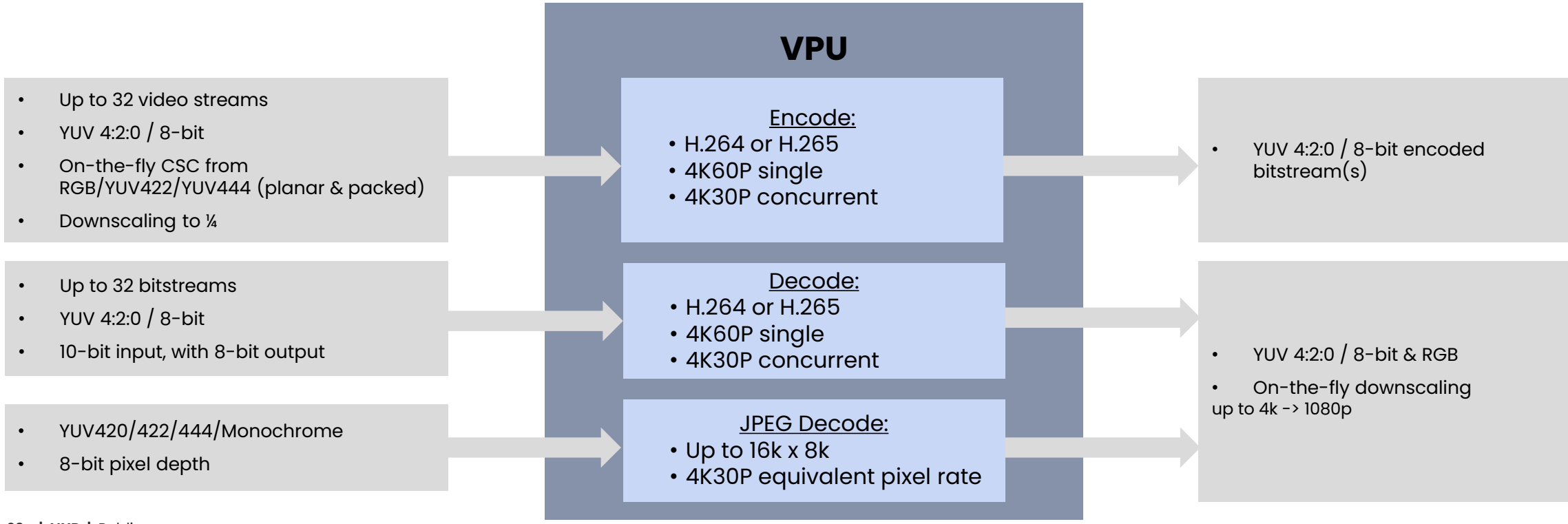
i.MX 95 SoC video processing unit (VPU)

i.MX 95 SoC video processing key features

- Minimizes memory bandwidth usage:
- Frame-buffer compression for internal VPU processing
- On-the-fly color-space conversion & downscaling of input video streams
- On-the-fly downscaling of output video streams
- Video output in YUV and/or RGB raster format

i.MX 95 SoC video processing key benefits

- Enables remote cameras & displays
- Supports up to 32 video streams
- H.265 supported for best quality compression



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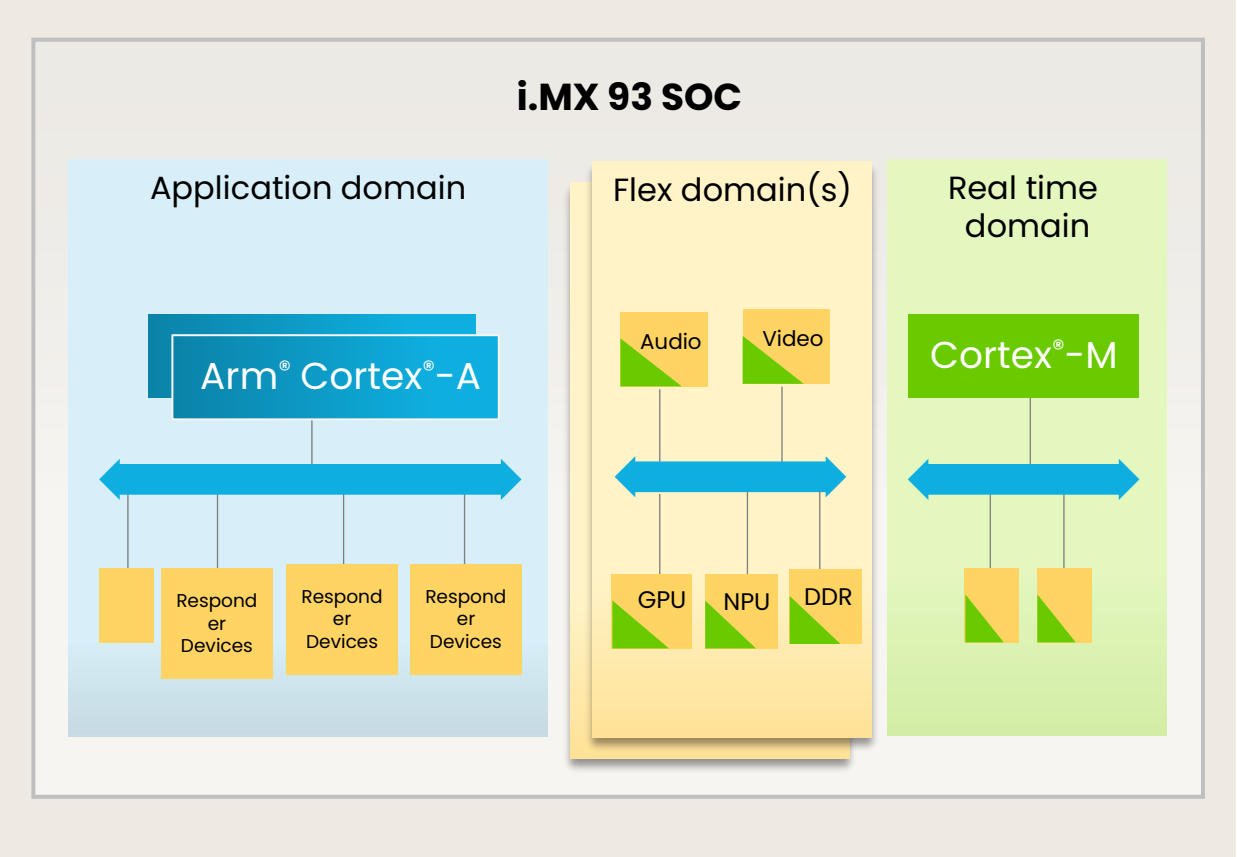
i.MX 93 SoC highlights

Technology inside the SoC

Energy efficient edge compute with Energy Flex architecture

Heterogeneous processing + hierarchical fine-grained power partitioning and management for power efficient processing

- Each domain can be independently powered off, so that it only consumes power when needed:
  - **Application domain** main high-performance application cores. Includes fine-grained control of number and operating frequency.
  - **Flex domain** includes multimedia and neural processing accelerators
  - **Real time domain** includes low-power real-time core and peripherals to enable background processes such as wake-word detect to consume very little power.
  - **Peripheral access** to any peripheral by any domain is allowed through extended Resource Domain Control (XRDC)
  - **Secure communication** between domains is enabled by secure Messaging Units (MUs)



Heterogeneous domain computing (HDC)
Shared topology, split power domains, split buses, secure IPC

i.MX 93 SoC – 11x11/14x14 mm package (196 Ios)

Package:
- 11x11 mm FCCSP 0.5 mm pitch, de-populated array
- 14x14 mm FCCSP 0.65 mm pitch de-populated automotive package

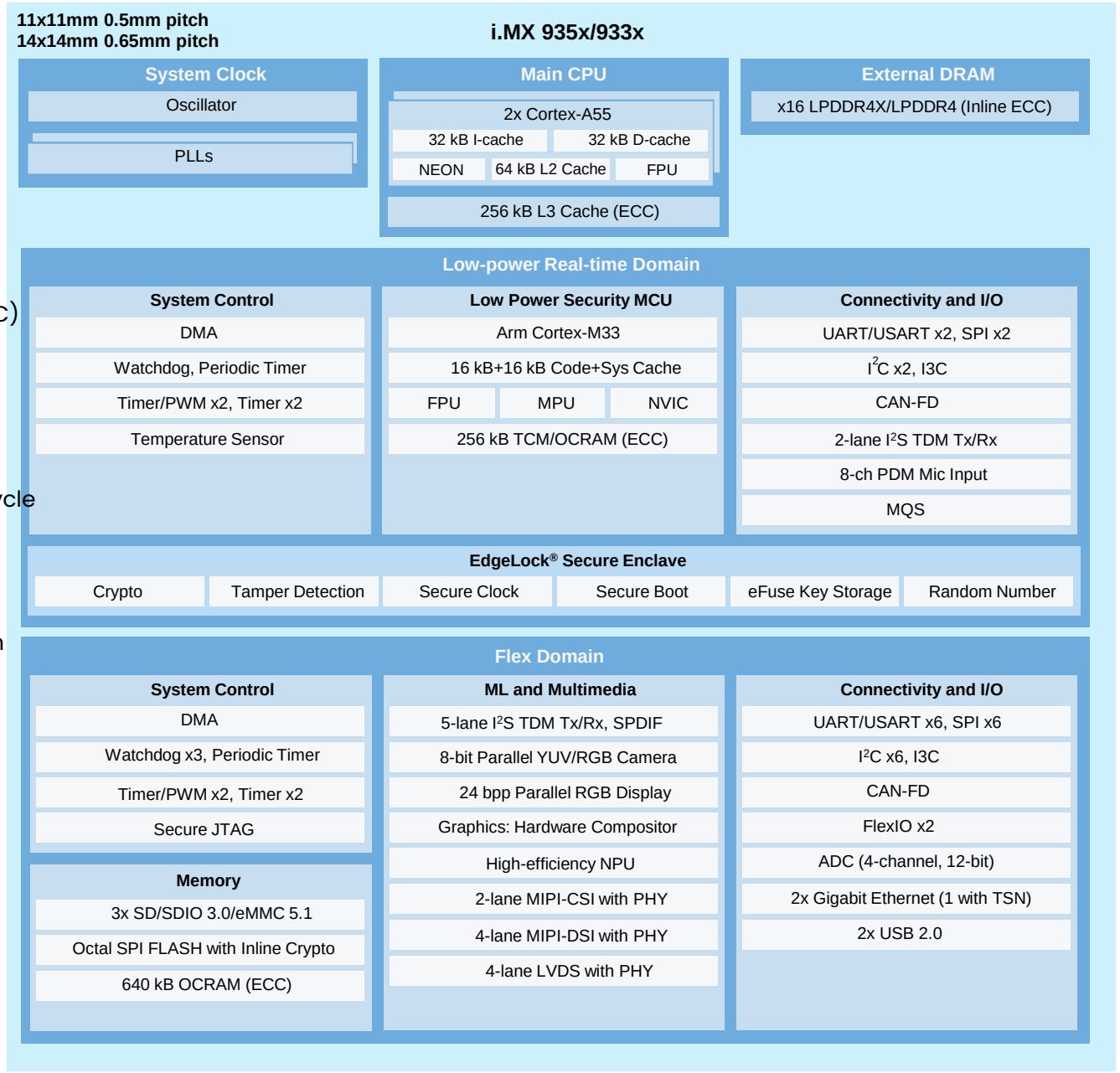
1x/2x Arm® Cortex®-A55 up to 1.7 GHz
- Arm v8.2 Fully 64-bit capable, 384kB total L2+L3 cache (ECC)

1x Arm Cortex-M33 up to 250 MHz
- Arm v8-M with Trustzone-M, 16 kB+16 kB cache (ECC), 256 kB TCM/OCSRAM (ECC)

Operating system targets: Linux® OS, FreeRTOS, VxWorks, QNX, GreenHills

Qual (Tj):
- Consumer (0 C to 95 C)
- Standard Industrial (-40 C to 105 C), Extended Industrial (-40 C to 125 C)
- Automotive (-40 C to 125 C) only for 14x14 mm pkg

Feature highlights:
- **Machine Learning**: Arm® Ethos™ U-65 Neural Processing Unit (NPU) 256 MACs/cycle
- **Security**: EdgeLock® Secure Enclave
- **External memory:**
  - Up to 3.7 GT/s x16 LPDDR4X/LPDDR4 (Inline ECC)
  - 3x SD 3.0/ SDIO3.0/ eMMC5.1
  - 1x Octal SPI, including support for SPI NOR and SPI NAND memories
- **2D graphics**: PXP Engine: Blending/Composition, Resize, Color Space Conversion
- **Display interface:**
  - 1080p60 MIPI-DSI (4-lane, 1.5 Gbps/lane) with PHY
  - 720p60 LVDS (4-lane)
  - 24-bit parallel RGB
- **Camera interface**:
  - 1080p60 MIPI-CSI (2-lane, 1.5 Gbps/lane) with PHY
  - 8-bit parallel YUV/RGB
- **Audio**:
  - 7x I2S TDM (32-bit @ 768 KHz), SPDIF Tx/Rx
  - 8 channel PDM microphone input
  - MQS: Medium Quality Sound output (sigma-delta modulator)
- **Connectivity**:
  - 2x USB 2.0 Type C with PHY
  - 2x Gb Ethernet: AVB & IEEE 1588 for sync, and EEE for low power. 1x with TSN
  - 2x CAN-FD
  - 8x UART/USART/Profibus, 8x I2C, 8x SPI, 2x I3C
  - 1x 4-ch, 12-bit ADC
  - 2x 32-pin FlexIO interfaces (camera, bus or serial I/O)



i.MX 93 Applications Processor features

Product	i.MX 931/932	i.MX 933/935	i.MX 930
Main CPU	1x/2x A55 1.7 GHz Arm® v8.2-A	1x/2x A55 1.7 GHz Arm v8.2-A	1x/2x A55 900 MHz Arm v8.2-A
	64 kB L2 + 256 kB L3 cache (ECC)		
MCU	1x M33, 250 MHz Arm v8-M		1x M33, 133 MHz Arm v8-M
	16 kB+16 kB cache (ECC), 256 kB TCM/OCRAM (ECC)		
DDR	3.2 GT/s x16 LPDDR4X/LPDDR4 Inline ECC	3.7 GT/s x16 LPDDR4X/LP4 Inline ECC	1.8 GT/s x16 LPDDR4X/LP4 Inline ECC
GPU	PXP Engine: Blending/Composition, Rotation, Resize, Color Space Conversion		
Security	EdgeLock® Secure Enclave		
AI/ML	Efficiency NPU		No NPU
SRAM	Up to 640 kB (ECC)		
Camera	8-bit parallel YUV/RGB	1080p60 MIPI CSI (2-lane), 8-bit parallel YUV/RGB	
Display I/F	24 bit per pixel parallel RGB	1080p60 MIPI DSI (4-lane) or 720p60 LVDS (4-lane) or 24 bit per pixel parallel RGB	1080p60 MIPI DSI (4-lane) or 24 bit per pixel parallel RGB
Connectivity	SDIO, USB2	SDIO, USB2	SDIO, USB2
Audio	SPDIF Tx/Rx, 8 channel PDM mic input, MQS output (sigma-delta modulator)		
	3x I2S TDM (32-bit @ 768 KHz)	7x I2S TDM (32-bit @ 768 KHz),	
Expansion I/O	8x UART/USART/Profibus, 8x I2C, 8x SPI, 2x I3C, 2x 32-pin FlexIO		
	1x USB 2.0, 1x 2-ch 12-bit ADC	2x USB 2.0, 1x 4-ch, 12-bit ADC	
Network/Storage	1x GbE, 2x CAN-FD, 3x SD/eMMC, Octal SPI	2x GbE (1x TSN), 2x CAN-FD, 3x SD/eMMC, Octal SPI FLASH	
Package	9x9 mm, 0.5 mm de-pop	11x11 mm, 0.5 mm de-pop 14x14 mm, 0.65 mm de-pop for auto	11x11 mm, 0.5 mm de-pop

04

i.MX 93 Family target markets

i.MX 93 Family: market positioning

"Intelligent and secure edge processor family for entry-level IoT applications" with key features including -

- EdgeLock® Secure Enclave subsystem to provide necessary security functions, dedicated NPU for efficient processing for ML applications in next-gen IoT market products
- Heterogenous processing of A55 + M33 cores (can boot from either core) with energy flex architecture for entry/mid-tier IoT applications that require high performance and low power
- Great Vision pipeline including MIPI-CSI interface along with 2x A55 and NPU to achieve cost-efficient vision applications across industrial, consumer IoT and auto markets
- Rich set of interfaces including 2x 1GbE, multiple audio channels, multiple display interfaces for a broad range of applications such as HMI, factory automation, audio soundbars

i.MX 93 Family vision applications across segments

- Keys features used in vision applications
  - Camera interface: MIPI-CSI
  - Other Interfaces: Ethernet, Wi-Fi connectivity and other low-speed interfaces (SPI, UARTs etc.)
  - Processing: A55, NPU, M33

Industrial automation	Smart home	Smart city	Automotive
• Industrial Machine vision • Industrial scanning/printing	• Smart doorbell • Smart lock • Smart home hub/ Hue Bridge	• Smart lighting • Traffic control	• Driver Monitoring System (DMS) • Object Monitoring System (OMS)

i.MX 93 SoCs for industrial automation and building control

- Keys features used in industrial applications
  - Network interfaces: 2x Ethernet (preferred), 2x CAN-FD
  - Display interface: LVDS (preferred), MIPI-DSI
  - Other Interfaces: good number of low-speed interfaces (SPI, UARTs, I^2C, etc.)
  - Processing: A55, M33 (for low power and/or real time application), NPU (for ML use cases)
  - Others: High Security, ADC, TSN on Ethernet, OS such as QNX, VxWorks, Green Hills

Industrial automation	Building control & energy
• Industrial HMI • Industrial gateway • I/O control • Combines with i.MX RT1180 crossover MCU for larger gateways and IO controller	• Access control • Energy meter • Energy grid equipment • EV charging station • Environmental control • Sensor hub

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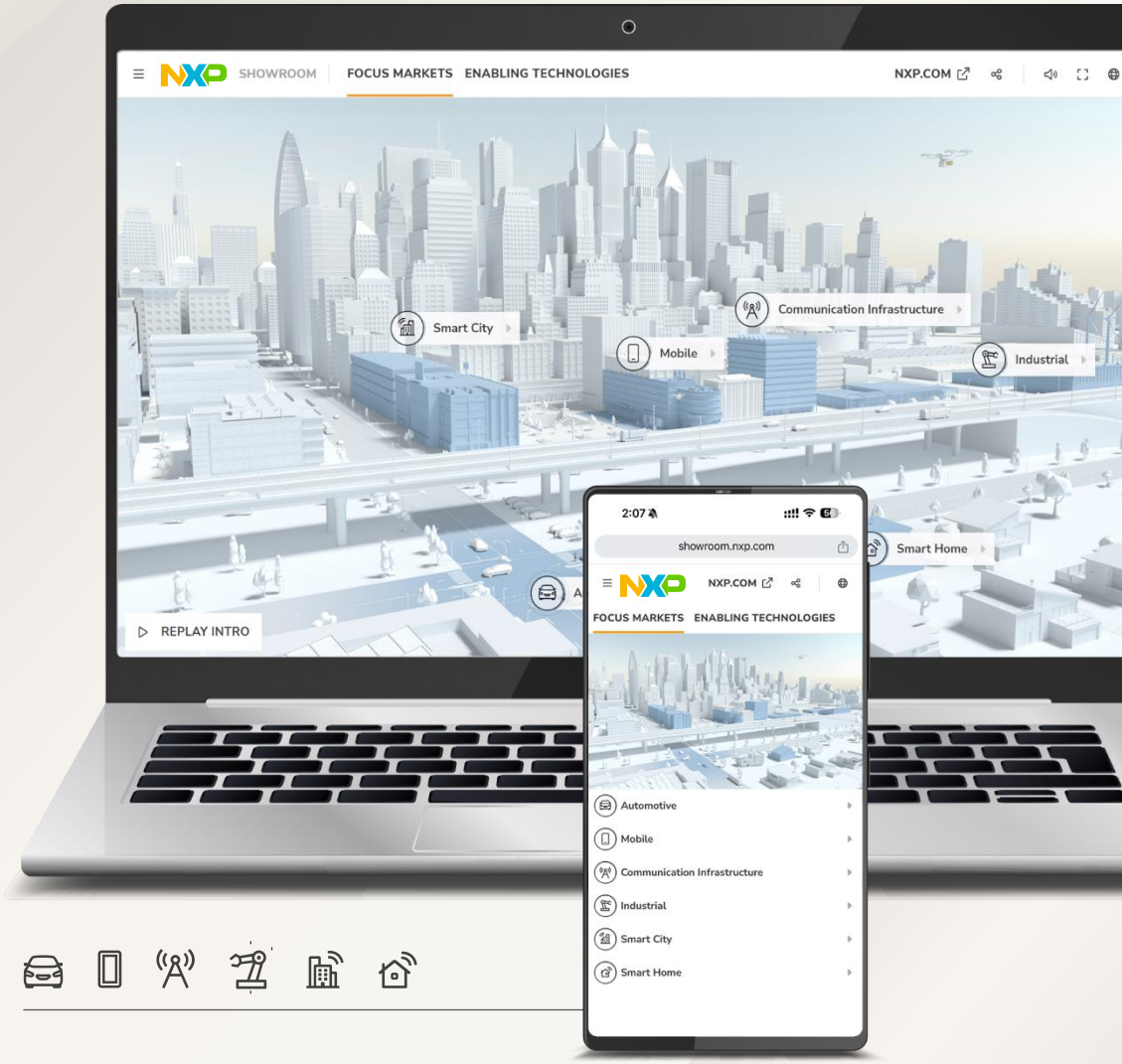

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车用i.MX系列路线图与i.MX 95亮点简介

i.MX automotive roadmap and overview featuring the i.MX95

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