

NXP NEW FUNCTIONAL SAFETY SBC – FS26

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REGIONAL MARKETING MANAGER



SECURE CONNECTIONS
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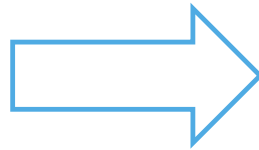
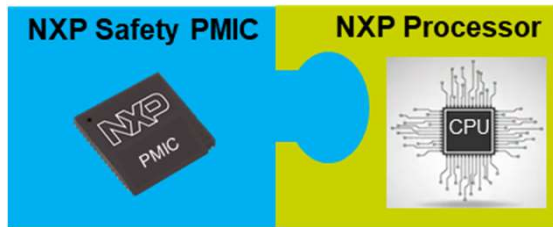


Agenda

- **NXP Safety Power Management**
- **FS26 Overview & Key Features**
- **Functional Safety Features**
- **Product Portfolio Segmentation**
- **S32K3 + FS26 attach**
- **Enablers**

Automotive Safety PMIC/SBC Solutions

1 100% Processor Attach



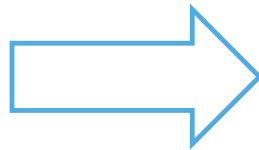
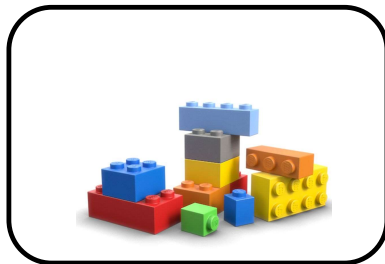
S32		V2X		Radio		LS	
S32K1	UJA11 / FS45	SAF51	PF3000	Mercury	VR5500	LS10x	FS85 + PF82
S32K3	FS23/FS26	SAF52	PF3000	DiRaNA	VR5500	LS10x	VR5510 + PF5020 + PF5023
S32S/Z/E	FS86 / FS67 + PF5030	SAF53	VR5500	Titan	VR5500	LS208x	FS84/85 + PF5020x2+ PF5023
S32G2	VR5510	SAF54	VR5510	Merlin	VR5500		
S32G3	VR5510+PF53	SXF1800	PF3000	Lithio	VR5500		
S32R2	FS84/FS85						
S32R4	FS85 + PF50						
S32V	FS85 + PF50						

i.MX		SCA	
i.MX 6	PF0100	UWB + BLE+ NFC Soc	FS24
i.MX 7	PF3000		
i.MX 8	PF8200 /PF7100		

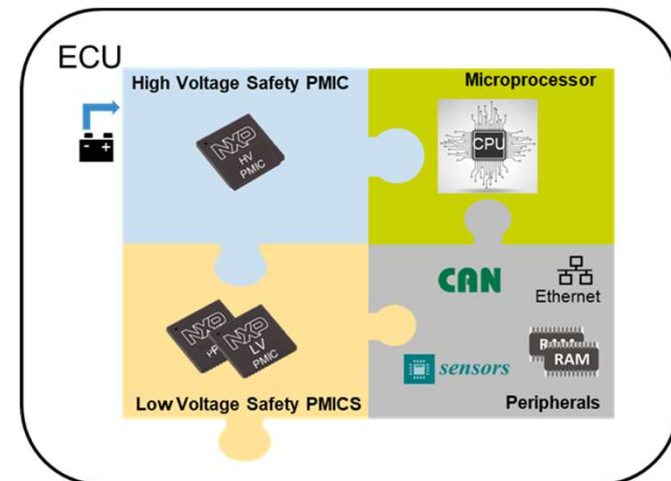
PF502X (Companion Chip – Low Vin (<5V) Domain)

FS56/FS86 (Companion Chip – Vbat Domain)

2 System Power Solutions



SAFETY PMIC “building blocks” Portfolio



NXP Safety PMIC's DNA



Safe

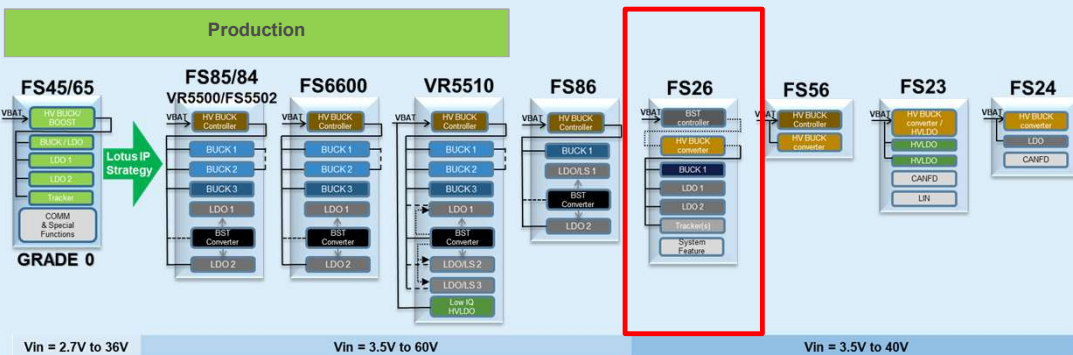


Scalable

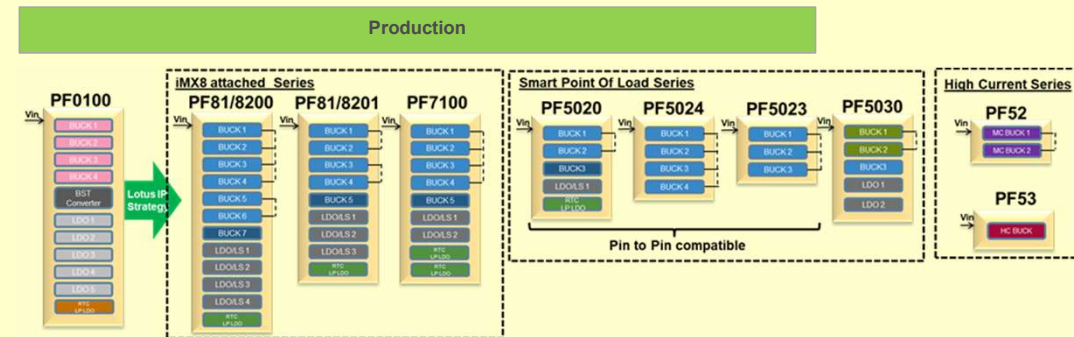


Expandable

PMIC 12V/24V Battery Connected

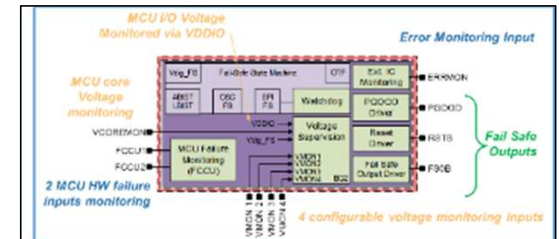
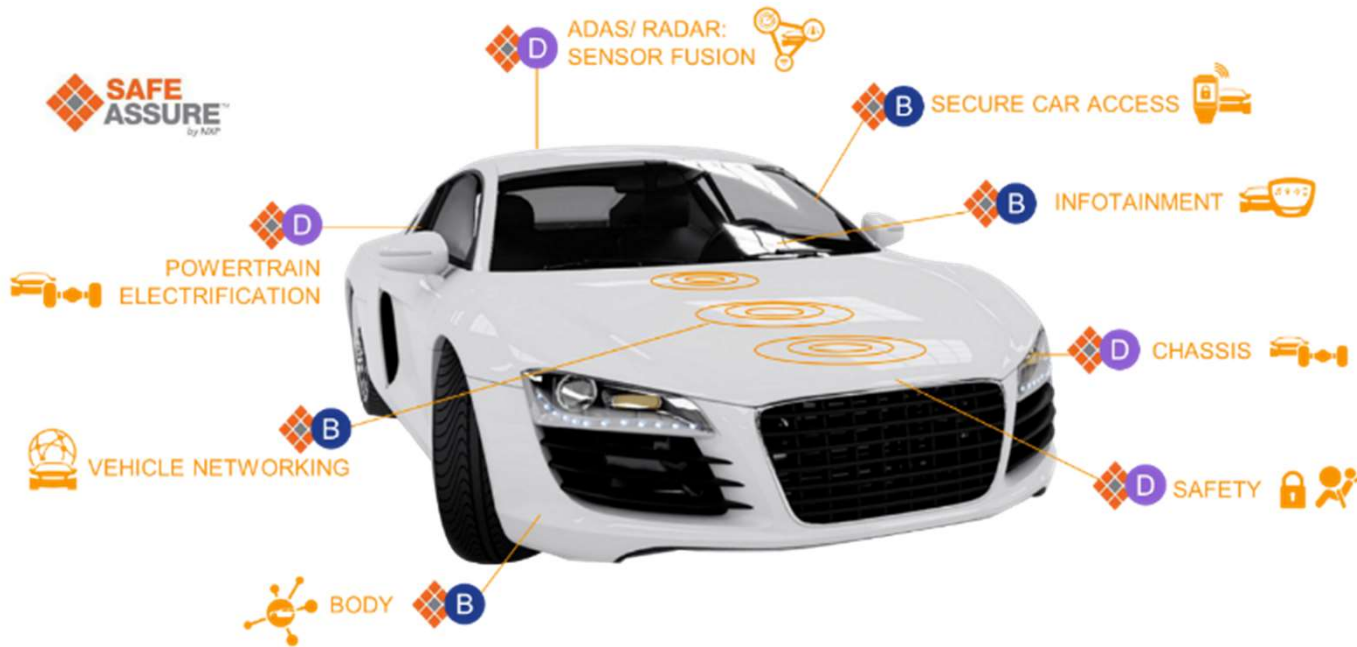


PMIC <5V Low Vin Connected



NXP FUNCTIONAL SAFETY SYSTEM SOLUTIONS

3rd Generation of SAFETY PMIC



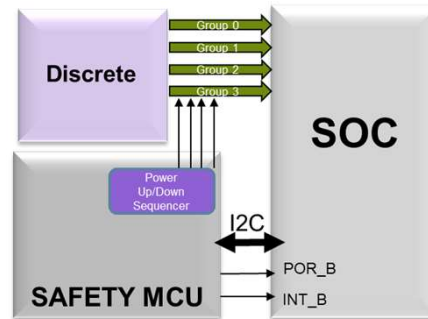


SCALABILITY

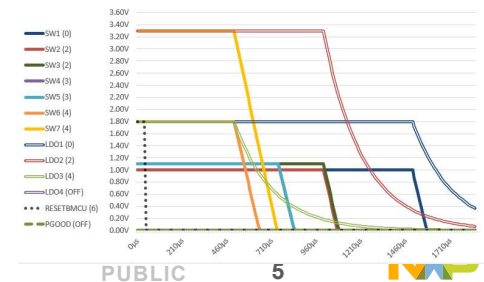
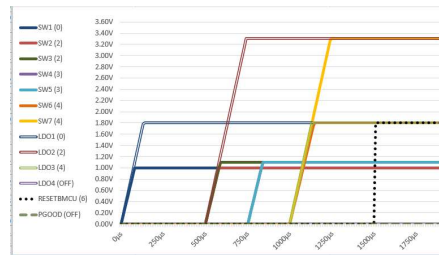
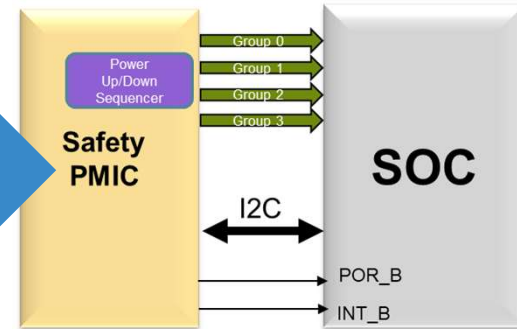
- **Flexible product** through OTP configuration
 - ✓ Buck / LDO/ Boost value setting
 - ✓ Safety reaction
 - ✓ Some functionality
- ✓ **Embedded & configurable Power up /down sequencer**
 - ➔ No Need for external controller
 - ➔ Predictable Power Sequence

Sequencing

	i MX 8Dx	S32G275
Group 0	SNVS	3.3V Standby GPIO's
Group 1	Main & SCU	All 3.3V GPIO's
Group 2	I/O's and DDR interface	All 1.8V Domains
Group 3	consists of the remaining portions of the SOC	Main Core and Standby Core

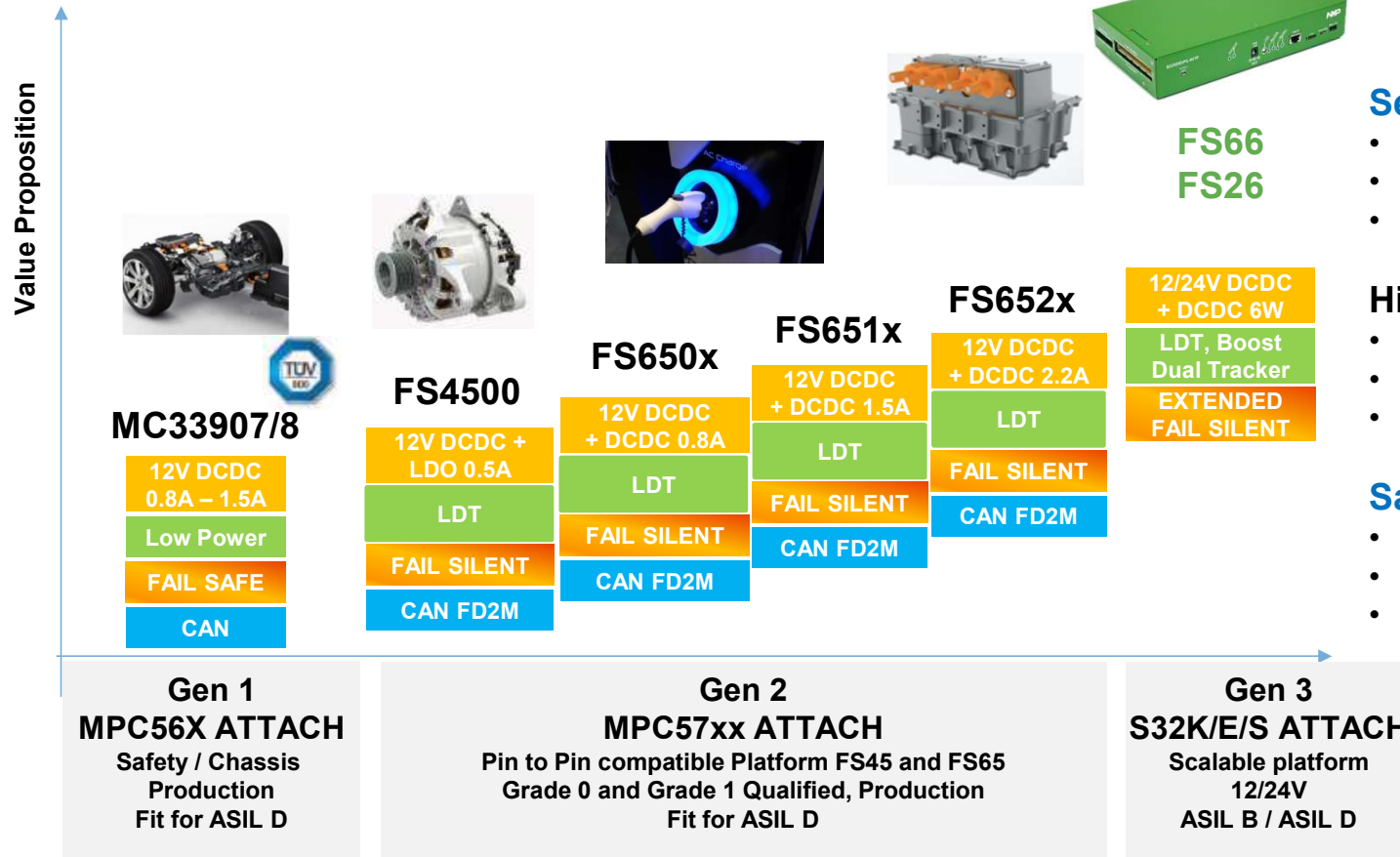


Integration Simplified



SENSE – THINK – ACT

MCU + POWER MANAGEMENT & SAFETY



Secured & Safe System Solutions

- ISO26262 architecture (TUV SUD proven)
- Functional robustness (non ISO pulse, EMC, HTOL)
- Security (SM transition)

High Efficient Solutions

- Target 12 V & 24 V (application note)
- Dual DCDC architecture (Vpre + Vcore)
- Ultra low power modes (low Iq, long dur. timer)

Safety Simplified Solutions

- ISO26262 ready documentation
- System validation test (eFAST)
- Global ecosystem (incl HW & SW)



New Gen FS SBC FS26 Overview

FS26: ASIL B/ASIL D PREMIUM SAFETY SBC

S32K & OTHER SAFETY MCUS ATTACH SOLUTION

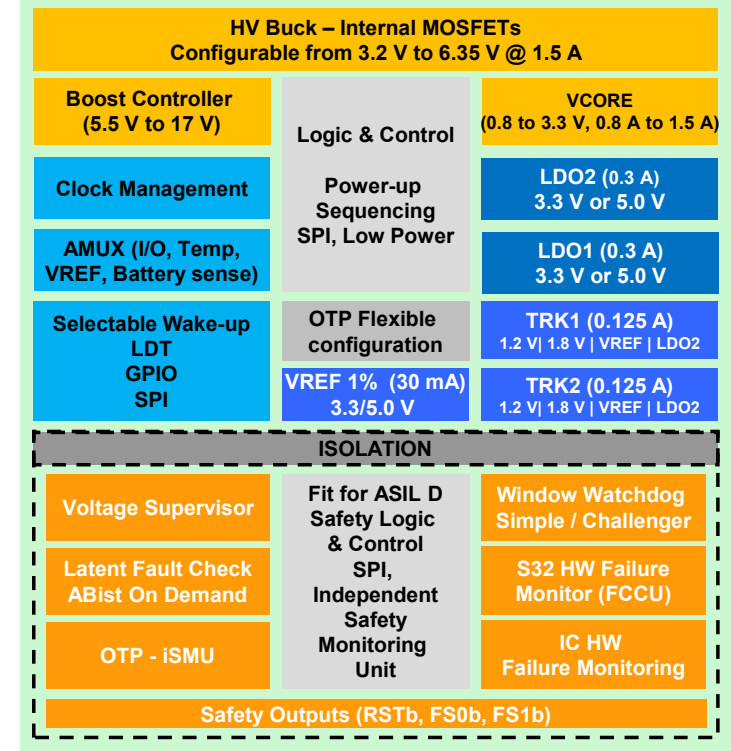
Power Management Solution

- Input supply up to 40 V DC
- HV Buck**, adjustable step down DC/DC converter 3.2 V to 6.35 V (50 mV step), 1.5 A DC,
 - 440 kHz or 2.25 MHz Synch. Buck with integrated MOSFETs, up to 92% efficiency
- VCORE**, adjustable step down DC/DC converter 0.8 V to 3.3 V (10 mV step), 800 mA to 1500 mA DC (to supply S32K3, and other Safety MCUs)
 - 2.25 MHz Fully-Integrated Synchronous Buck, up to 85 % efficiency
- Boost Controller** 5.5 V to 17 V, external Switch
- LDO1 and LDO2**, configurable 3.3 V or 5.0 V, up to 300 mA DC output current capability.
- VREF**, accurate voltage reference 3.3 V or 5 V, 1 %, 30 mA DC output current capability
- 2 TRACKERS**, 10 mV offset, 125 mA DC output current capability

Safety & System Features

- 3rd Generation Fail Safe State Machine** with Independent Safety Monitoring Unit
 - Fit for **ASIL B** and **ASIL D** with Extended Voltage Monitoring
 - ABIST On Demand** and Fault Recovery Strategy (combined with S32K3 – common platform)
 - 2 x FS outputs. 1 with configurable time delay (FS1b with dedicated part number)
- 32 bits SPI (including CRC)
- Long Duration timer (with dedicated part number)
- Low Power Mode :
 - 40 µA in Low Power mode in LPOFF and 20 µA in Standby (MCU powered)
 - Wake up via GPIOs, and Long Duration Timer (LDT) feature
 - Support S32K3 standby mode
- AMUX: Battery, Internal Safety critical voltages, Precise Vref and Temperature, GPIOs
- General Purpose I/O: Wake up or HS/LS Driver (HS 20 mA, LS 2 mA capability)

FS26 Functional Block Diagram



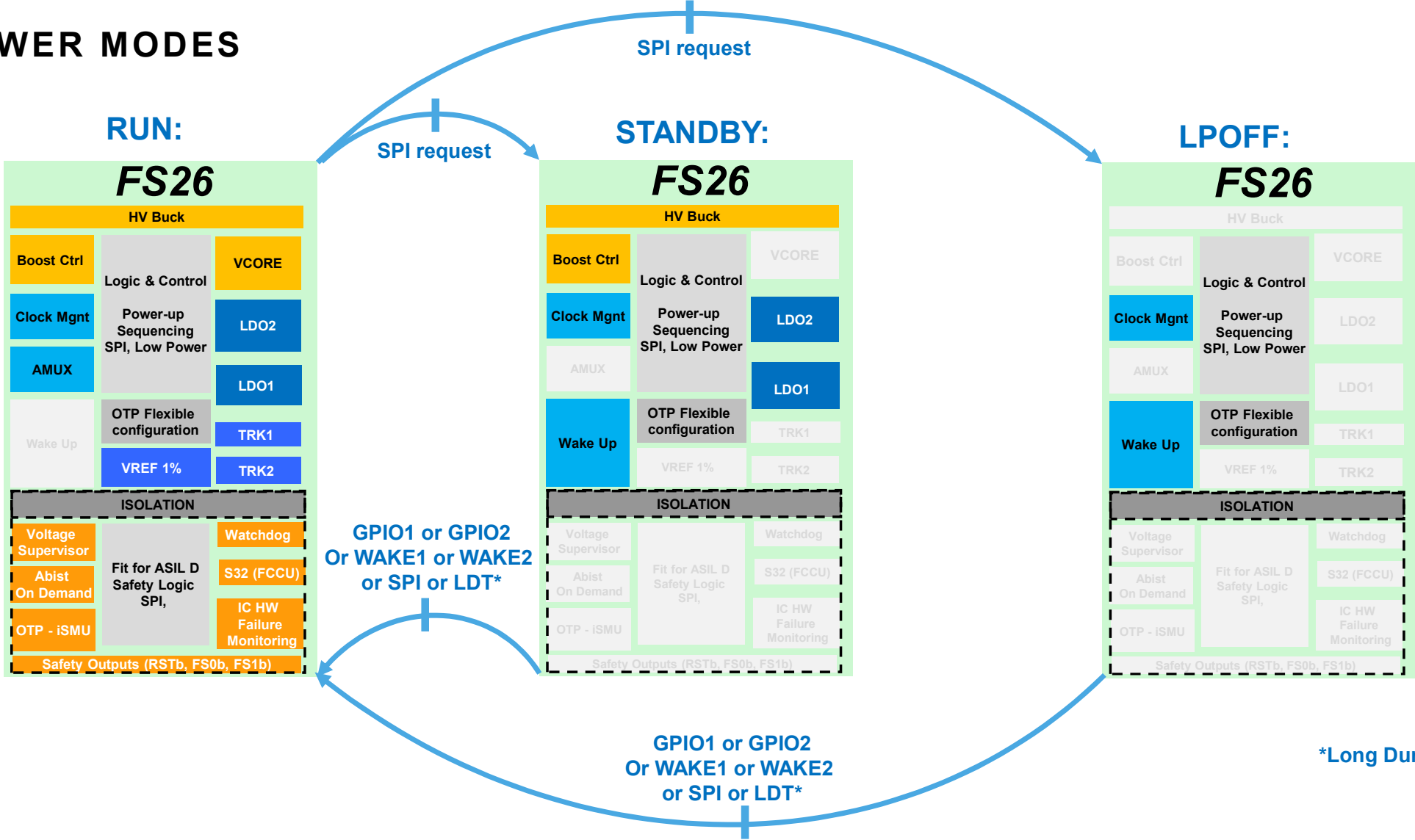
Package : LQFP48eP

Samples : Available now
PPAP: Q2'2022

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POWER MODES



*Long Duration Timer



Functional Safety Features

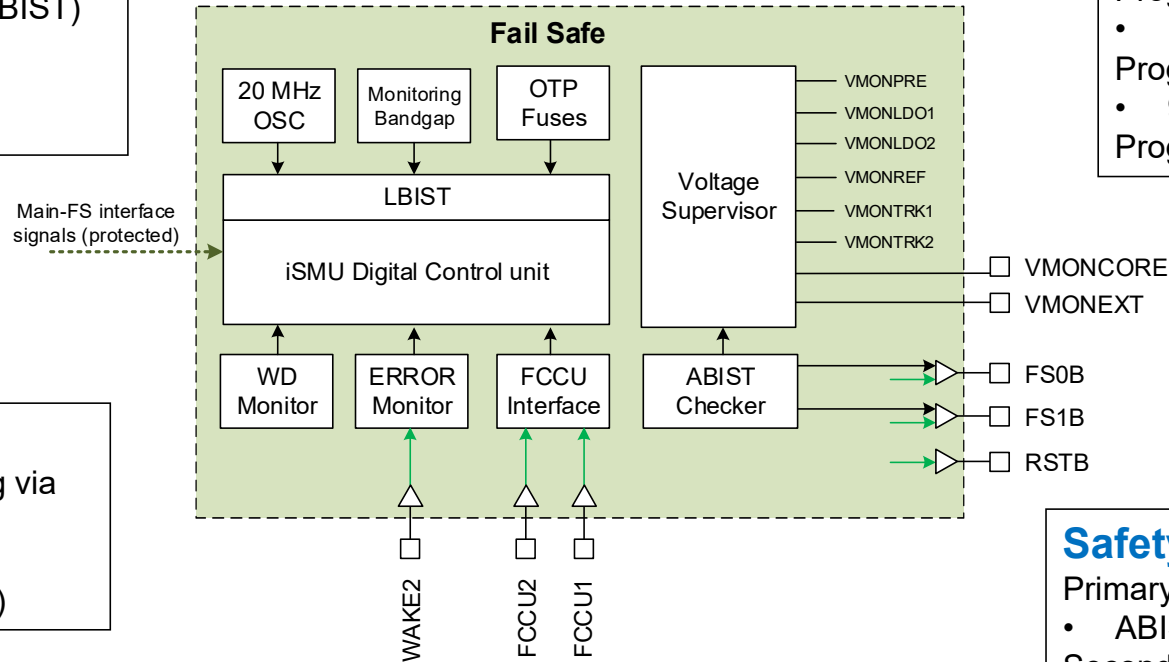
Functional Safety Features

Self Test:

- Logic Built-in test at power up (LBIST)
Analog build-in test (ABIST):
- At power up
 - ABIST on demand

OV/UV monitors:

- Programmable OV threshold:
- 104.5% to 112%
- Programmable UV threshold:
- 95.5% to 88%
- Programmable OV/UV deglitch time



Watchdog Monitoring:

- Configurable Watchdog Monitoring via SPI communication
- Simple Watchdog (ASIL-B)
 - Challenger Watchdog (ASIL-D)

Safety Inputs:

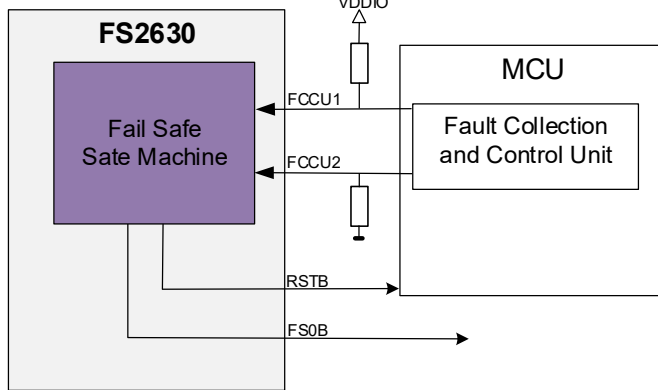
- General purpose ERROR MON on WAKE2 pin
Configurable MCU error detection via FCCU pins
- Bi-stable operation
 - 2 x independent inputs
 - Single pin operation

Safety Outputs:

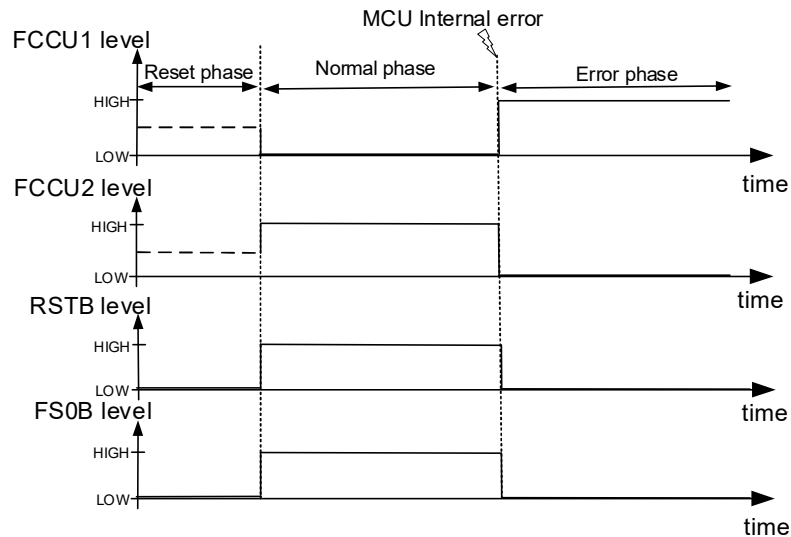
- Primary Safety output on FS0B:
- ABIST + redundant control
- Secondary Safety Output on FS1B:
- Configurable Reaction
- MCU reset signal (RSTB)
- Bi-directional with PMIC reset control via the 8second Timer.

FAULT COLLECTION AND CONTROL UNIT MONITORING

* FCCU pins connection example:



* FS2630 RSTB and FS0B reaction example:



Key Features:

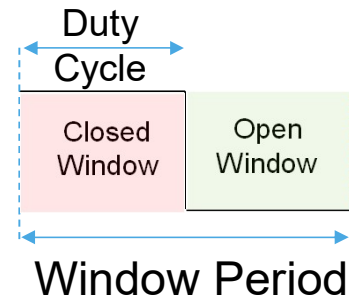
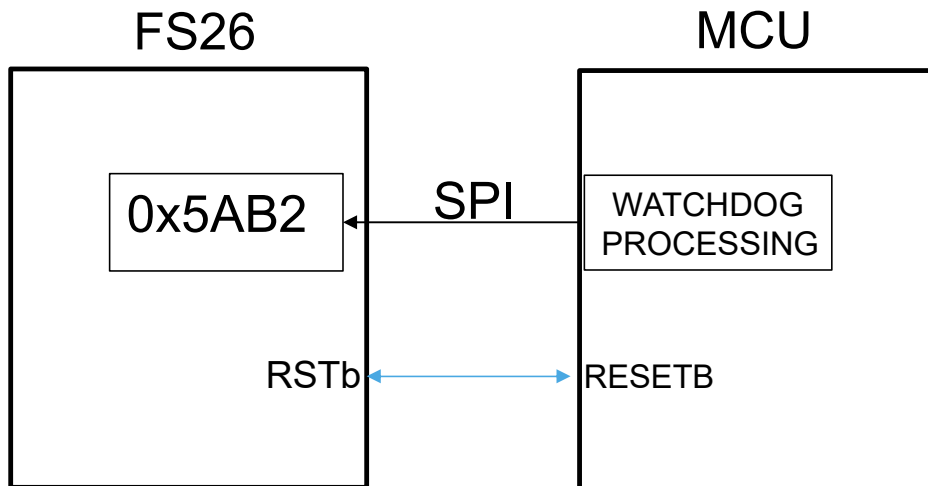
- 8 different error protocols **configurable via OTP**:
 - No monitoring
 - FCCU1 AND FCCU2 inputs monitoring activated by pair (Bi-stable protocol)
 - FCCU1 or FCCU2 single input level monitoring activated
 - FCCU1 input level monitoring only. FCCU2 input not used
 - FCCU2 input level monitoring only. FCCU1 input not used
 - FCCU1 or FCCU2 single input PWM monitoring activated
 - FCCU1 input PWM monitoring only, FCCU1 input level monitoring
 - FCCU2 input PWM monitoring only, FCCU2 input level monitoring
- Various settings configurable **by SPI command**:
 - FCCUx error level
 - Filtering time adjustable from 3 μ s to 20 μ s
 - Error impact on Reset and Safety output configurable

WATCHDOG PROCESSING

- 2 types of watchdog are available (Simple and Challenger) – OTP selection

Simple Watchdog

- This windowed watchdog is based on only one watchdog key : 0x5AB2 (default value).
- MCU can use its own seed if needed.

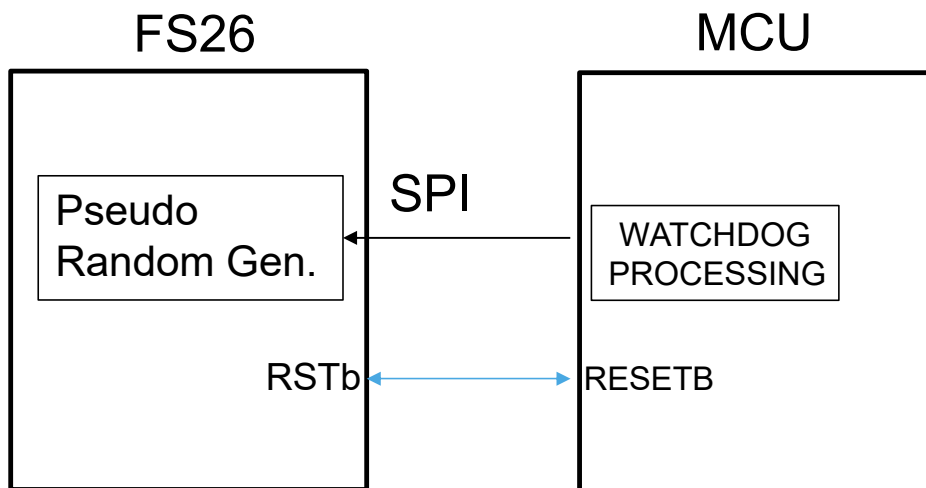


Duty Cycle [2:0]	Value	
	Closed Window	Open Window
Duty Cycle [2:0]=000	31.25%	68.75%
Duty Cycle[2:0]=001	37.5%	62.5%
Duty Cycle[2:0]=010	50%	50%
Duty Cycle[2:0]=011	62.5%	37.5%
Duty Cycle[2:0]=100	68.75%	31.25%
Others	50%	50%

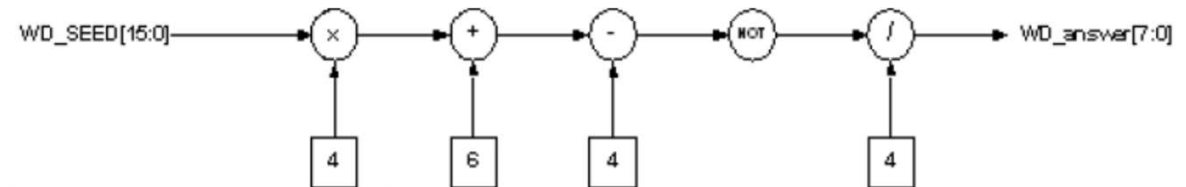
Parameter	Value
WD_WINDOW[3:0]=0000	DISABLE
WD_WINDOW[3:0]=0001	1 ms
WD_WINDOW[3:0]=0010	2 ms
WD_WINDOW[3:0]=0011	3 ms
WD_WINDOW[3:0]=0100	4 ms
WD_WINDOW[3:0]=0101	6 ms
WD_WINDOW[3:0]=0110	8 ms
WD_WINDOW[3:0]=0111	12 ms
WD_WINDOW[3:0]=1000	16 ms
WD_WINDOW[3:0]=1001	24 ms
WD_WINDOW[3:0]=1010	32 ms
WD_WINDOW[3:0]=1011	64 ms
WD_WINDOW[3:0]=1100	128 ms
WD_WINDOW[3:0]=1101	256 ms
WD_WINDOW[3:0]=1110	512 ms
WD_WINDOW[3:0]=1111	1024 ms

CHALLENGER WATCHDOG

- This windowed watchdog is based on pseudo-random word (16 bits)
- On each WD refresh a new seed is generated automatically by the FS26
- The WD answer is calculated separately on each device (MCU and FS26)
- MCU sends the results to FS26 (watchdog answer)
- FS26 compares two results



- 1 – MCU must read the new word
- 2 – MCU and FS26 compute the WD answer



- 3 – MCU send WD answer to FS26



FS26 Partnumbering

FS26XX PRODUCT NUMBERING SCHEME

★ M		FS		★ 26 X Y Z		V		M		zzz		★ AE		R2	
Release Type		Family		Product Core		Release Version		Temperature		Funct. or Param. variant		Package		Shipping Method	
M	Production	FS	High Voltage Power Management	0000-9999	Core	A	Initial Release	B	-0 to 70C	Blank	If not required	PP	Per NXPOMS-1719007347-1420	R2	Per NXPOMS-1719007347-2918
P	Pre-release					B-Z	as required	C	-40 to 85C						
S	Customer special					M	-40 to 125C	W	-40 to 150C						

FS 26 x y z

z	ASIL
B	Fit for ASIL B (Simple W/D, UV/OV, ABIST, VMON)
D	Fit for ASIL D (Challenger WD, FCCU, ABIST/LBIST, VMON)

y	FS1b	LDT	Use case
0	no	no	Base
1	yes	no	FS1b
2	no	yes	LDT
3	yes	yes	FS1b & LDT

x	PMIC Solution
0	Vcore 0.8A , Vboost, 1 MV Buck, 2 LDOs 1 Tracker
1	Vcore 0.8A , Vboost, 1 MV Buck, 2 LDOs 2 Trackers ,
2	Vcore 1.5A , Vboost, 1 MV Buck, 2 LDOs 1 Tracker
3	Vcore 1.5A , Vboost, 1 MV Buck, 2 LDOs 2 Trackers ,

Family Segmentation
2 series : General Purpose
26 : Attach to S32K3

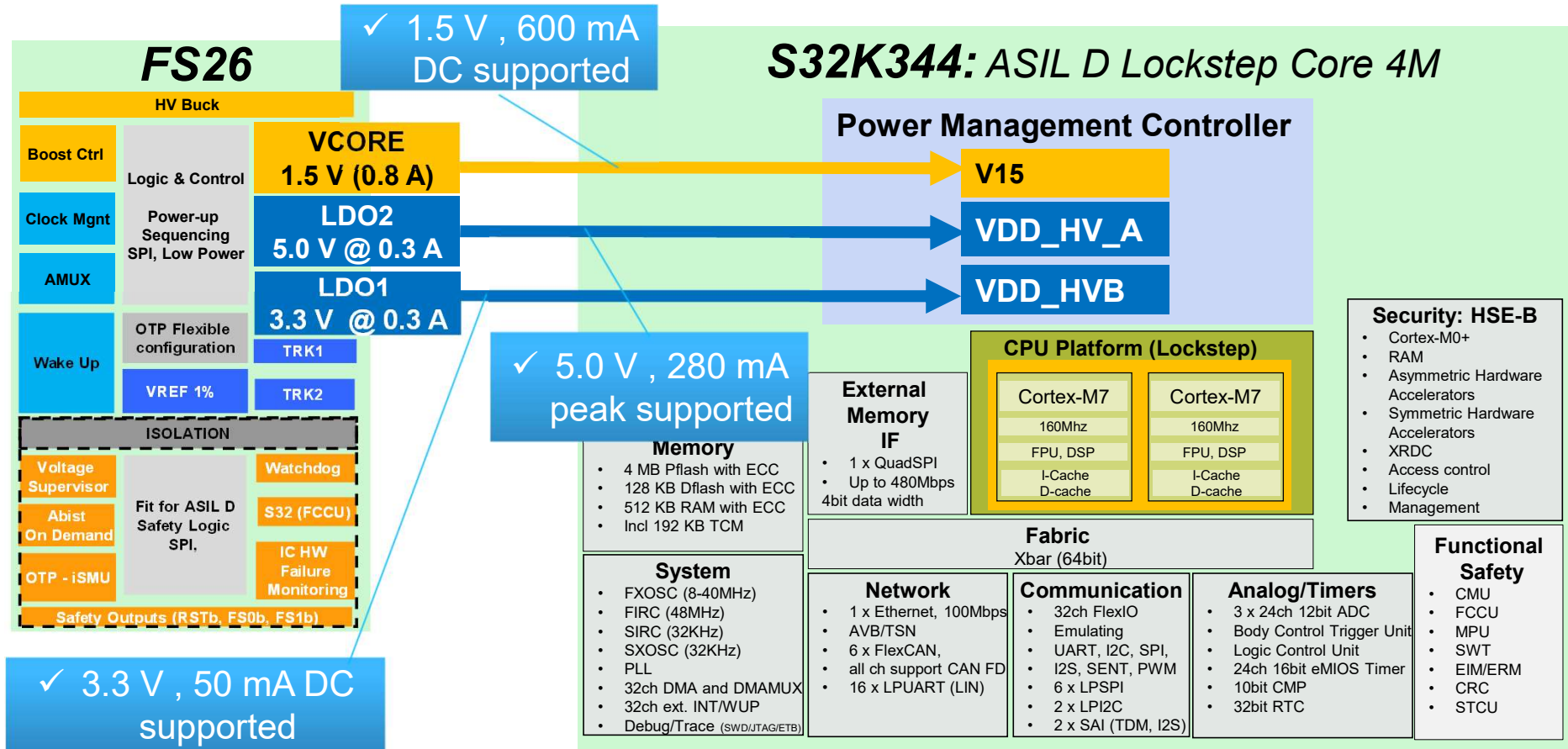
SELECT YOUR BEST CONFIGURATION

Vcore	0.8A core				1.5A core			
EXT Supply	1 TRK		2 TRK		1 TRK		2 TRK	
ASIL Level	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D
Base	FS2600B	FS2600D	FS2610B	FS2610D	FS2620B	FS2620D	FS2630B	FS2630D
FS1b	FS2601B	FS2601D	FS2611B	FS2611D	FS2621B	FS2621D	FS2631B	FS2631D
LDT	FS2602B	FS2602D	FS2612B	FS2612D	FS2622B	FS2622D	FS2632B	FS2632D
FS1b + LDT	FS2603B	FS2603D	FS2613B	FS2613D	FS2623B	FS2623D	FS2633B	FS2633D



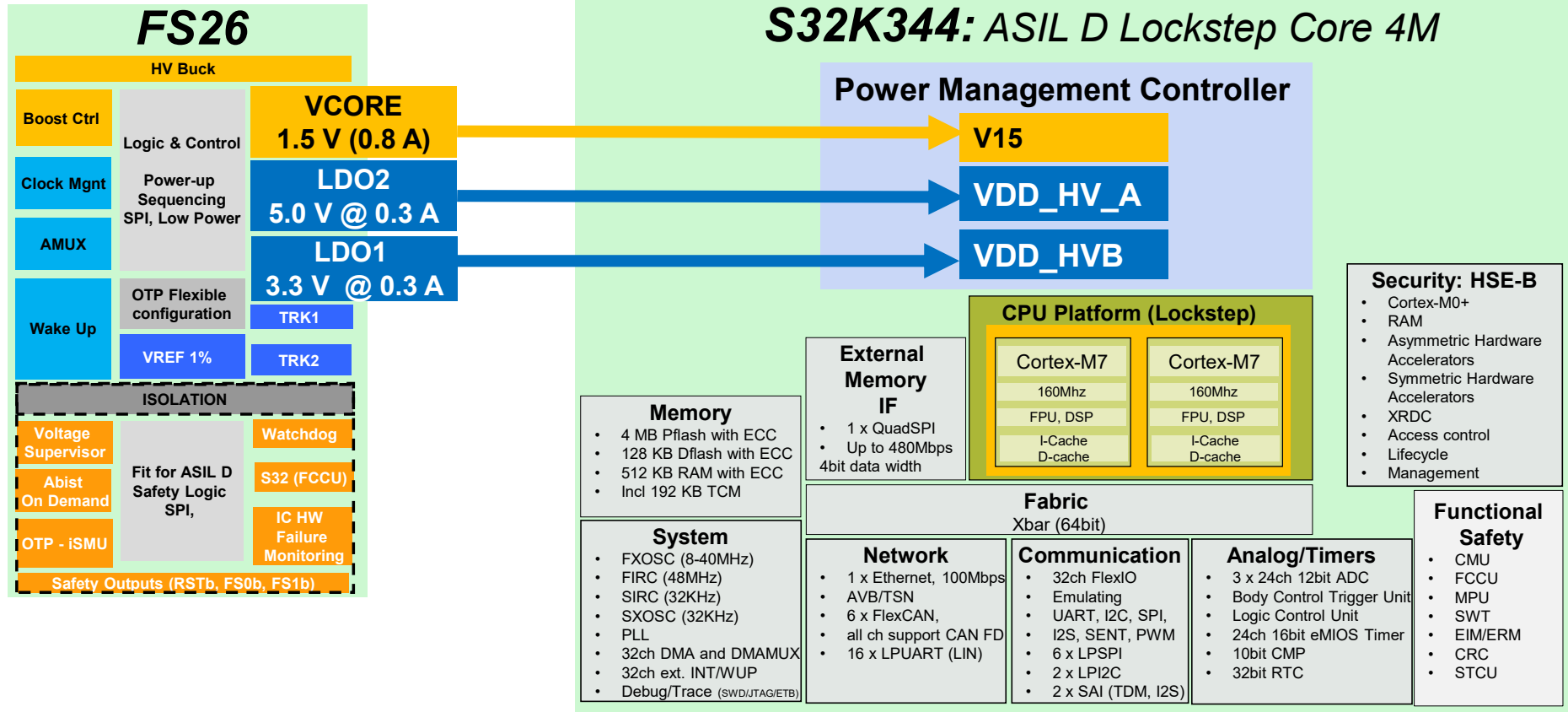
S32K3 + FS26
attach

S32K3 FS26 ATTACH, POWER MANAGEMENT OVERVIEW

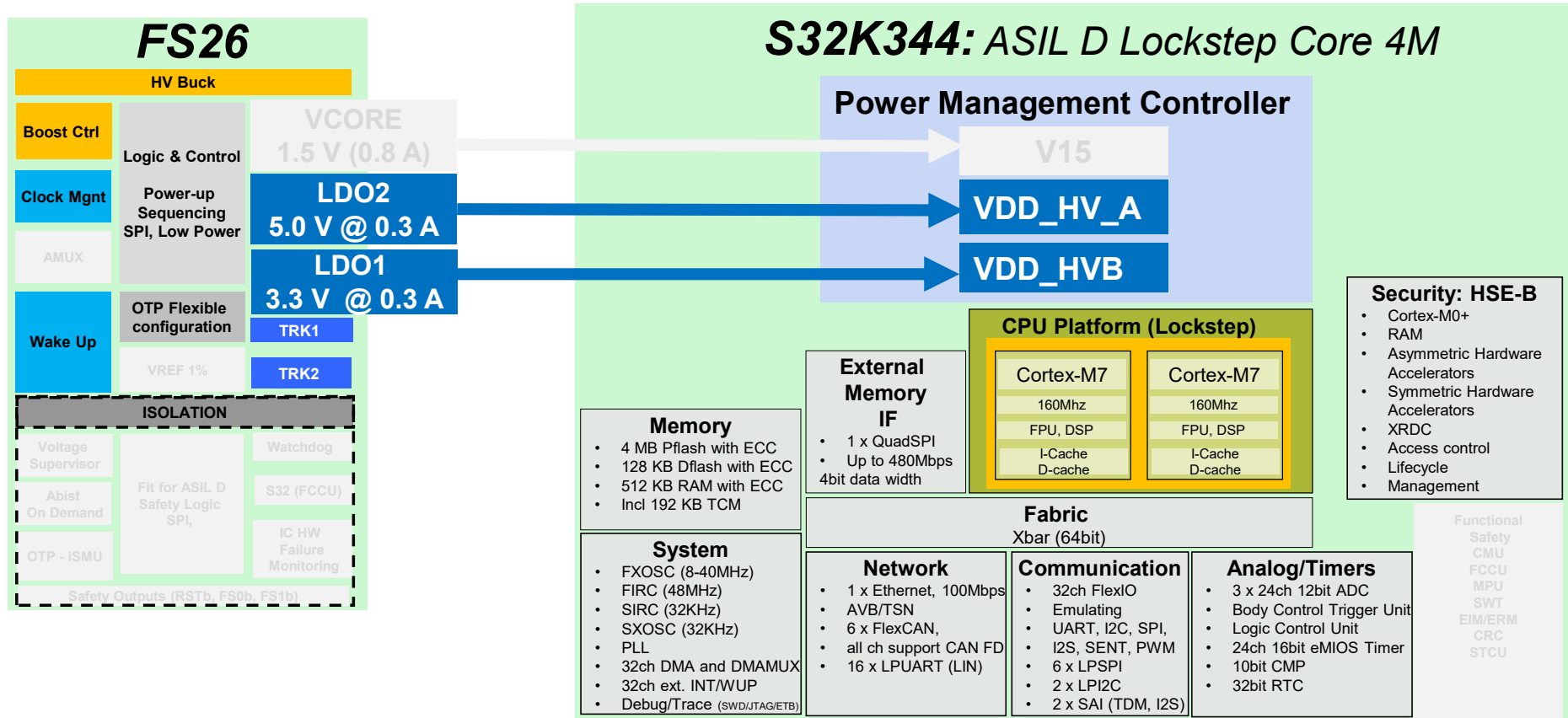


➔ **FS2630 offers adequate S32K32x and S32K34x power rails**

S32K3 FS26 ATTACH, RUN MODE

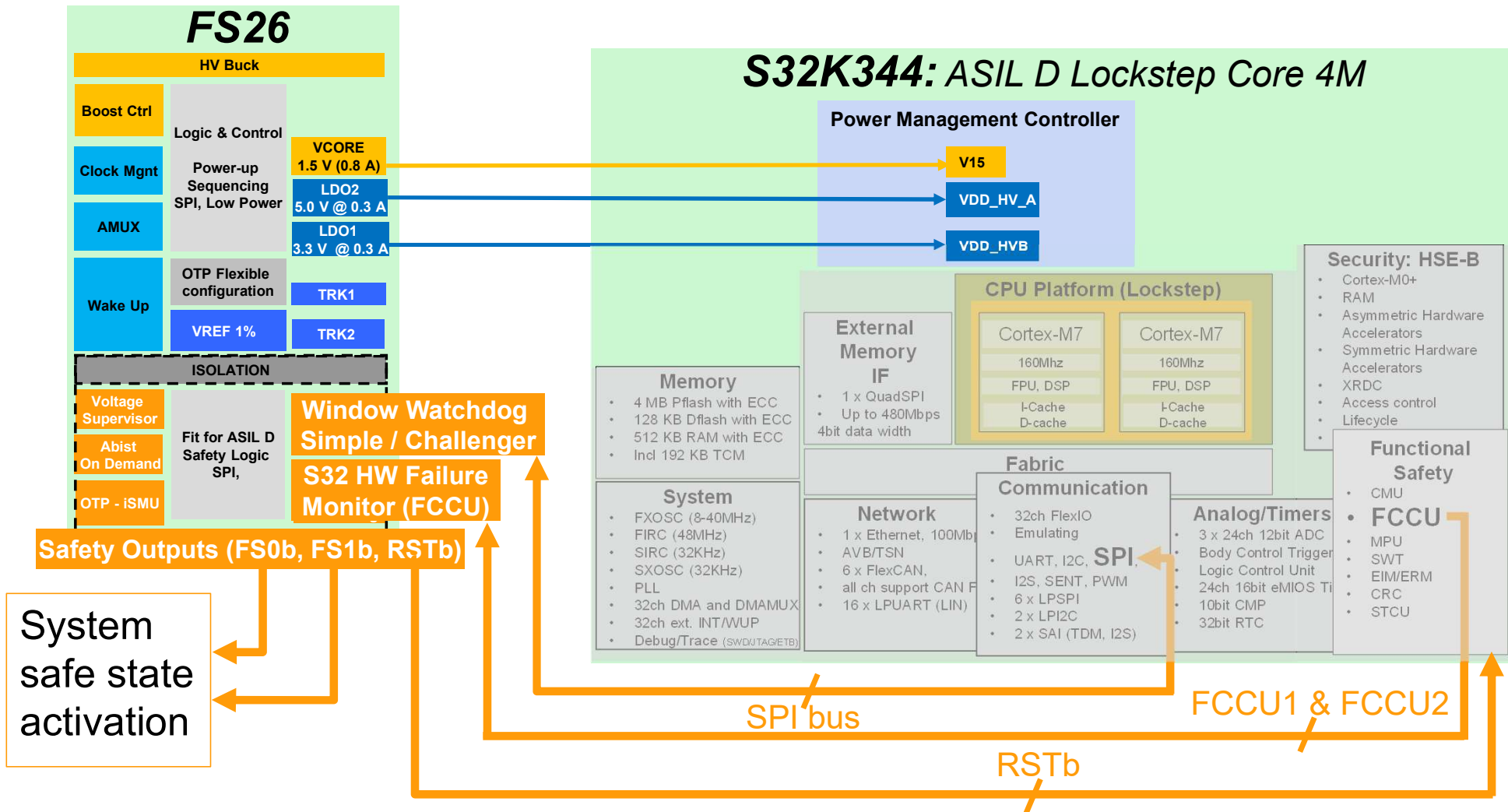


S32K3 FS26 ATTACH, STANDBY MODE



→ FS2630 supports S32K3 Standby mode. All (SBC and MCU) safety mechanisms disabled in low power mode

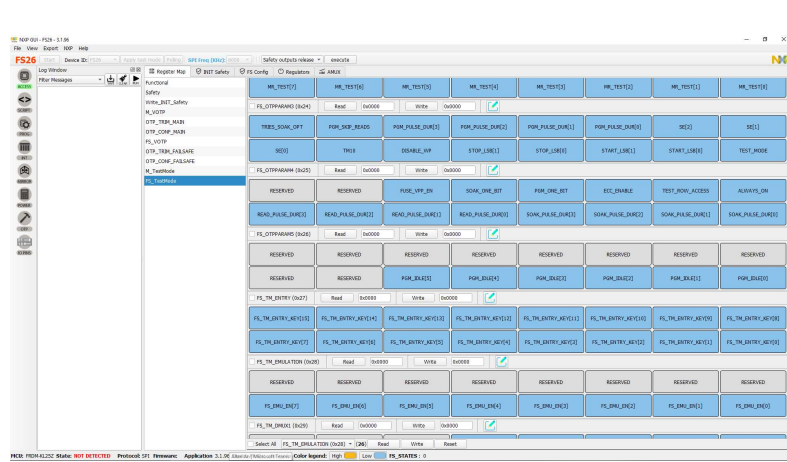
S32K3 + FS26 FUNCTIONAL SAFETY





ENABLEMENT STATUS

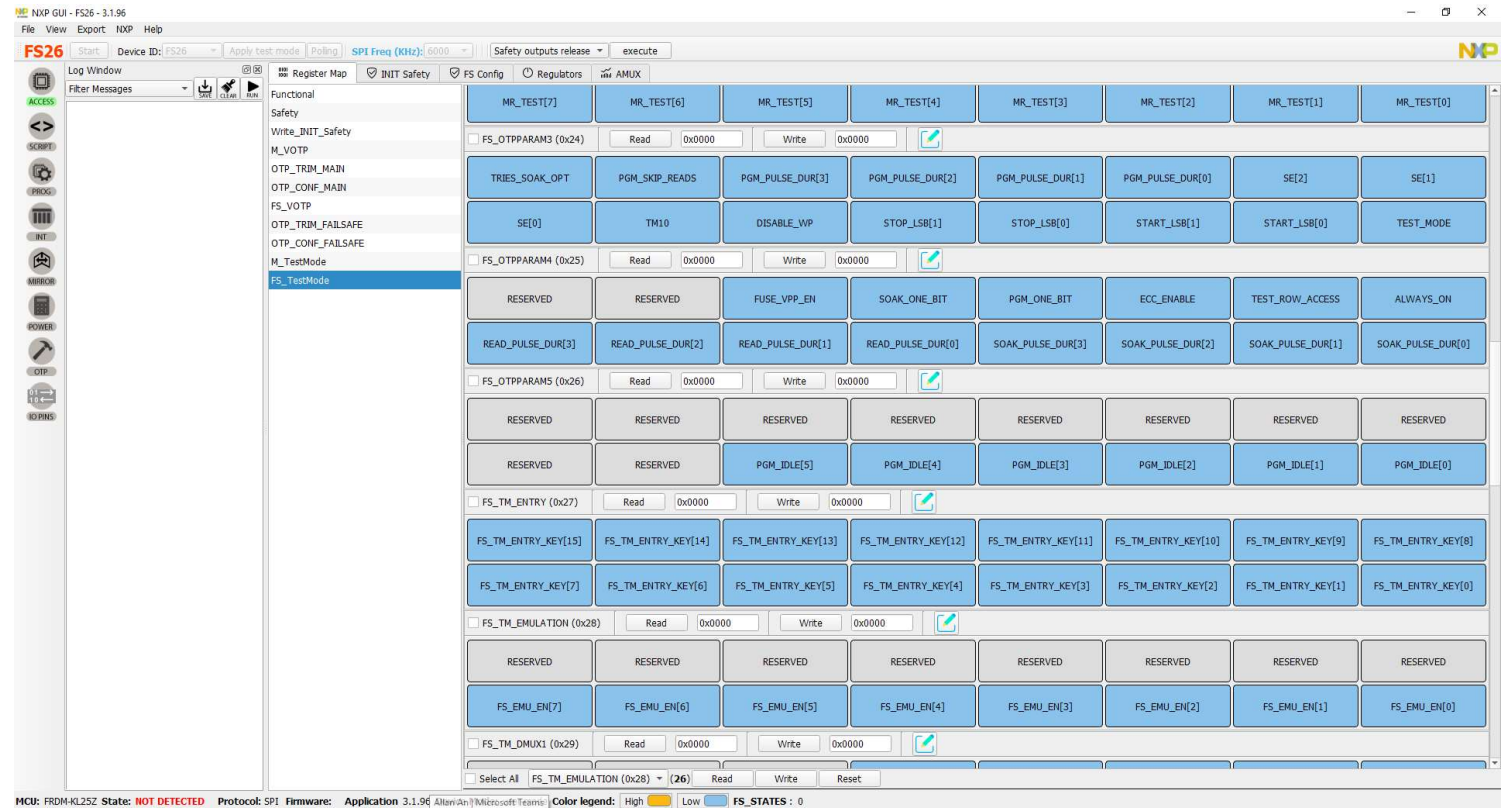
FS26 ENABLEMENT



Product	Type	Status	Link
Data Sheet	Document	available	DocStore
Safety Manual	Document	available	DocStore
FMEDA	Document	available	DocStore
Application note	Document	Available	DocStore
Socket EVB schematic and Layout	Hardware	available	AAA infocenter SharePoint
Soldered EVB schematic and layout	Hardware	available	AAA infocenter SharePoint
EVB GUI	Software	available	AAA infocenter SharePoint
OTP tool	Software	available	AAA infocenter SharePoint
Power dissipation calculator	Software	Available	AAA infocenter SharePoint
Safety Application Note	Document	Available	DocStore

EVALUATION INTEGRATED INTERFACE - NXP GUI

- ✓ Register map access
- ✓ Script editor
- ✓ OTP emulation
- ✓ OTP programming
- ✓ Power calculator
- ✓ OTP tool

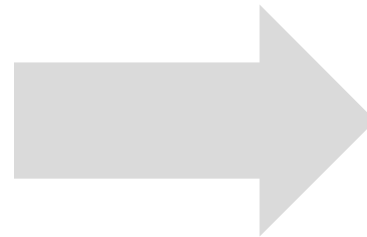
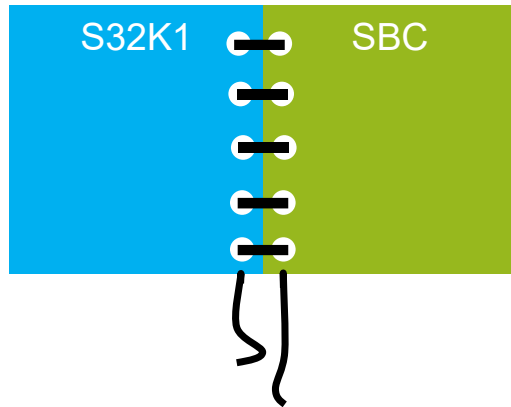


NXP MCU + SBC CHIPSET SOLUTIONS

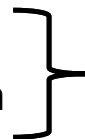
Ease-of-use

Chipset Solutions

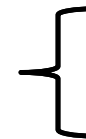
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- Software Drivers
- S32K SDK integration

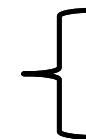


Value-add



- Safety concept and safety manual
- Low power and debug concept

Ease-of-use



- Software Drivers
- S32K SDK + Design Studio SBC integration

NXP Safety PMIC's DNA



Safe



Scalable



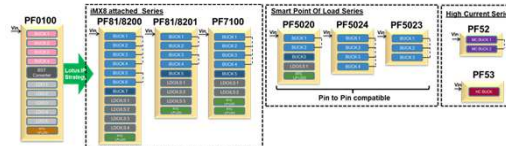
Expandable

➤ 3rd Generation of Safety PMIC

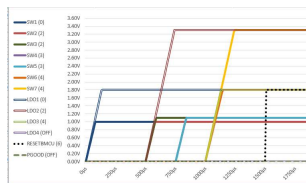


- Safety Scalability
QM, ASILB, ASIL D

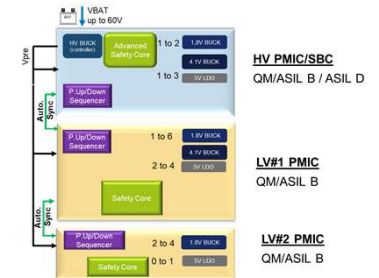
➤ Power Scalability



➤ Device Flexibility thanks to OTP



➤ “Building Blocks” portfolio



➤ Power & Safety expandability

ASIL D	HV	HV + LV1	HV + LV1	+ LV2
ASIL B	HV	HV + LV1	HV + LV1	+ LV2
QM	HV	HV + LV1	HV1 + LV1	+LV2

System Scalability →



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