AN14175

使用FlexIO模拟Quad SPI主设备

第1.0版—2024年1月20日 **应用笔记**

文档信息

信息	内容
关键词	AN14175、FlexIO模块、板接口、MCX-N947-EVK、i.MX RT595-EVK硬件平台、单工Quad SPI主设备、LCD驱动器
摘要	本应用笔记介绍了在MCX-N947-EVK或i.MX RT595-EVK硬件平台上，将Flex IO外设作为单工Quad SPI主设备来驱动LCD显示器的实现方法。

1 介绍

FlexIO是一种集成在Kinetis、S32K、i.MX RT和MCX微控制器系列中的片上外设。它具有高度可配置性，能够模拟多种通信协议，如UART、I2C、SPI、I2S和LIN等。这些协议的详细信息请参阅nxp.com.cn官网中的应用笔记《使用FlexIO模拟通信和定时外设》（AN12174）。此外，FlexIO还可用于模拟其他协议，如J1850、I3C和曼彻斯特编码等。

FlexIO作为独立外设模块，可用作微控制器的一个附加外设模块，但不会替代任何现有的通信外设。FlexIO的主要特点是，用户可以根据需求来构建自己的外设。

本应用笔记介绍了在恩智浦提供的MCX-N947-EVK和i.MX RT595-EVK硬件平台上，如何实现单工Quad SPI主设备以驱动LCD显示器。尽管半双工或全双工的QSPI也应该是可行的，但这不在本应用笔记的讨论范围之内。

2 FlexIO模块的概述

FlexIO模块有以下主要硬件资源：

- 移位器
- 定时器
- 引脚

图1所示为FlexIO模块的概览图。

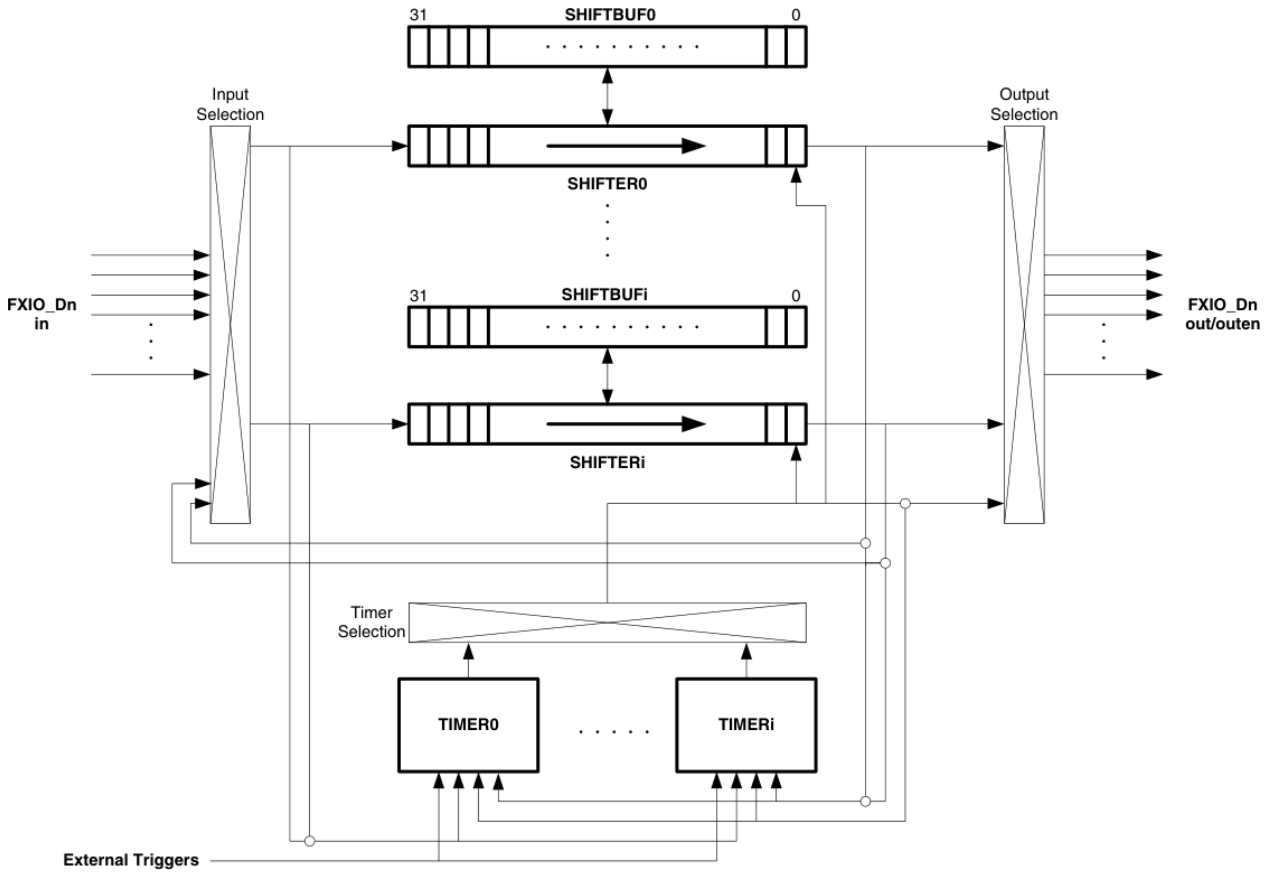

图1. FlexIO的结构框图

它提供以下主要功能：

- 32位移位器，支持发送、接收和数据匹配模式
- 双缓冲移位器操作
- 16位定时器，具有高度灵活性，支持各种内外部触发以及复位/启用/禁用/递减条件
- 自动起始/停止位的生成/检查
- 中断、DMA或轮询模式运行
- 移位器、定时器、引脚和触发器可灵活组合操作

发送和接收是移位器的两种基本模式。如果移位器被配置为发送模式，它会从缓冲寄存器中加载数据，并将数据逐位输出到指定的引脚。如果移位器被配置为接收模式，它会从指定的引脚接收数据并将数据存储在其缓冲寄存器中。移位器指定的定时器负责控制所有的加载、存储和移位操作。定时器还可以根据需求配置为不同的工作模式，包括双8位计数器的波特率/位模式、双8位计数器PWM模式和单16位计数器模式。

如需了解更多详细信息，请参阅nxp.com.cn上的AN12174应用笔记和相应芯片的《参考手册》。

3 使用FlexIO模拟Quad SPI主设备

3.1 要求

图2所示为一个工程的预期波形。

该通讯从命令信号（一个字节）和地址信号（三个字节）开始。在数据的头部和尾部，都会插入一个空周期（一个字节）。

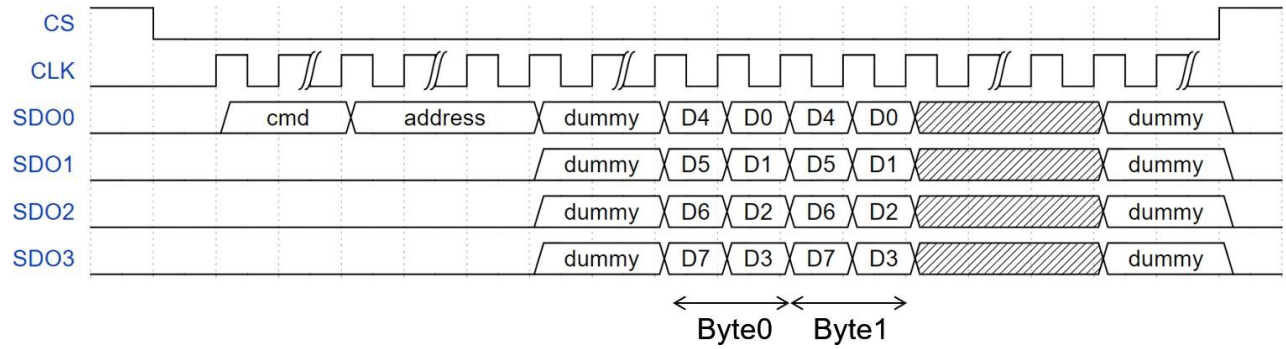

图2. FlexIO的波形

3.2 单工Quad SPI的配置

它的基本概念与普通SPI的概念相同。（AN12174）。移位器0用作Quad SPI主设备的发送器。表1列出了具体配置。

表1. 移位器0的配置

项目	配置
移位器模式	发送
定时器选择	定时器0
定时器极性	在时钟信号的负跳变边沿触发
引脚配置	引脚输出
引脚极性	高电平有效
引脚宽度	**3**
输入源	来自引脚
起始位	禁用，发送器在启用时加载数据
停止位	禁用
所用的缓冲器	半字节交换寄存器

主要的不同之处在于PWIDTH（引脚宽度）寄存器。通过将PWIDTH寄存器的值配置为3，每个周期将移位4位，从而实现并行的四路输出。以下是设置宽度的示例代码。另请参见图3。

```
/* Configure the shifter 0 for tx. */
            shifterConfig.timerSelect = kFLEXIO_QSPI_TIMER0;
            shifterConfig.pinConfig   = kFLEXIO_PinConfigOutput;
            shifterConfig.pinSelect   = base->SDOPinIndex;
            shifterConfig.pinPolarity = kFLEXIO_PinActiveHigh;
```

```
            shifterConfig.shifterMode = kFLEXIO_ShifterModeTransmit;
            shifterConfig.inputSource = kFLEXIO_ShifterInputFromPin;
            shifterConfig.parallelWidth = 3;
            if (masterConfig->phase == kFLEXIO_SPI_ClockPhaseFirstEdge)
            {
            shifterConfig.timerPolarity =
kFLEXIO_ShifterTimerPolarityOnNegitive;
            shifterConfig.shifterStop   = kFLEXIO_ShifterStopBitDisable;
            shifterConfig.shifterStart  =
kFLEXIO_ShifterStartBitDisabledLoadDataOnEnable;
            }
            else
            {
            shifterConfig.timerPolarity =
kFLEXIO_ShifterTimerPolarityOnPositive;
            shifterConfig.shifterStop   = kFLEXIO_ShifterStopBitLow;
            shifterConfig.shifterStart  =
kFLEXIO_ShifterStartBitDisabledLoadDataOnShift;
            }

            FLEXIO_SetShifterConfig(base->flexioBase, kFLEXIO_QSPI_SHIFTBUF0,
&shifterConfig);
```

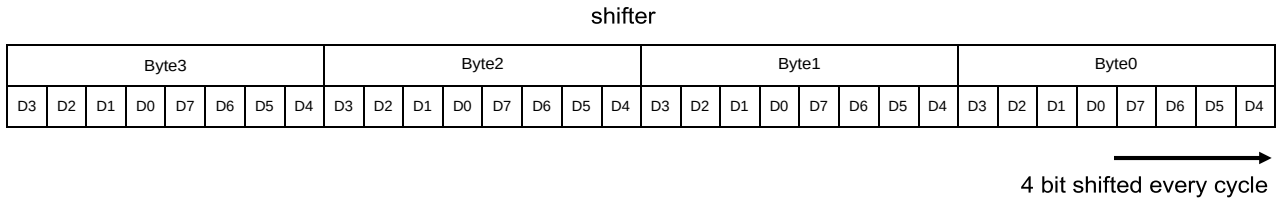

图3. PWIDTH寄存器

为了将半字节交换的数据存储到移位缓冲器，使用SHIFTBUFNBS（移位缓冲器N半字节交换）寄存器。请参阅表2。

表2. SHIFBUFNBS寄存器

字段	说明
31-0 SHIFTBUFNBS	移位缓冲器 与SHIFTBUF寄存器不同，对该寄存器的读/写操作会在每个字节内进行半字节交换。 读取时返回{SHIFTBUF[27:24]、SHIFTBUF[31:28]、SHIFTBUF[19:16]、SHIFTBUF[23:20]、SHIFTBUF[11:8]、SHIFTBUF[15:12]、SHIFTBUF[3:0]和SHIFTBUF[7:4]}。

- 定时器0由Quad SPI主设备用来生成时钟输出并控制移位器的加载/存储/移位。
- 定时器1用于生成片选输出。

有关定时器0或定时器1配置的更多信息，请参阅nxp.com.cn网站上的AN12174应用笔记。

4 软件实施概述

i.MX RT595-EVK和MCX-N947-EVK板用于测试驱动程序。

i.MX RT595软件示例支持SmartDMA的实现，而MCX-N947软件示例则支持eDMA的实现。SmartDMA需要一个自定义固件，以按需将数据从缓冲区移动到SHIFTBUFNBS，该固件以二进制的形式包含在`fsl_smartdma.h`中。

因此，**i.MX RT595使用：**

- `fsl_flexio_qspi.c/fsl_flexio_qspi.h`
- `fsl_flexio_qspi_smartdma.c/fsl_flexio_qspi_smartdma.h/fsl_samrtdma.c/fsl_smartdma.h`

MCX N947使用：

- `fsl_flexio_qspi.c/fsl_flexio_qspi.h`
- `fsl_flexio_qspi_edma.c/fsl_flexio_qspi_edma.h`

注： *`fsl_flexio_qspi.c/fsl_flexio_qspi.h`与RT595和MCX-N947两者兼容。*

4.1 函数说明

表3、表4和表5列出了FlexIO QSPI示例驱动程序中可用的函数。

表3. fsl_flexio_qspi.c 或 fsl_flexio_qspi.h

函数	说明
FLEXIO_QSPI_MasterGetDefaultConfig	获取FlexIO QSPI主设备的默认配置
FLEXIO_QSPI_MasterInit	为FlexIO QSPI主设备初始化FlexIO模块
FLEXIO_QSPI_MasterTransferCreate Handle	初始化用于中断模式的FlexIO QSPI主设备句柄
FLEXIO_QSPI_MasterTransferNonBlocking	以中断模式开始传输

表4. fsl_flexio_qspi_smartdma.c 或 fsl_flexio_qspi_smartdma.h

函数	说明
FLEXIO_QSPI_TransferCreateHandle SMARTDMA	初始化用于SmartDMA模式的FlexIO QSPI主设备句柄
FLEXIO_QSPI_TransferSMARTDMA	以SmartDMA模式开始传输

表5. fsl_flexio_qspi_edma.c 或 fsl_flexio_qspi_edma.h

函数	说明
FLEXIO_QSPI_MasterTransferCreateHandleEDMA	初始化用于eDMA模式的FlexIO QSPI主设备句柄
FLEXIO_QSPI_MasterTransferEDMA	以eDMA模式开始传输

4.2 运行演示

本演示在i.MX RT595-EVK和MCX-N947-EVK上运行。请参见表6。

注:

- *本例中MCX-N947-EVK所用的引脚布局与MCX-N5XX-EVK和FRDM-MCX-N947完全兼容。因此，该例可在上述任意MCX评估平台上正常运行。*

在通过J-link或CMSIS-DAP将程序镜像下载到MCU之前，请确保将Quad SPI主设备和Flexcomm SPI从设备信号连接到同一板上。必须如图4所示进行连接。

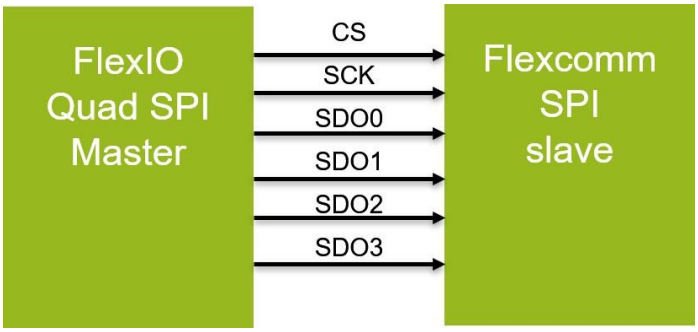

图4. 导线的连接

表6和表7所示为CS、SCK、SDO0、SDO1、SDO2和SDO3的FlexIO引脚分配。

表6. QuadSPI主设备的引脚分配

引脚分配	i.MX-RT595-EVK	MCX-N947-EVK
CS	J28-2	J20-24
SCK	J28-1	J20-23
SDO0	J28-3	J20-25
SDO1	J28-4	J20-26
SDO2	J28-5	J20-27
SDO3	J28-6	J20-28

表7. Flexcomm SPI从设备的引脚分配

引脚分配	i.MX RT595-EVK	MCX-N947-EVK
CS	JP26-1	J2-6
SCK	JP26-4	J2-12
MOSI	JP26-2	J2-10

注: *如果使用的是 i.MX RT595-EVK板，则必须断开JS23 1-2的连接，并将 JS23-2连接到 JP23-3，从而为VDDIO_3提供 1.8V电压。*

SPI无法一次接收所有的SDO0-SDO3位，但可以逐位接收SDOx位并对其进行验证。

调试控制台上收到的验证结果如图5所示。在本例中，SDO0连接到SPI从设备。可以看到SPI从设备已正常接收到与SDO0匹配的数据。

```
FLEXIO Master SmartDMA - SPI Slave edma example start.
This example use one flexio spi as master and one spi instance as slave on one board.
Master uses SmartDMA and slave uses edma way.
Please make sure you make the correct line connection. Basically, the connection is:
FLEXIO_QSPI_master -- SPI_slave
   SCK      --    SCK
   PCS0     --    PCS0
   MOSI     --    MOSI
   MISO     --    MISO
This is SPI slave call back.
This is QSPI Master call back.
FLEXIO QSPI master[0] <-> SPI slave transfer all data matched!
```

图5. MOSI连接到SDO0时的调试控制台

5 用逻辑分析仪所做的测量

图6和图7显示了用逻辑分析仪测得的信号输出结果。输出完全符合工程的要求。通信协议可根据所连接的设备进行定制。

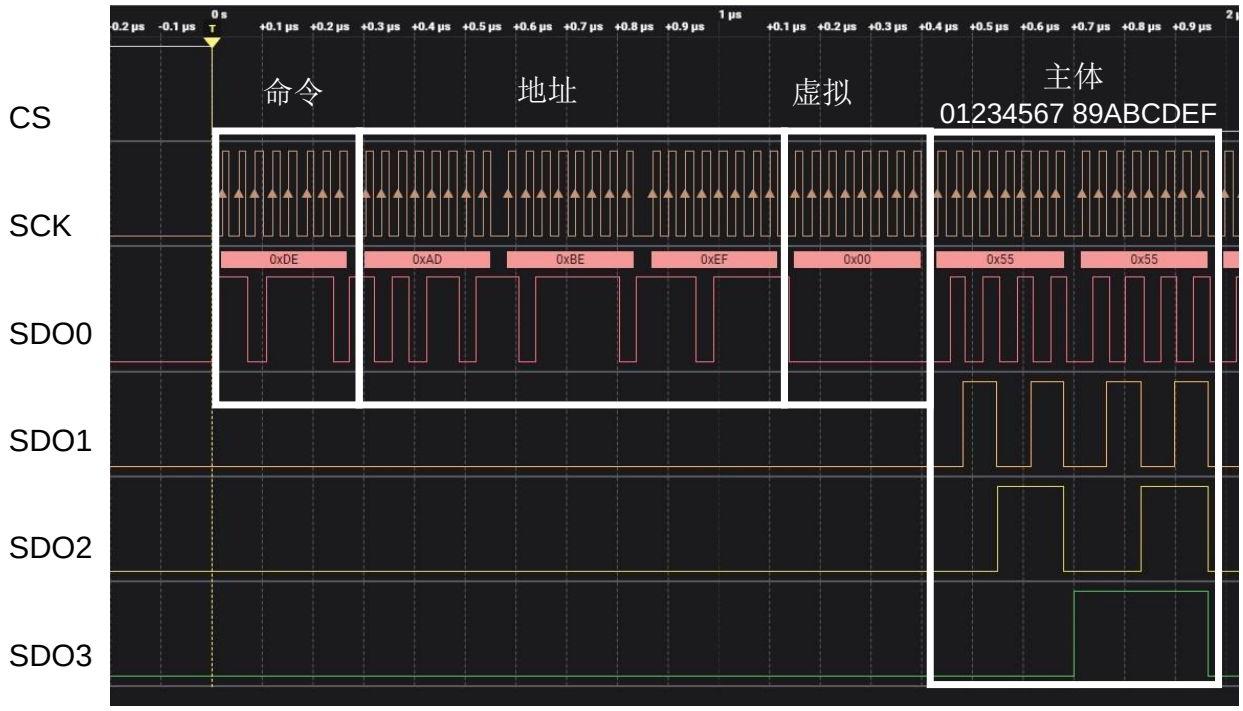

图6. 命令 + 地址+ 空字节 + 主体

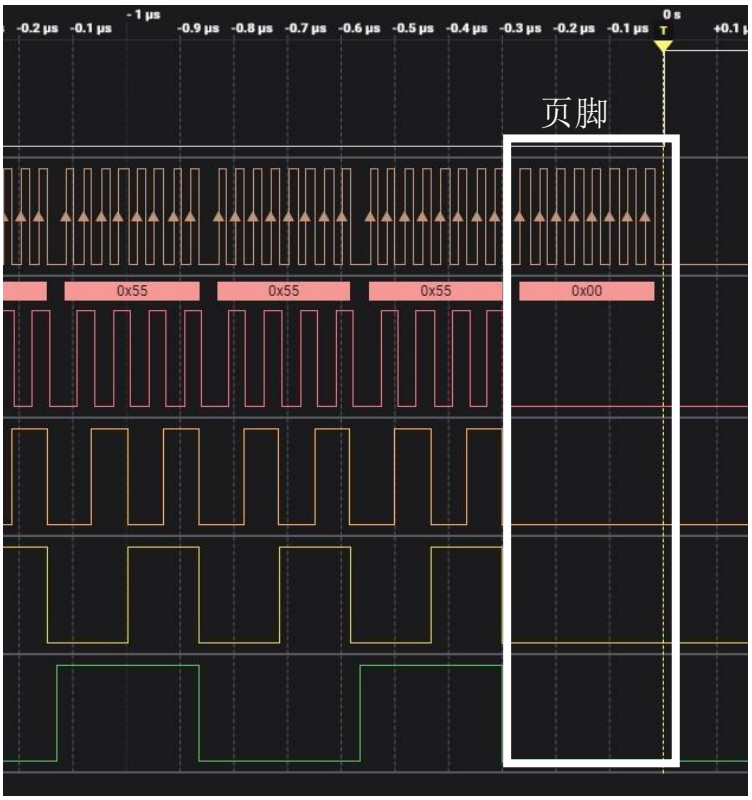

图7. 波形尾

6 结论

本应用笔记介绍了在i.MX RT和MCX平台上的单工Quad SPI主设备的实现。FlexIO是一种灵活的模块，不仅可用于设计SPI或I2C等常见接口，还可通过组合移位器和定时器来设计专有接口。

7 相关文档

如需了解更多信，请参阅以下链接中的文档：

- https://www.nxp.com.cn/design/design-center/development-boards/i-mx-evaluation-and-development-boards/i-mx-rt595-evaluation-kit:MIMXRT595-EVK#documentation
- https://www.nxp.com.cn/products/processors-and-microcontrollers/arm-microcontrollers/general-purpose-mcus/mcx-arm-cortex-m/mcx-n94x-and-n54x-mcus-with-dual-core-arm-cortex-m33-eiq-neutron-npu-and-edgelock-secure-enclave-core-profile:MCX-N94X-N54X#documentation
- https://community.nxp.com/t5/Kinetis-Microcontrollers/Understanding-FlexIO/ta-p/1115419
- nxp.com.cn上的AN12174。
- nxp.com.cn上相应芯片的参考手册。

8 缩略语

表8列出了本文所用的缩略语。

表8. 缩略语

缩略语	说明
DMA	直接内存访问
PWM	脉宽调制
SPI	串行外设接口
QSPI	四线串行外设接口

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10 修订历史

表9总结了本文的修订情况。

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文档ID	发布日期	说明
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