Freescale Semiconductor
Solution Guide

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Using the PowerQUICC™ II Pro MPC8360E and DSPs Based on StarCore Technology to Design a Media Gateway

As growth in data network traffic drives major changes in public networks, the convergence of existing voice traffic onto the data network infrastructure promises significant benefits, such as reduced costs and simplified network management, for both carriers and enterprises. The media gateways and switches that support the integration of Voice over Internet Protocol (VoIP), legacy public switched telephone network (PSTN), and ATM networks make this convergence possible, as Figure 1 shows.

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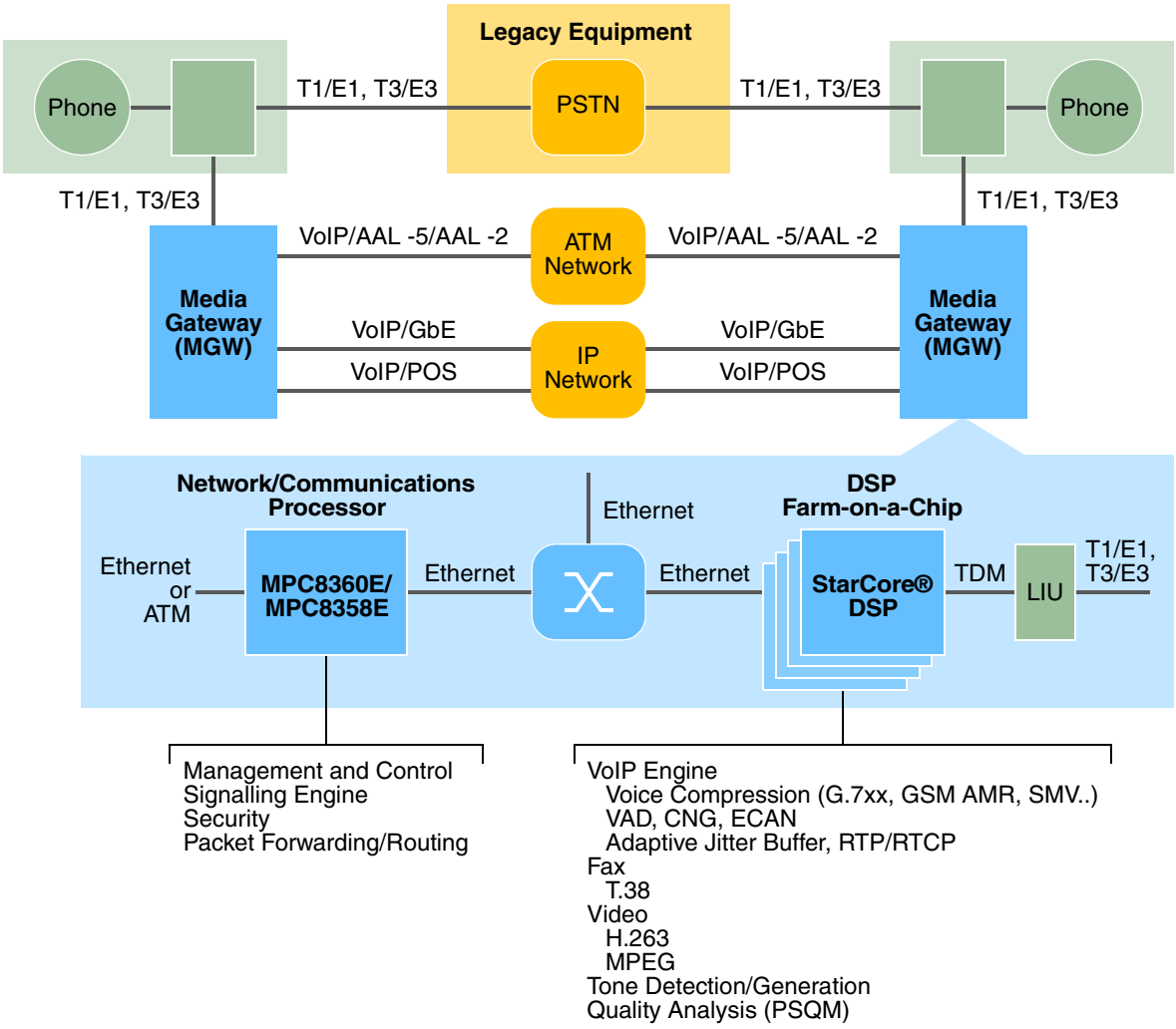


Figure 1. Media Gateway

Traditionally, companies maintain two separate communications networks—one for voice and one for data—but the Internet Protocol (IP) networking evolution means these services are changing for both users and service providers. By delivering voice in IP packets to the desktop over the LAN, VoIP now both allows and necessitates the convergence of these two networks.

Corporate network communication strategies increasingly use VoIP as a means to enable new applications. In time, VoIP will be predominant form of enterprise voice. The need to support only one network promises substantial cost savings, but the greatest opportunity lies in the ability to deploy and integrate new productivity applications and enhanced voice services such as the following:

- IP-based call centers allowing mobility, messaging and management over IP
- Hosted voice in the form of hosted IP PBXs and IP Centrex
- Network-based voice-enabled IP VPN services offering enhanced voice features to remote offices and telecommuters

Within Enterprise LAN, convergence onto a single IP/Ethernet packet network may be inevitable, but it is not as certain that this convergence will apply to the Metro or Long Haul Transport. Carriers have used Synchronous

Optical Network (SONET) and Asynchronous Transfer Mode (ATM) to deploy WAN services. Both technologies have rich feature sets including quality of service, high speed and availability, service differentiation and Operations, Administration and Management (OAM).

However, with increased bandwidth and numerous IEEE standards, Ethernet can now address these requirements and provide connectivity across the MAN or WAN and between LAN environments. Already the de-facto Layer 3 standard for delivering e-commerce and other web-base services such as data, voice and video, IP has used Ethernet as the preferred medium for routing and switching. With the wider network shifting towards all-IP, Ethernet deployment is expected to become the dominant Layer 2 protocol. It is supported within fibre, copper, and wireless, and it has bandwidth support ranging from 10Mbps up to 10Gb. The different media and varying bandwidth increases flexibility in deploying Ethernet based network solutions.

IEEE standards support such as 802.1q Virtual LAN (VLAN) and 802.1p Class of Service (CoS) have made Ethernet more robust and resilient. With these two standards, carriers can deliver high-priority, low-latency VLAN-based services such as Voice. VLAN allows logical network partitioning. Voice services and Data services are carried on separate VLANs, which in turn have different CoS gradings. Voice has a high CoS ensuring low latency and less jitter. This simple labelling approach is augmented by the IETF sponsored Differentiated Services (DiffServ) protocol, which uses an indication of how a given packet is to be forwarded, known as the Per Hop Behavior (PHB). The PHB describes a particular service level in terms of bandwidth, queuing theory, and dropping (discarding the packet) decisions.

In general terms, network services that need highly reliable connections use TCP/IP, but those that need real-time delivery like Voice and Video use UDP/IP. However, the threat of Denial of Service (DoS) and call snooping have clouded that picture somewhat. VoIP security is now fundamental and the solution lies in the standards. Securing the call signalling channels allows a call to be authenticated and set up securely between two parties. Standards define the use of the Secure Sockets Layer (SSL) and/or Transport Layer Security (TLS) protocols to secure Session Initiation Protocol (SIP) over TCP, as well as H.323 with H.325 VoIP sessions. While these call signalling protocols use SSL/TLS over TCP/IP, the voice data is sent over an unreliable packet-based network—UDP/IP. While SSL/TLS can be used to implement Secure RTP or Datagram TLS, it carries a significant performance cost.

Due to factors such as built-in QoS, ATM remains strong as a Metro and Long Haul transport technology. Any Media Gateway system solution would be incomplete without support for ATM. VoATM is therefore still a valid scenario, whether it be VoIP over AAL-5 over ATM (VoIPoAAL5) or VoAAL2.

While ATM Adaptation Layer 1 (AAL1) is able to carry voice over individual Constant Bit Rate (CBR) links, the bandwidth reducing features of AAL2 make it a more suitable option for major installations. AAL2 was developed specifically for transporting real-time Variable Bit Rate (VBR) traffic, e.g. voice traffic with silence detection. By allowing multiple VBR voice calls to share a single ATM virtual circuit and by using silence suppression, AAL2 can offer very significant bandwidth savings on top of those gained during voice compression.

A simpler solution—but one that is more costly in bandwidth terms—is to use AAL5 to carry the voice indirectly. Many Frame Relay and IP networks have ATM backbones which use AAL5 at the edge to segment and reassemble the traffic to/from ATM cells. Voice packets are not necessarily distinguishable from packets containing data and are therefore sent over ATM using AAL5 by default.

The Enterprise or Media gateway is instrumental in enabling IP convergence. Gateway functions are being implemented in standalone devices, as modules in multi-service switches, in edge routers, in remote access concentrators, or in PSTN switches. In all cases, they share a common set of hardware and software design challenges.

1 Design Challenges

With the potential to offer three revenue streams from a single IP packet network, the triple play of voice, video and data is the goal of every telecoms operator. IP is the key enabler toward this goal. In time, it will be universal. Until then, equipment has to inter-operate not only between circuit and packet-switched networks but also between many standards and protocols.

The media gateway is a classic example of the requirement to interoperate between different networks and standards due to the wide variety of technologies that make up existing networks. These include the circuit-switched PSTN, ATM and Frame Relay based public data networks, and IP packet networks, all of which may be carried over the same SONET transport network.

Functions required of media gateways typically include the conversion and compression of time-division-multiplexed (TDM) voice circuits onto ATM networks using a variety of adaptation protocols (AAL0, AAL1, AAL2 and AAL5) or onto packet-based networks using IP (including RTP), frame relay, or extensions of both. Voice switches that support the switching of voice circuits among the various network interfaces may require interworking between different protocols as well.

The specific design challenges for media gateways include the following:

- Accommodating increasing numbers of voice (or fax and modem) circuits per slot within a specific networking device
- Supporting the increasing number of different network interfaces and speeds required, ranging from channelized T1/E1 lines through OC-12 SONET and Gigabit Ethernet interfaces
- Adapting to the number of different protocols used (such as ATM AAL2/AAL5, VoIP/RTP, Packet-over-SONET/PPP, MPLS, and so on), even as the protocol standards evolve and improve
- Providing the flexibility to add new features and functions through software as market demands dictate in the future

2 Freescale Semiconductor Solutions

Freescale Semiconductor offers complete solutions for all aspects of media gateway and switch implementations. This includes the Freescale’s Digital Signal Processors (DSPs) based on StarCore technology required to convert and compress TDM voice circuits into packet or cell-based flows, the PowerQUICC communications processors required to terminate or switch the packet or cell-based circuits, and if required, PowerPC host processors to implement the control functions that manage each voice connection.

The proven and evolving PowerQUICC communications processors form a key element to Freescale's VoIP offering. The versatile PowerQUICC delivers functionality tailored to meet the needs of the embedded communications market space, excelling not only in VoIP systems but also in today’s and tomorrow’s networking and wired and wireless access equipment.Target applications include MTUs, DSLAMs, wireless base stations, multi and fixed subscriber access nodes, add/drop multiplexers and routers. Each PowerQUICC provides a cost-effective mix of performance and System-on-Chip (SoC) integration with a 32-bit embedded PowerPC core, a powerful memory controller, and system connectivity options, as well as a wide range of networking and protocol support including OC-12 ATM/POS and Ethernet options ranging from dual-10/100 to quad-1Gb. The separate RISC-based communication module not only handles the Layer 2 protocols but is also capable of accelerating packet processing by offloading even more of the protocol handling from the CPU. This potential promises to deliver even greater performance. An integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9 and ARC-4 encryption algorithms further enhances the feature set for an even wider range of applications.

The latest additions to the PowerQUICC family—the PowerQUICC II Pro MPC8360E and MPC8358E—take this to a new level by integrating the next generation communications engine (QUICC Engine) to provide accelerated and customizable packet processing and protocol interworking. Dual 32-bit DDR controllers (on MPC8360E) provide an elegant extension to the memory control capabilities ensuring high speed memory access. Figure 2 shows a block diagram of the PowerQUICC II Pro MPC8360E.

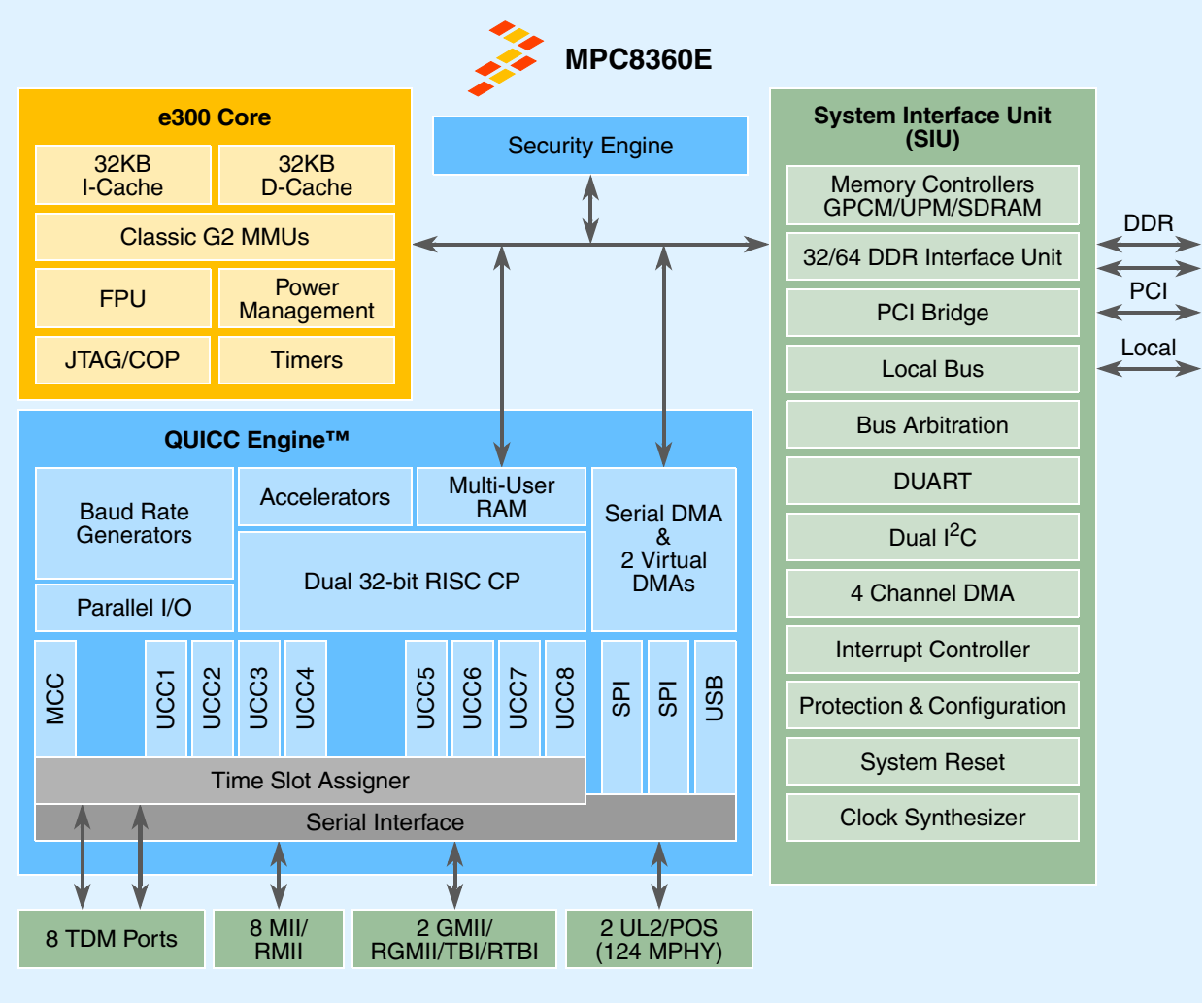


Figure 2. MPC8360E Block Diagram

A new communications complex—the QUICC Engine™—forms the heart of the networking capability of the MPC8360E. The QUICC Engine contains several peripheral controllers and integrates two 32-bit RISC controllers. Each RISC controller can control multiple peripherals and work together to provide increased aggregated system bandwidth for higher throughput applications. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs) and multi-channel communication controller (MCC).

Each of the eight UCCs can support a variety of communication protocols: 10/100/1000 Mbps Ethernet through a Media-Independent Interface, ATM / POS PHY support up to OC-12 speeds, Serial ATM, Multi-PHY ATM, HDLC, UART, Multi-Link/Class PPP, BISYNC and 64 TDM channels. Each MCC is capable of supporting up to 256 TDM channels in either transparent or HDLC channel modes and multiplexing almost any combination of sub-groups into a single or multiple TDM stream. Inverse Multiplexing over ATM is supported and allows ATM traffic to be

distributed across multiple E1/T1 circuits. This allows service providers to lease the exact bandwidth that subscriber's request.

In addition, the QUICC Engine can also support two UTOPIA level 2 or two POS interfaces, each interface capable of supporting 124 Multi-PHY, or up to two, 128 Multi-PHY interfaces using extended address mode. The QUICC Engine also features an integrated 8-port, L2 Ethernet switch which can provide 4 priority levels on each port, VLAN functionality, IGMP snooping, network auto-negotiation function, store-and-forward switching and packet-error filtering. Enhanced interworking features within the QUICC Engine helps offload the main CPU. The QUICC Engine can provide ATM-to-ATM switching, Ethernet to ATM switching with L3 / L4 support and PPP interworking.

The MPC8360E's security engine allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, MD-5, and ARC-4 algorithms. It includes a public key accelerator and an on-chip random number generator.

For DSP options, both the MSC81xx and MSC71xx families provide Ethernet solutions. The MSC8122 takes full advantage of the scalable StarCore architecture to provide a "DSP-Farm-on-a-chip" level of performance integration. The raw processing power of this highly integrated system-on-a-chip device enables developers to create next-generation networking products that offer tremendous channel densities, while maintaining system flexibility, scalability and upgradeability. Using the latest process technologies to drive both low core voltage and low power dissipation, the quad-core MSC8122 can deliver up to 8000 DSP MMACS performance at up to 500MHz, yielding a performance equal to 2.0GHz.

Although the new MSC71xx-series of DSPs are useful for any 16-bit fixed point signal processing, they are especially suited for Packet Telephony. Priced relatively low for high-performance DSPs, the MSC71xx family integrates the 1200 MMAC SC1400 (at 300MHz) synthesizable core with a glueless DDR SDRAM interface and large amount of on-chip SRAM. Several of the chips have Ethernet support, thereby enabling the DSP to be connected to the rest of the system via low-cost Ethernet switches.

Combining Freescale's next generation MPC8360E communication processor with StarCore DSP-based reference designs means Freescale can offer all of this in a turn-key system solution. One architecture, one software, from low to high density. Freescale's open software architecture preserves manufacturer's differentiation and intellectual property investment, improves time-to-market and saves product development resources, allows leverage of software applications across product lines and abstracts the developer from the underlying DSP, allowing easier code portability.

2.1 The PowerQUICC II Pro MPC8360E

The PowerQUICC II Pro MPC8360E is a high performance, highly integrated communication processor solution that offers the following.

2.1.1 MPC8360E Features

- High-performance, low power (< 5W typical power dissipation), and cost-effective communications processor
- The MPC8360E QUICC Engine offers a future proof solution for next generation designs by supporting programmable protocol termination, network interface termination, and interworking features to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks, including interworking between these networks

- Simplified network interface card design with a cost-effective single chip data plane/control plane solution for ATM or IP packet processing (or both). This reduced component count, board power consumption and board real estate.
- Universal network interface card design for multiple applications, which lowers costs and reduces time-to-market
- Built-in proprietary, hardware accelerators that accelerate data plane traffic, such as interworking, and control plane packet snooping, such as IGMP, VLAN tagging, DHCP, and so on
- DDR memory controller—one 64-bit or 2x32-bit interfaces that split data and control plane traffic at up to 333 MHz
- e300 PowerPC core (enhanced version of 603e core with 32K bytes of Level 1 Instruction and 32K bytes of Level 1 Data caches)
- 32-bit PCI interface
- 32-bit Local Bus interface
- USB
- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS
  - QoS types of traffic, such as voice, video, and data
- Security engine provides termination or encrypted plane traffic
- High degree of software compatibility with previous-generation PowerQUICC™ processor-based designs for backward compatibility and easier software migration
- Seamless connection to PowerQUICC III family devices for increased control (CPU) application processing requirements

2.1.1.1 Protocols

- ATM SAR up to 622Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
- Support for ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
- Support for IMA and ATM Transmission Convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
- IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
- L2 Ethernet switching using MAC address or IEEE 802.1P/Q VLAN tags
- Support for ATM (AAL2/AAL5) to Ethernet (IP) Interworking
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
- Support for 256 channels or HDLC/Transparent or 128 channels of SS#7

2.1.1.2 Serial Interfaces

- Support for two UL2 / POS-PHY interfaces with 124 Multi-PHY addresses each.

- Support for two 1000Mbps Ethernet interfaces using GMII or RGMII, TBI, RTBI.
- Support for up to eight 10/100Mbps Ethernet interfaces using MII or RMII
- Support for up to eight T1 / E1 / J1 / E3 or DS-3 serial interfaces
- Support for dual UART, I²C and SPI interfaces.

2.2 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our smart network partnership alliance program, including third party protocol and signaling stack suppliers, real time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

2.2.1 Software Development Tools

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator and debugger for the e300 PowerPC core.

2.2.2 Application Development System (ADS)

Freescale will provide an ADS board as a reference platform and programming development environment of the MPC8360E and the MPC8358E. The ADS support on-board DDR SDRAM memory, a PCI interface, a debug port and can be configured with optional daughter cards supporting protocols such as OC-3 or OC-12 ATM, T1/E1 or Gigabit Ethernet. The same provision is also made for the MSC71xx and MSC81xx DSP devices.

2.2.3 Smart Packet Telephony (SPT)

At the core of Freescale's VoIP solution is the Smart Packet Telephony (SPT) developer's kit, an integrated hardware and software kit for developing packet telephony solutions, ranging from single channels right up to 1000s of channels of capacity. To maximize flexibility and possible applications, a modular platform architecture has been implemented. The kit provides a completely integrated packet telephony development and reference system, consisting of three main subsystems: a baseboard; DSP subsystem, and PSTN subsystem. The baseboard provides Ethernet, UTOPIA Level 2 and CTBus TDM interfaces, and runs all the application specific protocols required by the target application on the resident PowerQUICC communications processor. The DSP subsystem performs all signal processing functions for voice, fax and modem data applications. Typical functions include voice compression, DTMF detection, voice activity detection, echo cancellation and silence suppression, as well as modem and fax data modulation and demodulation. The PSTN subsystem connects to the DSP subsystem, and provides four narrow band T1/E1 TDM or three T3 ports. The POTS subsystem also supports four analogue POTS ports for direct interfaces to standard analogue voice terminals, and it provides a TDM stream for the DSP array.

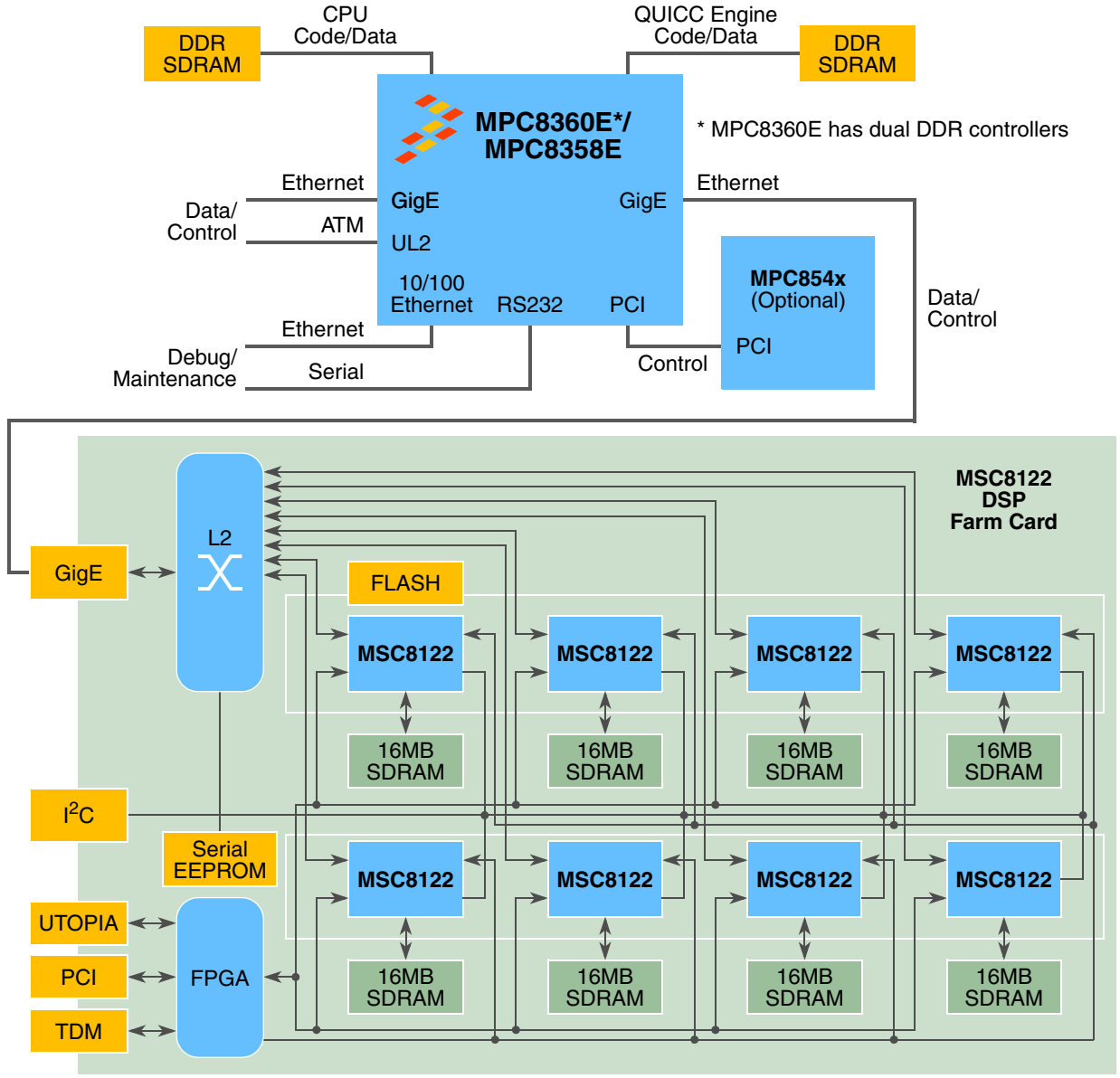
An integral part of the system is the DSP mezzanines. For future implementations, Freescale is developing a DSP mezzanine based on the Advanced Mezzanine Card format, designed to take advantage of the strengths of the new PICMG ATCA specification. It provides a hot swappable mezzanine that maximizes density through use of greater surface area, component height and higher electrical power with higher I/O bandwidth. AMC is optimized for packet based systems communicating with the carrier card via a packet based serial interface, which features up to 21 lanes of high speed I/O (12.5Gbit/s each), supporting a variety of protocols (Ethernet, Serial RapidIO, PCI Express etc.) and features integrated I2C and Ethernet based system management. This format is of course not only limited to DSP mezzanines and options for adding an MPC8360E/MPC8358E based ‘aggregator’ or host/control processing mezzanine cards exist.

While many VoIP vendors propose a closed solution, Freescale is able to offer a series of comprehensive and flexible systems solutions that seamlessly integrate VoIP functionality, delivering a single host interface, DSP software and a framework that can accommodate integration of customer software. From low to high end applications on a single DSP core architecture, customers can maintain a single code base across a wide variety of markets and applications, preserving legacy software and customizing products.

Whether developing a solution based on the Freescale design or developing your own system software in parallel with hardware design, Freescale's family of reference designs based on PowerQUICC processors and DSP based on StarCore technology, provide a proven quick to market platform for end product development. The platforms are just one of the many building blocks that can be implemented for a turnkey or customized solution for VoIP.

3 Application Example

One of the biggest challenges facing manufacturers today is minimizing time to market whilst maintaining and building key product differentiation. Overcoming these challenges requires careful selection of components to produce a competitive solution that meets the demands of service providers. Not only is the hardware choice important, the manufacturer must also consider the ecosystem surrounding the products that enable them to take their system to market quickly with minimal effort. This includes the supporting software, the tool chain and the available reference designs. An example of Freescale’s hardware solution is shown in Figure 3. The MPC8360E and MPC8358E PowerQUICC II Pro is shown combined with a MSC8122 DSP farm card.



* MPC8360E has dual DDR controllers.

Figure 3. Example Medium Density Media Gateway Reference Platform

Taking a high level view, a Media Gateway system operates on traditional time division multiplexed (TDM) voice data, converting it to and from the desired packet format. The format depends on the network protocol and could be either IP or ATM. With IP, the voice packet is formatted into a specific VoIP protocol (such as RTP), possibly tagged as part of an MPLS session, and forwarded onto an IP-based network (over Ethernet or SONET), where QoS may be guaranteed through the use of various protocols including DiffServ. ATM is suitable for carrying voice because of its native QoS features. Options for ATM processing in media gateways might include VoIPoAAL5, where voice packets from the DSPs are formatted into a specific VoIP protocol (such as RTP), which are then converted into AAL5 PDUs, and segmented into ATM cells. Alternatively, voice packets may be formatted into ATM AAL2 “mini-packets”, one or more of which are encapsulated into ATM cells.

The conversion between packet and TDM involves voice encoding or decoding using standard ITU codecs, such as G.711, to provide toll quality voice or one of the other codecs (G.723.1, G.726, and G.729A) that can provide near toll quality voice by compressing the data, thus utilizing network bandwidth more efficiently. Echo Cancellation is employed to remove near end echo that can be introduced by mismatches between hybrid impedances and low cost end user equipment. Packet networks can also introduce an array of problems, such as lost packets, packet errors, or even delayed and out of order delivery. These can all affect the quality of service (QoS) in a voice system. QoS can be maintained in these systems through the use effective jitter buffers that can deal with and overcome these issues. The voice coding and echo cancellation is most suited to a digital signal processor (DSP), and coupled with a TDM interface, it provides a connection to the PSTN network.

A PowerQUICC communications processor with the appropriate protocol interfaces provides the conduit to the packet network, performing uplink aggregation, downlink routing and if required the protocol interworking between ATM and IP. These tasks can be implemented using the integrated features of the PowerQUICC, which include the communications engine and with the embedded PowerPC core capable of handling the protocol stack and control functions Freescale has all the key hardware and software components of a VoIP System.

Combining DSPs with PowerQUICC over Ethernet is easy regardless of the system scaling. Figure 4 provides system scaling guidelines.

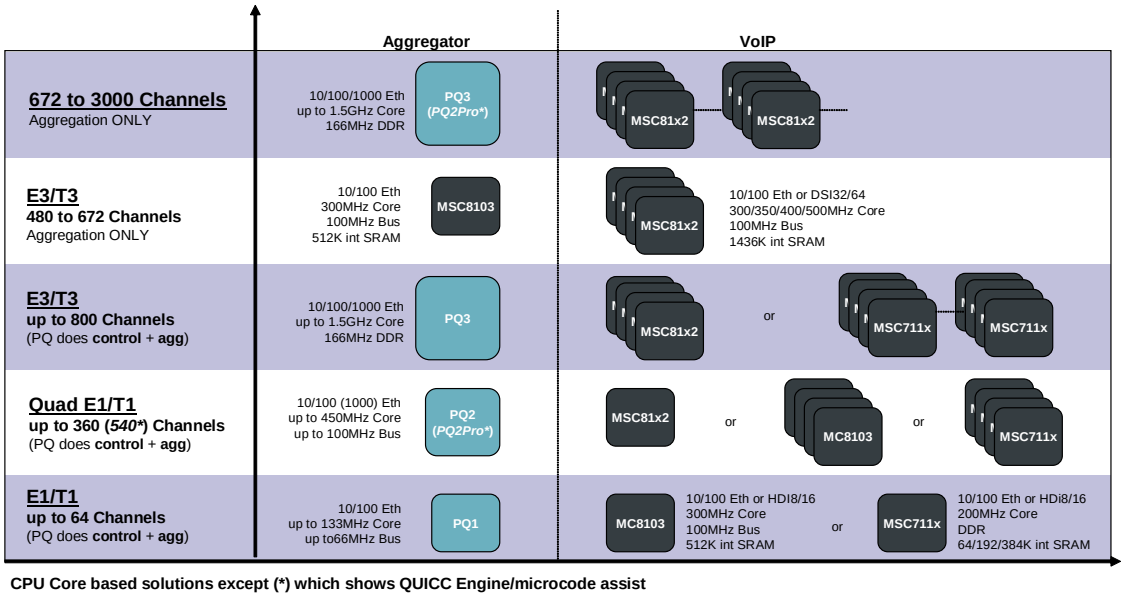


Figure 4. System Scaling

4 Summary

Freescale offers a scalable system solutions based on PowerQUICC and DSPs based on StarCore technology. The specific PowerQUICC and DSP that is utilized depends on the target system performance. However, the PowerQUICC II Pro MPC8360E with the new QUICC Engine is a significant step forward in performance, integration, and cost effectiveness for flexible, high performance media gateway designs. The MPC8360E offers a comprehensive feature set that enables cost-effective solutions with an unrivalled level of versatility to evolve as standards and the system requirements change.

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