i.MX31 PDK Hardware
User's Guide

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About This Book

This document explains how to connect and operate the i.MX31 3-Stack Platform System.

Audience

This document is intended for software, hardware, and system engineers who are planning to use the product and for anyone who wants to understand more about the product.

Organization

This document contains the following chapters.

Chapter 1	Introduces the features and functionality of the 3-Stack board.
Chapter 2	Provides configuration and setup information.
Chapter 3	Explains how to assemble the boards.
Chapter 4	Provides block diagrams and memory mapping.
Chapter 5	Provides connector pin assignments and signal descriptions.

Conventions

This document uses the following conventions:

`Courier`	Is used to identify commands, explicit command parameters, code examples, expressions, data types, and directives.
Italic	Is used for emphasis, to identify new terms, and for replaceable command parameters.

All source code examples are in C.

Definitions, Acronyms, and Abbreviations

The following list defines the abbreviations used in this document.

APMS	Atlas Power Management System
ATA	Hard drive interface spec
CD	Compact Disk
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Custom Programmed Logic Devices
CPU	Central Processing Unit
CSI	Camera Sensor Imaging
CSPI	Serial Peripheral Interface
DCE	Data Communications Equipment
DDR	Double Data Rate

DIP	Dual In-line Package
DMA	Direct Memory Access
DTE	Data Terminal Equipment
DUART	Dual Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
FIR	Infra Red
GPIO	General Purpose Input/Output
GPO	General Purpose Output
I2C	Inter-Integrated Circuit
ICE	In-Circuit Emulator
I/O	Input/Output
IrDA	Infrared Data Association
ISA	Instrumentation, System, and Automation Society
JTAG	Joint Test Access Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MB	Megabyte
MCU	Microcontroller Unit
MMC	Multi-media Card
MCP	Multi-chip product
MS	Memory Stick
NVRAM	Non-volatile Random Access Memory
OTG	On the Go
PC	Personal Computer
PCMCIA	Personal Computer Memory Card International Association
PCB	Printed Circuit Board
PHY	Physical interface
POR	Power on Reset
PSRAM	Pseudo Random Access Memory
PWM	Pulse Width Modulation
QVGA	Graphics Adapter
RAM	Random Access Memory
SD	SanDisk (Smart Media)
SDRAM	Synchronous Dynamic Random Access Memory
SI	System International (international system of units and measures)
SIMM	Single In-Line Memory Module
SPST	Single Pole Single Throw
SSI2	Synchronous Serial Interface
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Chapter 1
Introduction

The i.MX31 3-Stack Platform System helps you develop new solutions using the i.MX31 ARM11™ MCU and the MC13783 audio and power management chip.

The 3-Stack platform comprises the CPU Engine board, Personality board, and Debug board. The system supports application software development, target board debugging, and optional circuit cards. The CPU board can be run in stand-alone mode for code development. An LCD display panel is supplied with the 3-Stack system.

Figure 1-1 shows the major components of the 3-Stack system.

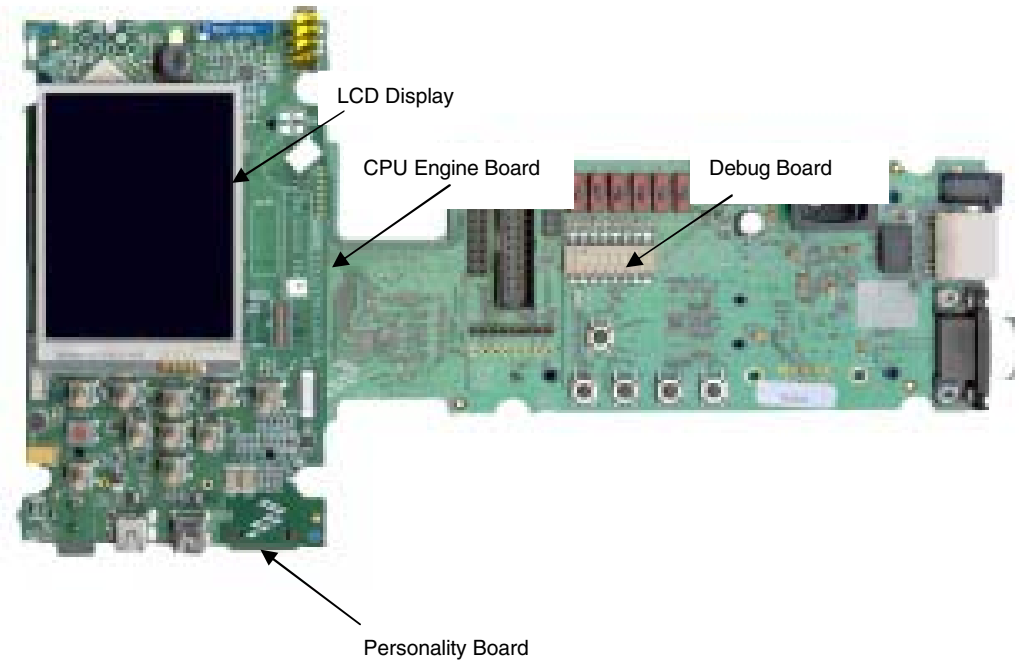

Figure 1-1 Major Components of the 3-Stack System

1.1 Features

The 3-Stack system can be used in two ways: the development mode requires a three-board assembly; the demonstration mode requires only a two-board assembly (without the Debug board).

The system includes the following features.

- Near form-factor demonstration modules and working platforms.
- Solid reference schematics that closely resemble final products to aid customers' designs.
- Three-board system, which includes:
  - CPU board with i.MX31 ARM11 MCU, MC13783 chip
  - Personality board with peripheral components and interface connectors
  - Debug board with two RS-232 interfaces, 10/100 Base-T Ethernet connector, and current measure connectors.
- Utilizes reliable high-density connector to interface between boards.

Figure 1-1 illustrates the three-board assembly (left) for development and the two-board assembly (right) for demonstration.

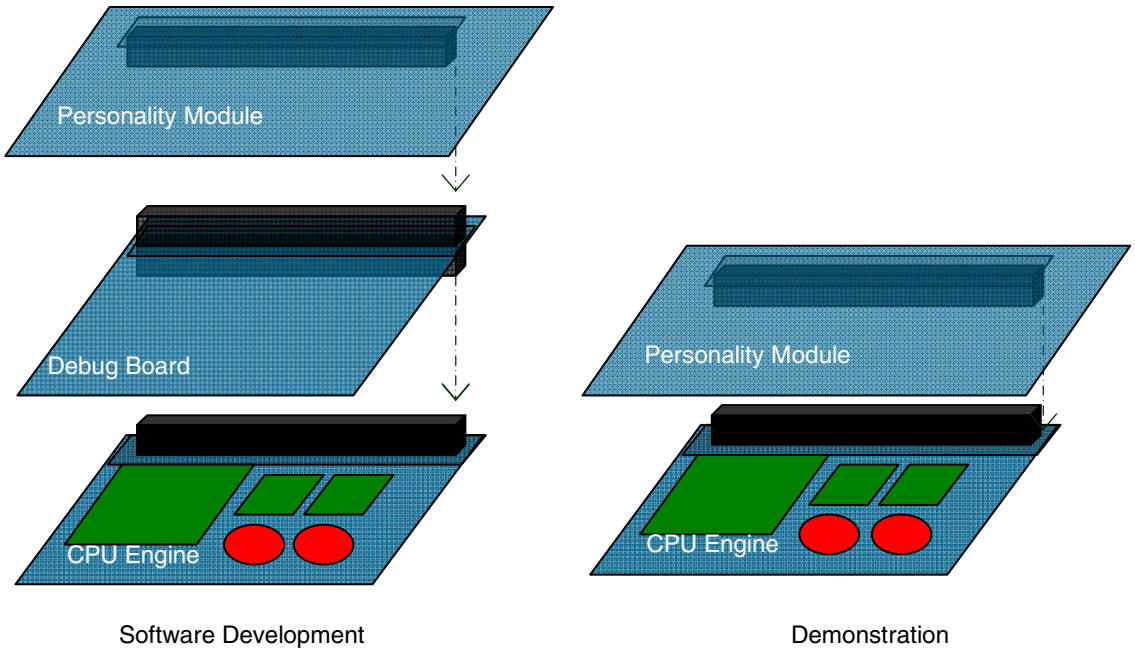

Figure 1-1 Board Assemblies

1.2 Components

The 3-Stack board set includes the following components:

- +5.0 VDC, 2.4 A universal power supply
- +4.2 V 2400mAh battery power supply and battery charging function
- 2.8-inch thin film transistor liquid crystal display (TFTLCD) panel with touch panel and LED backlight
- 2.4-inch Quarter Video Graphics Array (QVGA) smart display panel connector
- Image sensor camera connector
- Configurable intelligent management of system power through power management chip MC13783
- Two selectable system clock sources, 32.768KHz and 26MHz
- 256 MB of NAND Flash Memory
- 128 MB of 32-bit DDR SDRAM memory
- RealView-ICE® debug support`
- Pushbutton reset (on CPU) or reset control from MC13783
- Stereo microphone jack, headphone and video jack, stereo and mono (ear piece) speaker terminals
- One connector to outboard GPS module
- FM receiver
- TV decoder that supports 8-bit color, and NTSC and PAL formats
- SD card connectors, with card sense functionality
- Onboard keypad and keypad connector
- Onboard Wi-Fi CERTIFIED™ IEEE 802.11™ b/g standards and Bluetooth(r) Core Specification Version 2.0 + EDR (enhanced data rate) combination module
- One USB On-the-Go (OTG) high-speed transceiver with mini-USB connector
- One USB high-speed host transceiver, with standard USB host connector
- ATA5-compliant controller with one 44-position dual row, 2mm header for small form-factor disk drivers, and one 40-pin ZIF connector for Toshiba HDD
- Onboard accelerometer with sensitivity in three separate axes (X, Y, and Z)
- Two RS-232 interfaces with DB-9 connectors: one is driven by UART channel internal to the i.MX31 and supports DCE with optional full modem controls; the other is DTE with optional full modem controls

1.3 System and User Requirements

You will need an IBM® PC or compatible computer that includes:

- Windows 98™, ME™, 2000™, XP™, or NT ™ (version 4.0) operating system
- One +5VDC, 2.4A power supply with a female (inside positive) power connector (included)

CAUTION

Never supply more than +5.5 V power to the i.MX31 3-Stack. Doing so can damage board components.

1.3.1 3-Stack System Operating Specifications

Table 1-1 identifies the clock, environmental conditions, and dimensions of the i.MX31 3-Stack system.

Table 1-1 Specifications

Characteristic	Specifications
Clock	Selectable 32.768KHz or 26 MHz
Temperature: Operating Storage	 -10 °C to + 50 °C -40 °C to +85 °C
Relative Humidity	0 to 90% (noncondensing)
Power Requirements	4.5V to 5.5 V DC @1.5A
Dimensions	CPU Engine board: 37.914mm x 67.517 mm Personality board: 71.428mm x 129.462mm Debug board: 71.400mm x 174.900mm

Chapter 2
Configuration and Connections

This section contains configuration information, connection descriptions, and other operational information that may be useful during the development process.

2.1 Debug Board Configuration

The Debug board provides an easy, familiar interface for programming and debugging the i.MX development systems and reference platforms.

This section describes the switches and connectors on the top of the Debug board, and the connector to the CPU Engine board on the bottom of the Debug board. The Debug board is a small card that you can insert or remove from the platform. The ability to remove the debug board is a major advantage to marketing and sales teams who want to demonstrate and showcase a variety of products and ideas in a streamlined, near form factor way, without the added software development bulk.

2.1.1 Debug Board Top Switches and Connectors

Figure 2-1 identifies the switches and connectors located on the top of the Debug board. Table 2-1 describes the switches and connectors.

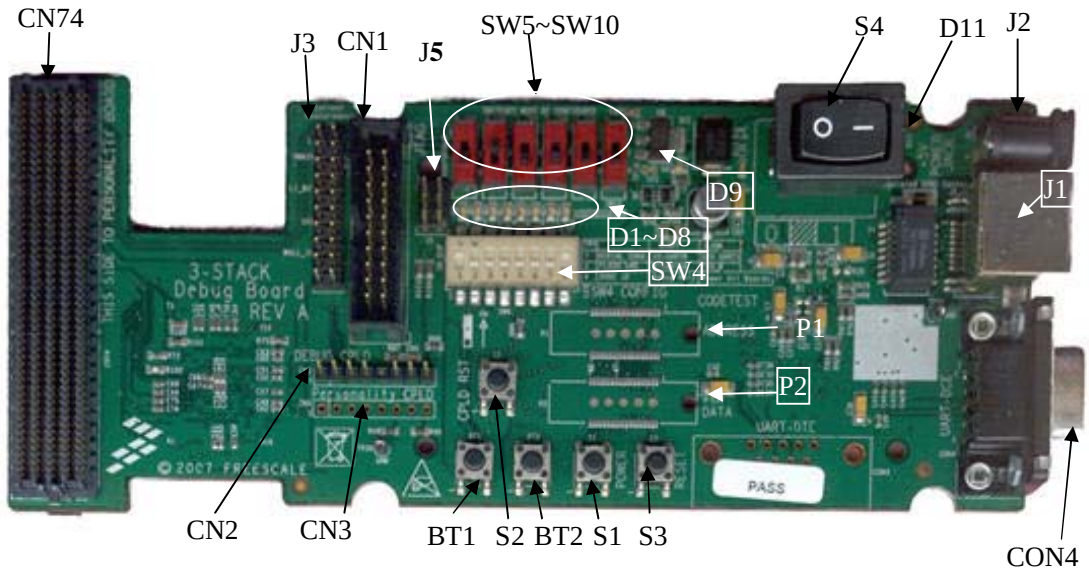

Figure 2-1 Debug Board, Top View

Table 2-1 Debug Board, Top Components

Component Identifier	Description		
S1	Power button, which is connected to the ON1B input of the MC13783 through the 500 pin connector. The line is pulled up, and push it grounds the line. If MC13783 is in Off, User Off or Memory Hold Mode, the board can be powered on via pushing the button		
S2	Reset button, which resets the debug board.		
S3	System reset switch, which is connected to the RESETB to MX31. The line is pulled up, and push it grounds the line.		
S4	Power on switch, which powers up the Debug board when set to 1.		
J1	10/100 Base T Ethernet RJ45 Connector		
J2	5.0V DC power connector		
J3	Current measure connector; measure the current at various points of CPU Engine and Personality board from the connector.		
F1	Re-settable fuse; re-settable over-current protection		
D1 – D8	LEDs for CPLD debug		
D9	LED for debug board 3.3V power; the LED will be bright when debug 3.3V is power on		
D11	LED for DC power supply; the LED will be bright when 5.0V DC power is supplied		
P1	WEIM Address measure connector; it can support CodeTest Interface Probe		
P2	WEIM Data measure connector; It can support CodeTest Interface Probe		
BT1, BT2	Test buttons for CPLD		
CN1	i.MX31 JTAG connector		
CN2	Debug board CPLD JTAG connector		
CN3	Personality board CPLD JTAG connector (Reserved)		
CN74	500 pins connector to Personality board		
CON4	UART (DCE) DB9 female connector		
SW4	Enable switch; the switch designation settings follow.		
	SW4-1 UART Port Select	ON	Serial port UART (DTE) CON3 is selected
		OFF	Serial port UART (DCE) CON4 is selected
	SW4-2 NorFlash Enable	ON	Enable NorFlash on Debug board
		OFF	Disable Norflash on Debug board
	SW4-8 Power Enable	ON	Power supply to three boards
		OFF	Power supply to Debug board only

SW5 – SW10	Boot mode setting switches; SW5 to SW10 settings determine where the processor begins program execution; the valid combinations of the switch settings follow.						
	Boot mode device	SW5	Boot4 SW6	Boot3 SW7	Boot2 SW8	Boot1 SW9	Boot0 SW10
	UART/USB Bootloader	X	0	0	0	0	0
	8-bit NAND Flash (2KB page) Ext	X	1	0	0	0	0

2.1.2 Debug Board Bottom Connectors

Figure 2-2 illustrates the bottom view of the Debug board, where J4 identifies the 500-pin connector to the CPU Engine board.

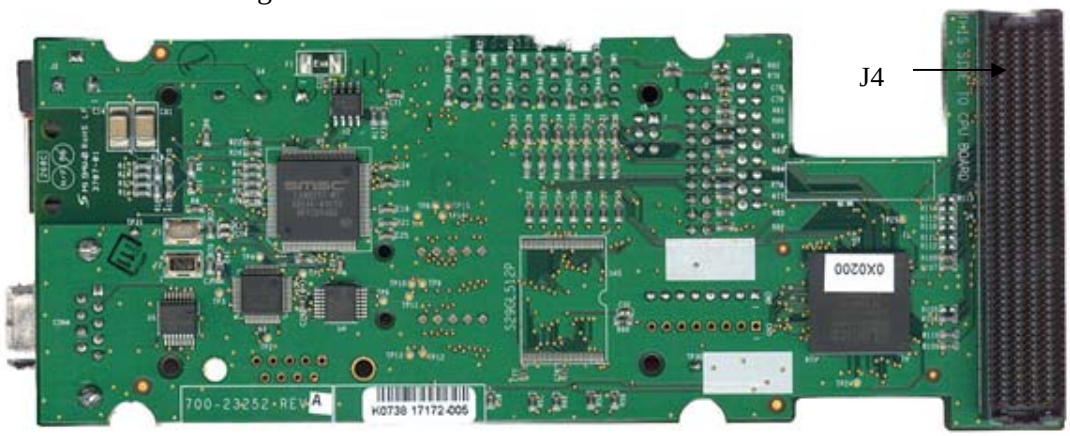

Figure 2-2 Debug Board, Bottom View

2.2 Personality Board Connectors

This section describes the switches and connectors on the top of the Personality board, and the connectors on the bottom of the Personality board.

2.2.1 Personality Board Top Connectors

Figure 2-3 identifies the connectors on the top of the Personality Board.

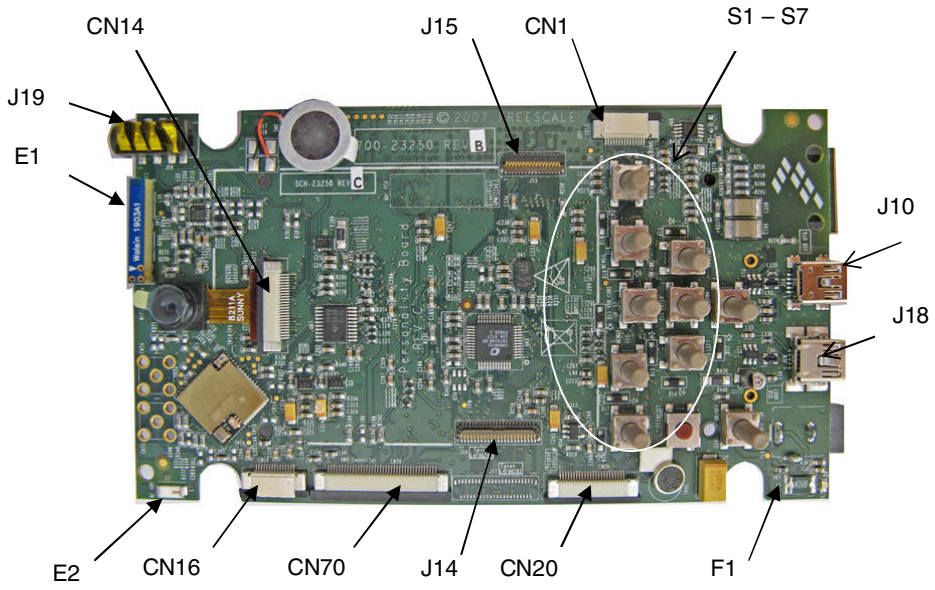

Figure 2-3 Personality Board Connectors, Top View

Table 2-2 Personality Board Connectors, Top View

Component Identifier	Description
E1	Wi-Fi antenna
E2	Bluetooth antenna
F1	Resettable over current-protection fuse
J10	Mini USB OTG High speed connector, for USB OTG connection
J14	Epson VGA LCD connector
J15	Giantplus QVGA Smart display connector
J18	mini USBOTG High speed connector, for USB HOST connection
J19	Audio and Video connector
CN13	GPS module connector
CN14	2.0M pixel CMOS sensor connector
CN16	Debug port for Wi-Fi and Bluetooth module
CN70	40 pin ZIF connector for Toshiba HDD
S7 – S17	Onboard keypad

2.2.2 Personality Board Bottom Connectors

Figure 2-4 illustrates the bottom view of the Personality board. Table 2-3 describes the connectors.

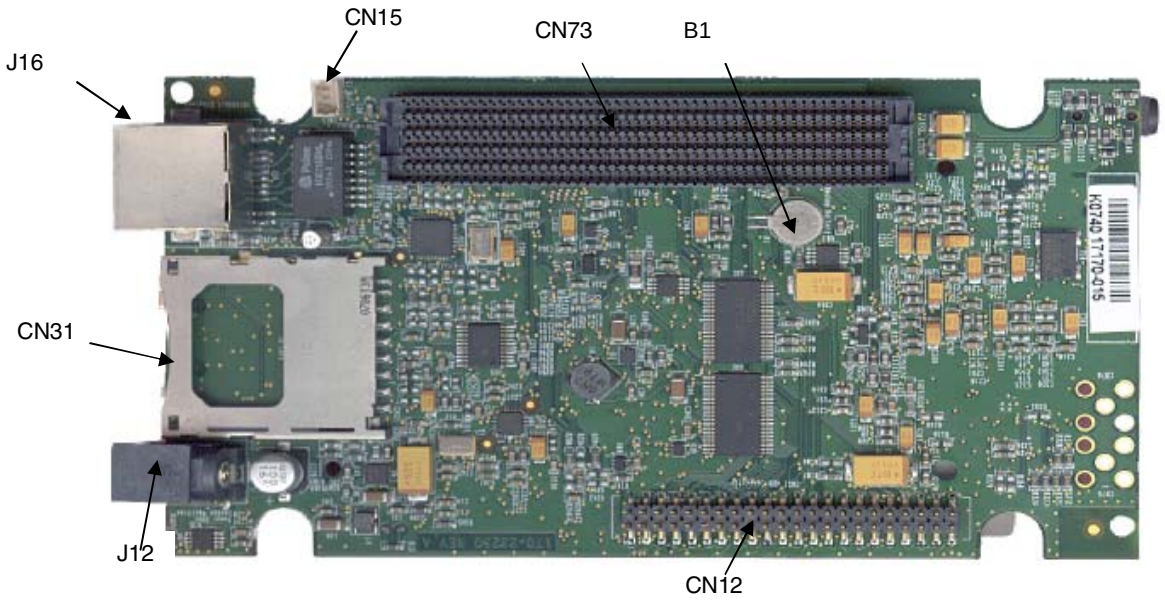

Fig 2-4 Personality Board, Bottom View

Table 2-3 Personality Board Bottom Connectors

Component Identifier	Description
B1	Coin cell battery
J12	5.0 Vdc power connector
J16	10/100BT Fast Ethernet Connector
CN12	44-position dual row, 2mm header for HDD
CN31	SD card socket
CN73	500-pin Connector to CPU Engine board (In Demo Mode) or Debug board (In Debug Mode)
CN15	Battery Connector

2.3 CPU Board Connector

Figure 2-5 illustrates the bottom view of the CPU Engine board, where J1 is the 500-pin connector to the Personality board (for demonstrations) or the Debug board (for software development).

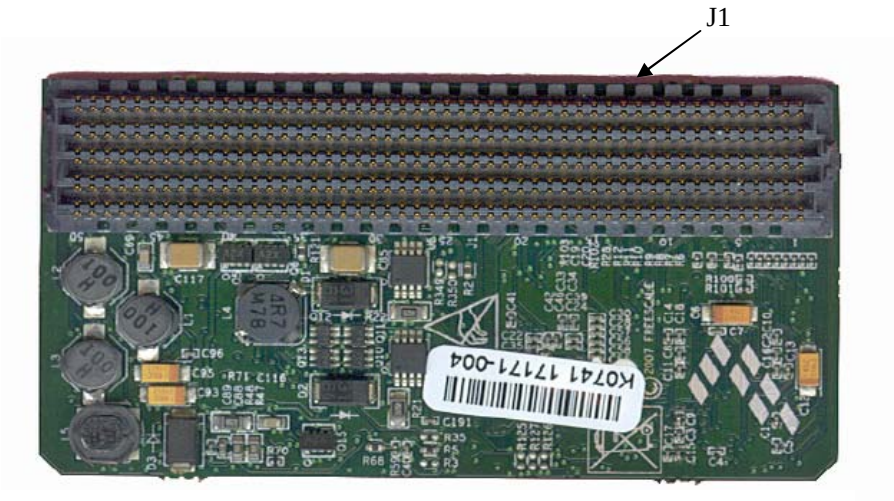

Figure 2-5 CPU Engine Board, Bottom View

2.4 Setting Up the 3-Stack Platform

2.4.1 Debug Board Switches

To set the Debug board switches, use these steps:

1. Set CPU Engine and Personality board power enable switch SW4-8.
2. Set Boot Mode Switches, SW5~SW10.

Chapter 3
Building the Platform

This chapter explains how to connect the three types of 3-Stack boards (Debug, Personality, CPU) together (Figure 3-1), to make either a development platform (Personality board + CPU board + Debug board), or a demonstration platform (Personality board + CPU board); and how to connect the 3-Stack platform to your PC.

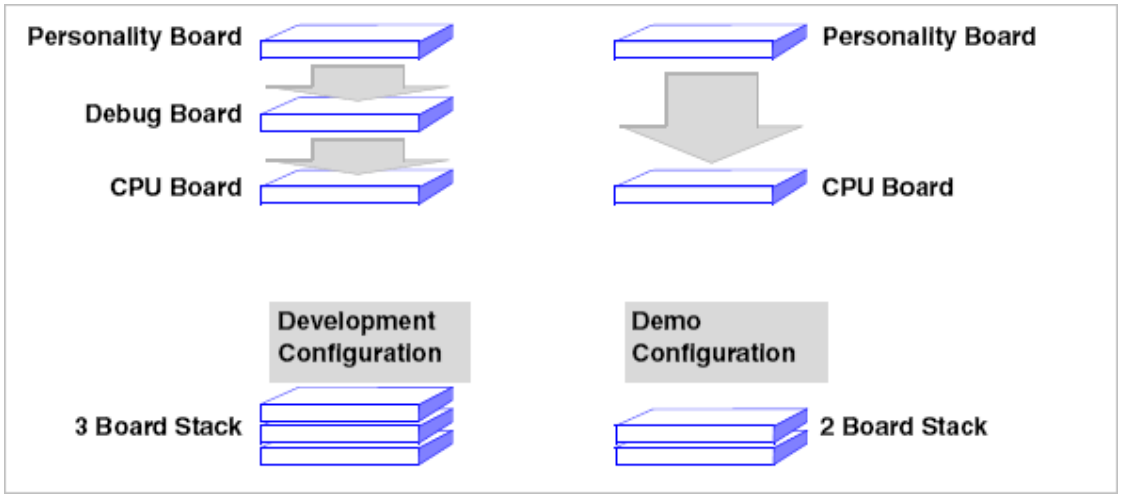

Figure 3-1 Platform Configurations

The three 3-Stack boards in your development kit may already be assembled. If the three boards are already assembled, review the procedures in the following sections, and be sure to configure the Debug board appropriately.

- To build a development platform, follow the procedures in “Building a Development Platform: Assemble 3 Boards” on page 3-2.
- To build a demonstration platform, follow the procedures in “Building a Demo Platform: Assemble 2 Boards” on page 3-6.

3.1 Building a Development Platform: Assemble 3 Boards

This section explains how to connect the Personality, Debug, and CPU boards.

3.1.1 Connect Personality Board to Debug Board

The Personality board connects to the Debug board using a 500-pin connector. The connector is keyed to avoid misconnection, so there is only one way to connect these boards. Connect the Personality board to the Debug board. See Figure 3-2.

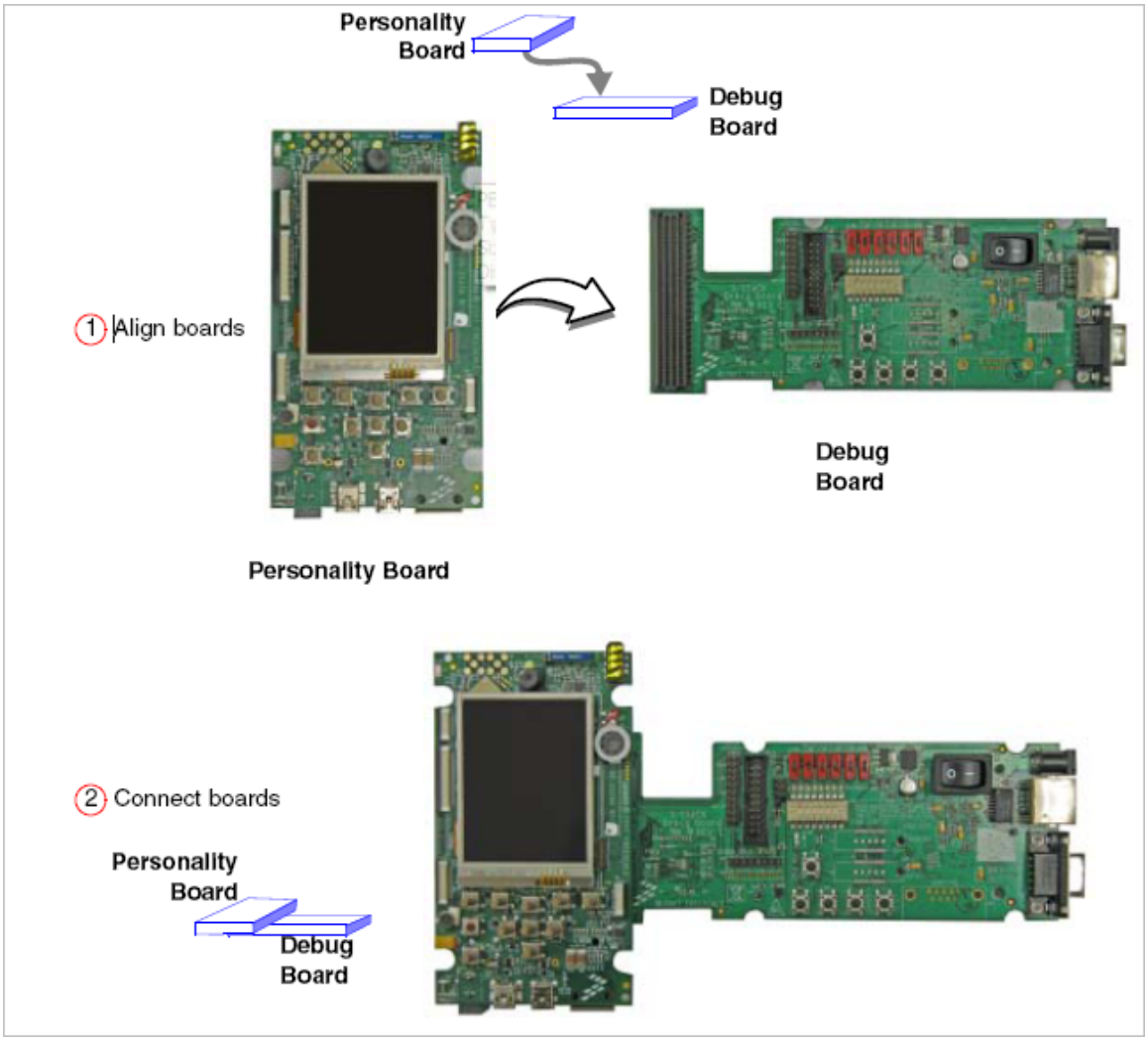

Figure 3-2 Install Personality Board onto Debug Board

3.1.2 Connect CPU Board to Debug Board

After connecting the Personality board to the Debug board, now connect the CPU board to the underside of the Debug board (Figure 3-3).

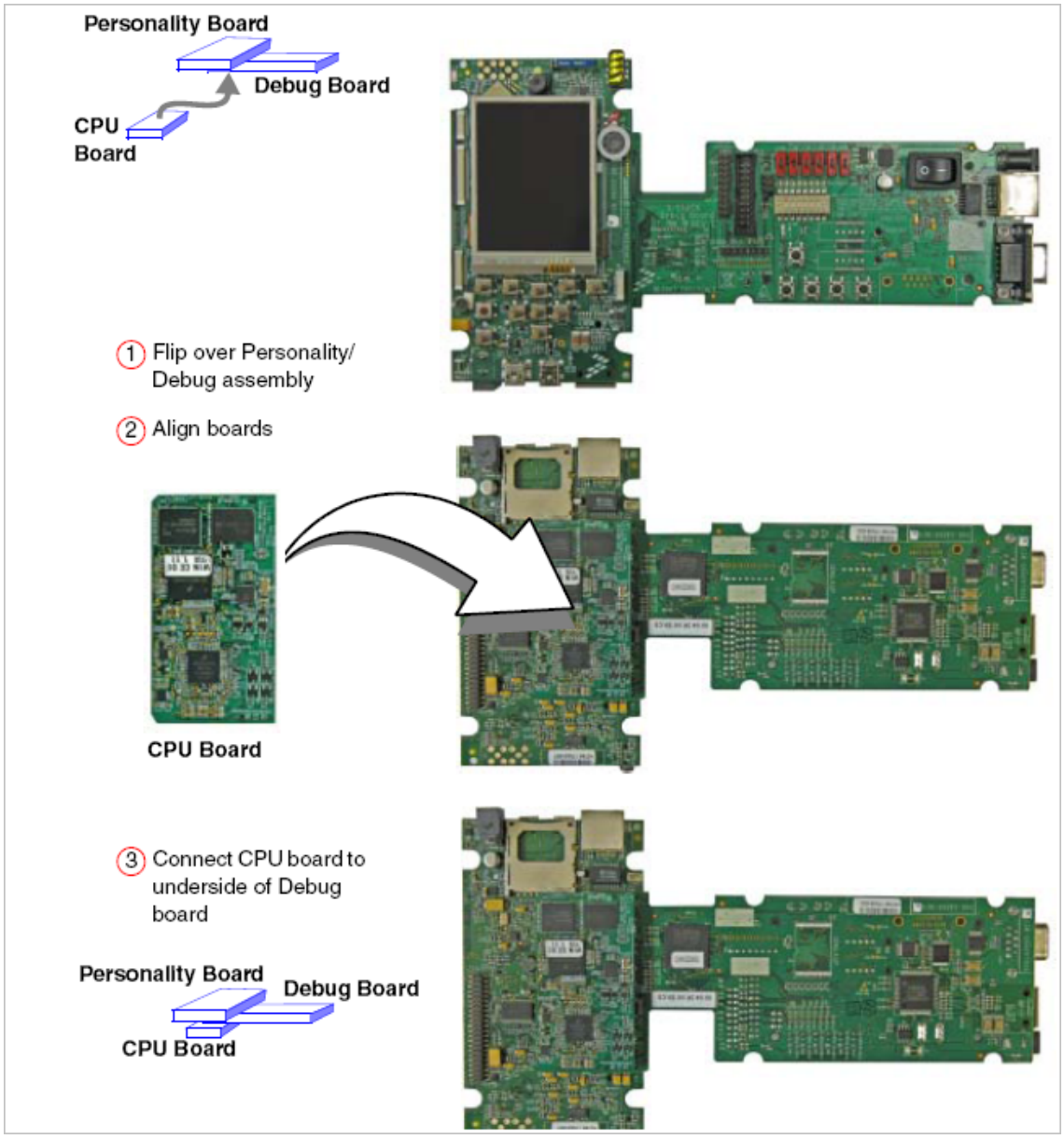

Figure 3-3 Align CPU Board and Debug/Personality Board

3.1.3 Connect Development Platform to PC; Run Preloaded Image

Figure 3-4 illustrates the switches and PC connection.

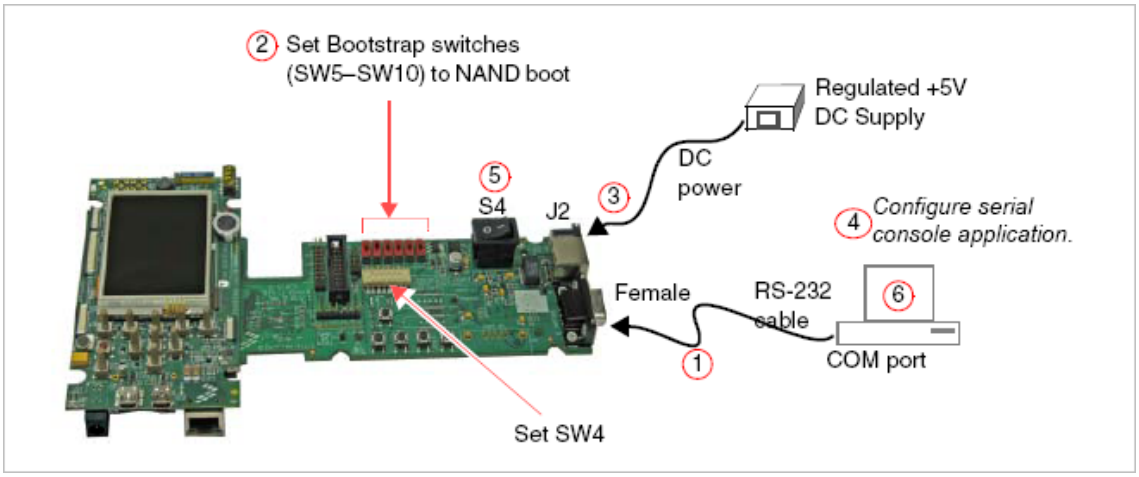

Figure 3-4 Connecting the Platform to Your PC

To connect the 3-Stack platform to your host PC, use these steps:

1. Connect one end of an RS-232 serial cable (included in the kit) to a serial port connector (CON4) on the Debug board and connect the other end to a COM port on the host PC.
   - Configure SW4-1 to ON.
   - Make sure that SW4-8 is ON, to supply power to all three boards.
   - Configure SW4-2 to OFF.
2. Confirm that the Bootstrap switches (SW5–SW10) are set for NAND boot; see the following table.

Boot Mode Device	SW5	SW6 (Boot4)	SW7 (Boot3)	SW8	SW9	SW10
UART/USB Bootloader	X	0	0	0	0	0
8-bit NAND Flash (2KB page) Ext	X	1	0	0	0	0

3. Connect the regulated 5V power supply to the appropriate power adapter. Plug the power adapter into an electrical outlet and the 5V line connector into the J2 (5V POWER JACK) connector on the Debug board. See Figure 3-5.
4. Start a serial console application on your host PC with the following configuration:
   - Baud rate: 115200
   - Data Bits: 8
   - Parity: none
   - Stop Bits: 1
   - Flow Control: none
5. On the Debug board, switch the power switch (S4) to 1.
6. The OS image pre-loaded in the 3-Stack board will boot and the debug messages from the bootloader should now appear on the serial console application on your PC.

3.2 Building a Demo Platform: Assemble 2 Boards

This section explains how to make a demonstration platform using the Personality and CPU boards. To make a demonstration platform, the CPU board is directly connected to the Personality board using the 500-pin connector; the Debug board is not used (Figure 3-5).

NOTE

If your system is already configured as a development platform (using all three boards), disconnect all boards from each other.

3.2.1 Connect CPU Board to Personality Board

Connect the CPU board to the Personality board. The connector is keyed to avoid misconnections, so that there is only one way to connect the CPU board to the Personality board.

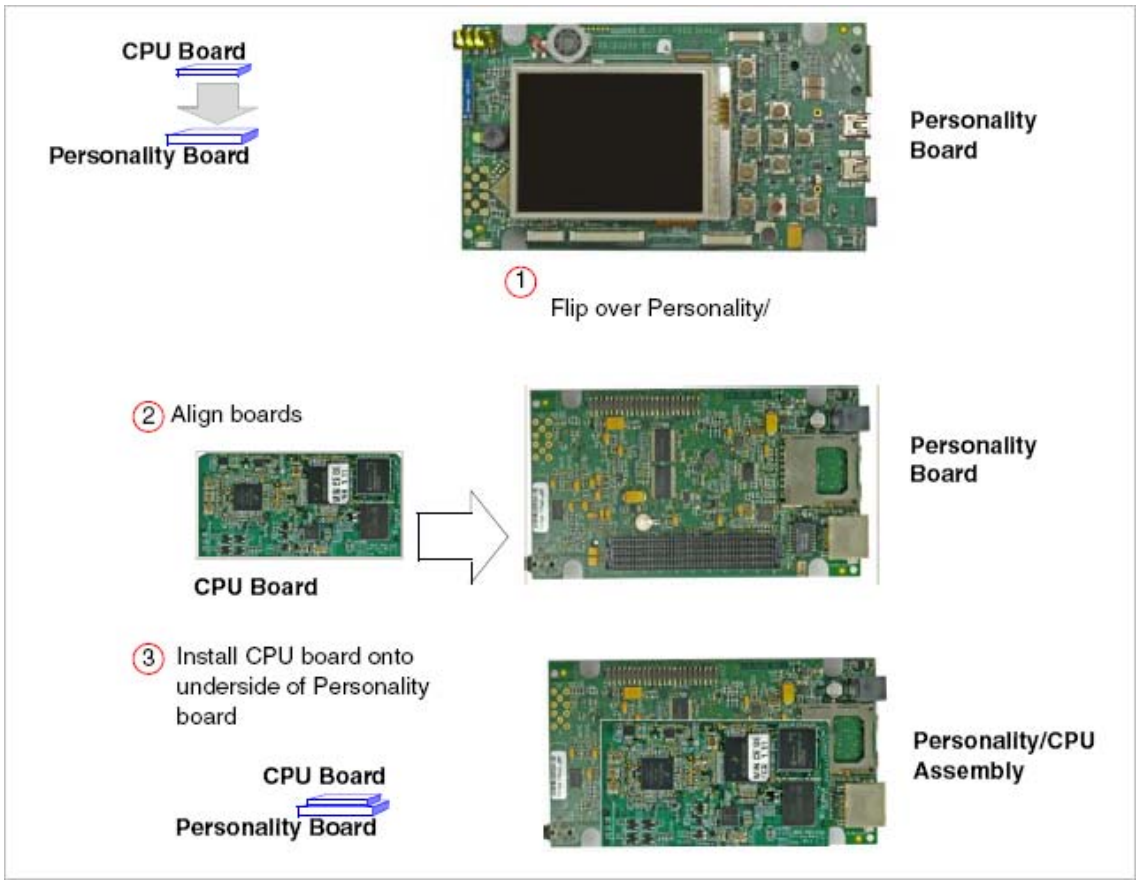

Figure 3-5 Install CPU Board onto Personality Board

3.2.2 Connect Power Supply; Run Pre-loaded Demo

The system has two DC power jacks: one on the Debug board and one on the Personality board (Figure 3-6).

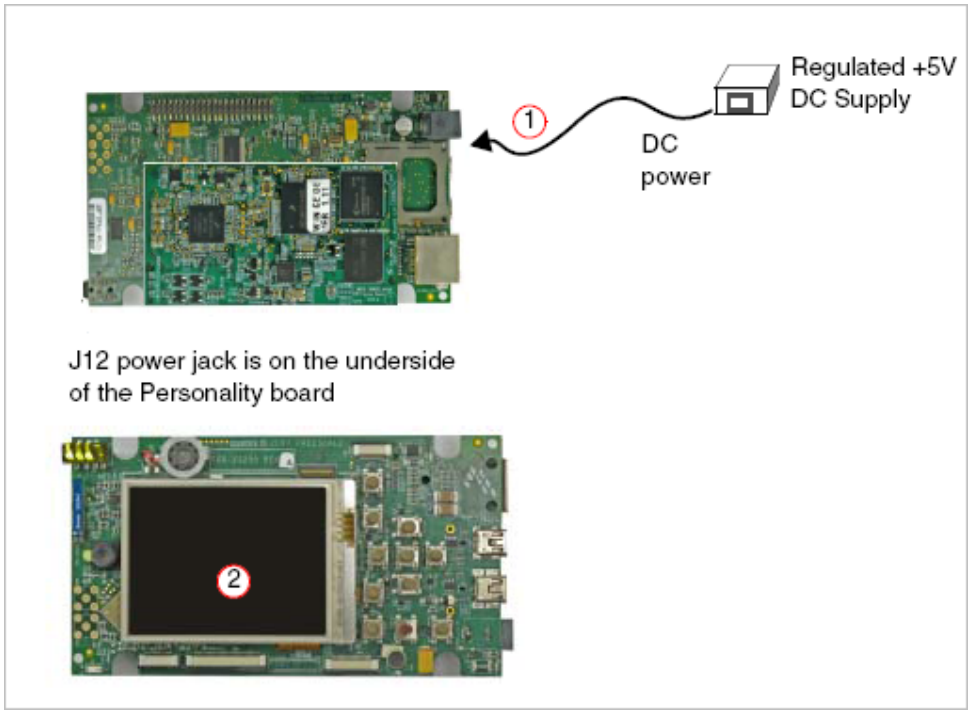

Figure 3-6 Connect Personality Board to Power Supply

Connect the regulated 5V power supply to the appropriate power adapter. Plug the 5V line into the J12 (5V POWER JACK) connector on the Personality board. Turn the 5V power supply ON. The OS image pre-loaded in the 3-Stack should boot and the operating system should appear at the Personality board's LCD display.

Software development mode:

- Assemble the three boards together.
- Plug the 5.0 volts DC power into the Debug board DC power jack.
- Press S4 on the Debug board to "1" to power on the 3-Stack system.

Demonstration mode:

- Assemble the Personality and CPU Engine boards together (without the Debug board).
- Plug the 5.0V DC power into the Personality board DC power jack, and the 3-Stack system will be powered on directly.

Chapter 4
Functional Operation

4.1 Functional Block Diagram

Figure 4-1, Figure 4-2, and Figure 4-3 illustrates the functional blocks of the 3-Stack board.

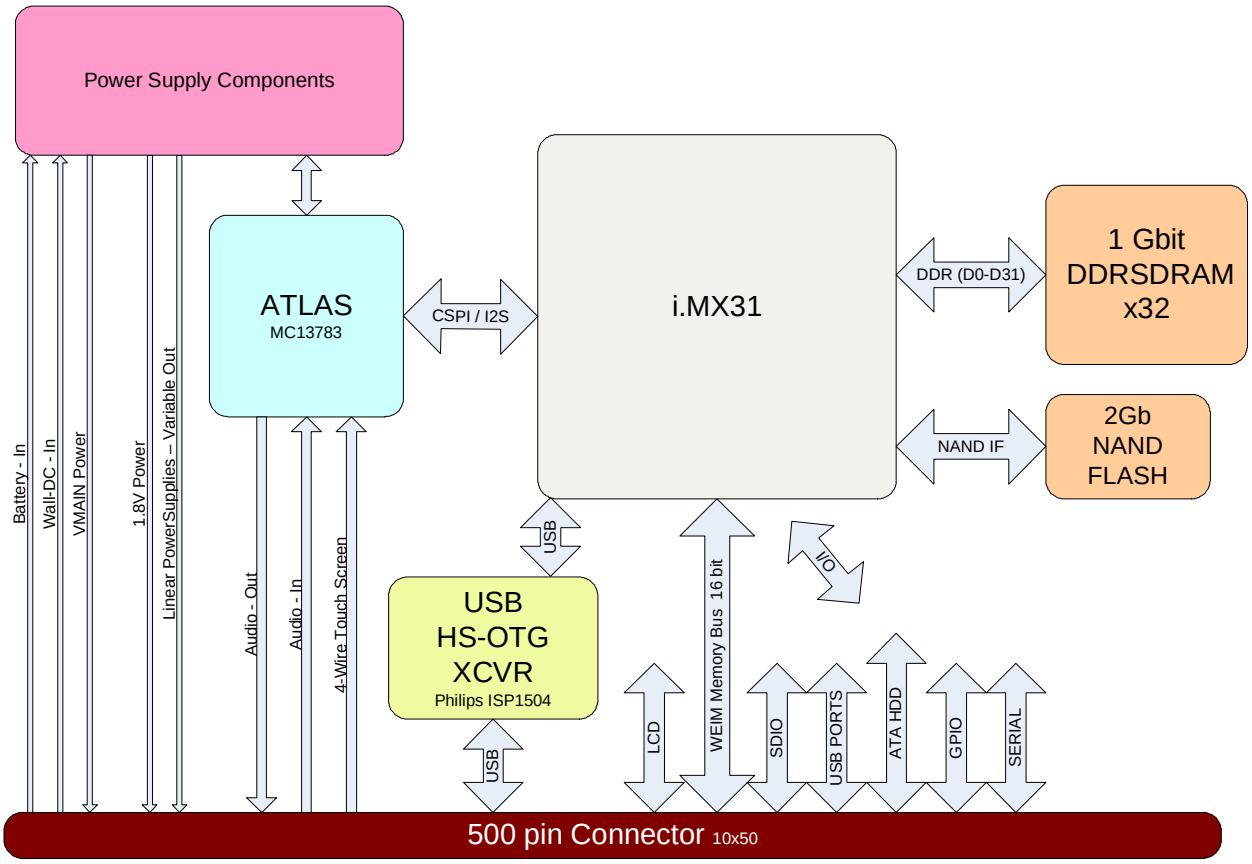

Figure 4-1 Functional Block 1 of 3

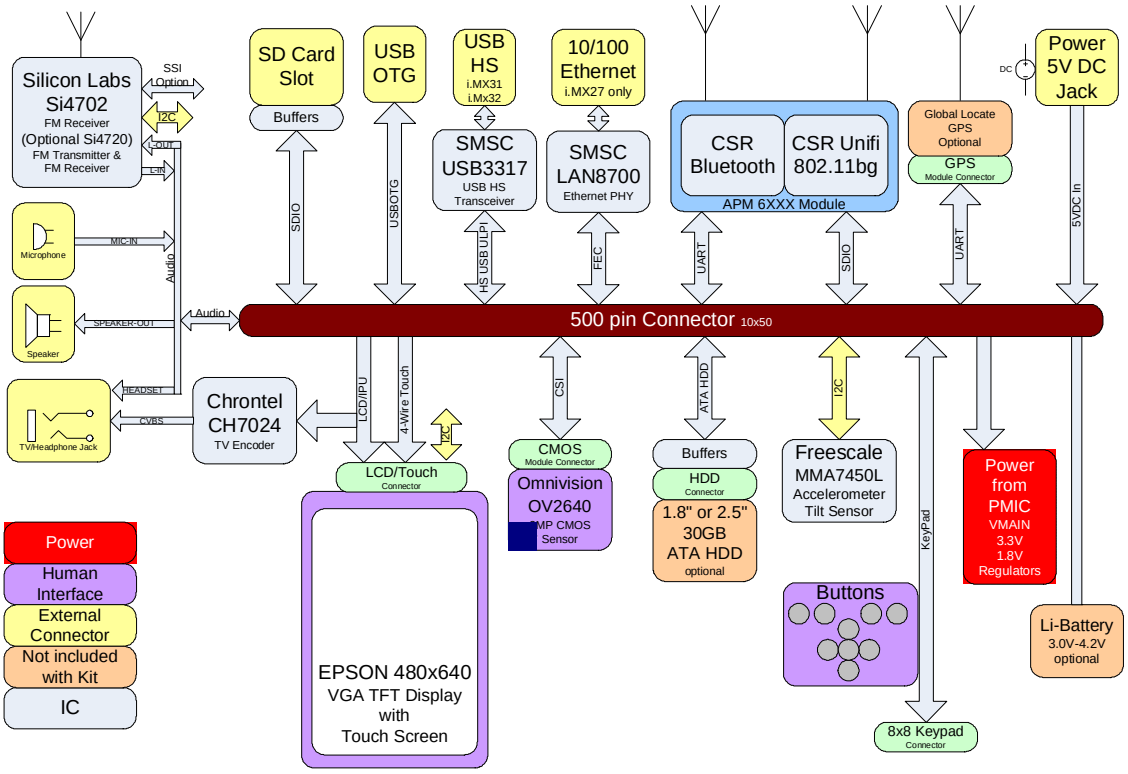

Figure 4-2 Functional Block 2 of 3

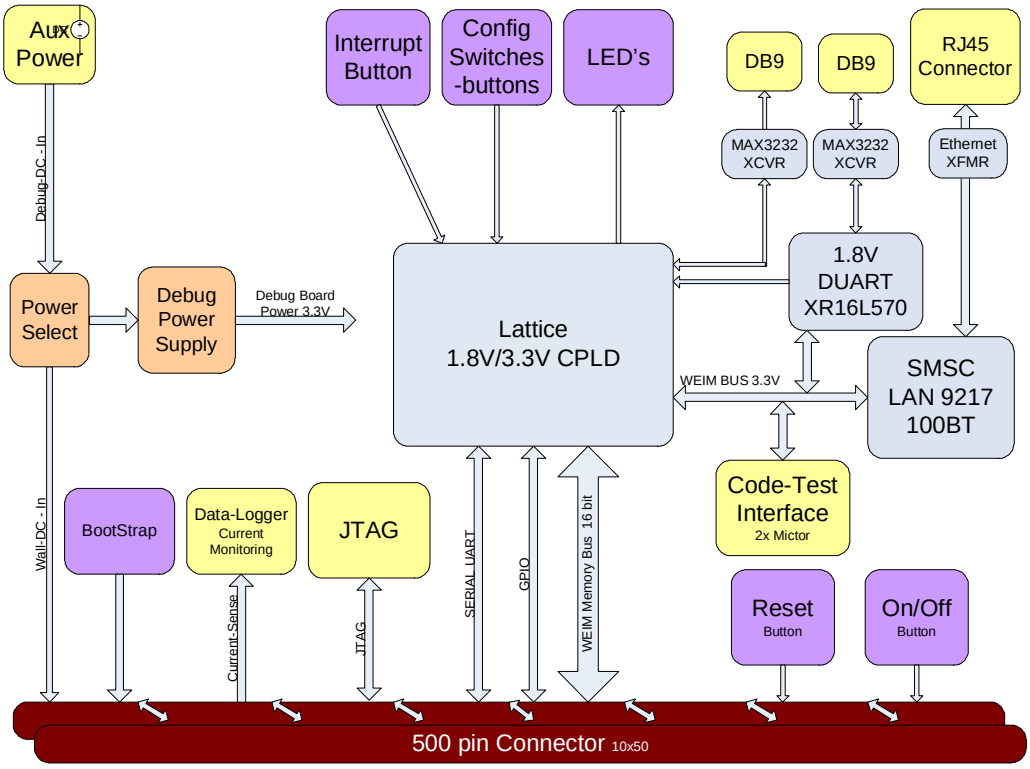

Figure 4-3 Functional Block 3 of 3

4.2 3-Stack Memory Map

Table 4-1 describes the memory map for the 3-Stack system. None of the memories take up the entire address space of the associated chip selects, and the software can access the same physical memory location at more than one range of address. For instance, DDR SDRAM occupies only 128 MB of the 256MB space available to CSD0, so it appears in two different ranges of addresses.

Table 4-1 Memory Map

Peripheral	Chip Select	Address Range (HEX)	Size
DDR	$\overline{\text{CSD0(CS2)}}$	0x8000_0000 to 8FFF_FFFF	128MB
Ethernet Controller LAN9217	$\overline{\text{CS5}}$	0xB600_0000 to B600_007F	128MB

Peripheral	Chip Select	Address Range (HEX)	Size
External UART-A DB9-Male	$\overline{\text{CSD0(CS2)}}$	0xB600_8000_ B600_8007	8 Bytes

4.3 CPLD on the Debug Board

A complex programmable logic device (CPLD) is an electronic component used to build reconfigurable digital circuits. The CPLD provides a great deal of functionality, including glue logic, which is needed to achieve compatible interfaces between two (or more) different off-the-shelf integrated circuits. For the 3-Stack board, glue logic provides peripheral bus address decoding, board control and status signals, board revision registers, and other functions, and is implemented with a CPLD on the Debug board.

4.3.1 CPLD Features

The CPLD provides the following key features:

- A 16-bit slave interface to the CPU data bus
- Address decode and control for the Ethernet controller
- Address decode and control for the external UART controller
- Level shift for Ethernet signals and UART signals
- Control and status registers for various board functions

4.3.2 CPLD Memory Map

Table 4-2 CPLD Memory Map

CS5_B	A16	A15	A14	A5	A4	A3	A2	Description
0	0	0	0	x	x	x	x	SMSC LAN9217 Ethernet 10/100BT
0	0	0	1	x	x	x	x	External UART-A
0	0	1	0	x	x	x	x	External UART-B
0	0	1	1	x	x	x	x	Reserved
0	1	0	0	0	0	0	0	Read/Write LED's (1=on, 0=off)
0	1	0	0	0	0	0	1	Read Only Switches/Buttons
0	1	0	0	0	0	1	0	Read Only Status - Interrupts, Interrupt latch
0	1	0	0	0	0	1	1	Read/Write - Interrupt Mask
0	1	0	0	0	1	0	0	Write - Interrupt reset
0	1	0	0	0	1	0	1	R/W Software Override: Set UART-B/CPU UART routing
0	1	0	0	0	1	1	0	R/W Software Override: Enable/Disable Flash Access, select CSx
0	1	0	0	0	1	1	1	Software Override 3 reserved
0	1	0	0	1	0	0	0	Read Only Returns AAAA

0	1	0	0	1	0	0	1	Read Only Returns 5555
0	1	0	0	1	0	1	0	Read Only CPLD Code Version #
0	1	0	0	1	0	1	1	Read Only Returns CAFÉ
0	1	0	0	1	1	0	0	Reserved

4.3.3 Programming the CPLD

To program the CPLD, use these steps:

1. Install Lattice ispLEVER Project Navigator Ver 6.0 on the PC.
2. From the **Start** menu, select **Programs** > **Lattice Semiconductor** > **Accessories** > **ispVM System**.
3. Connect the **Lattice CPLD ispDOWNLOAD Cable** to the PC parallel port.
4. Attach the **JTAG** connector to **CN2** on the Debug board.
5. Power on the Debug board.
6. Scan **Chain**.

   The CPLD device list is displayed (Figure 4-4).

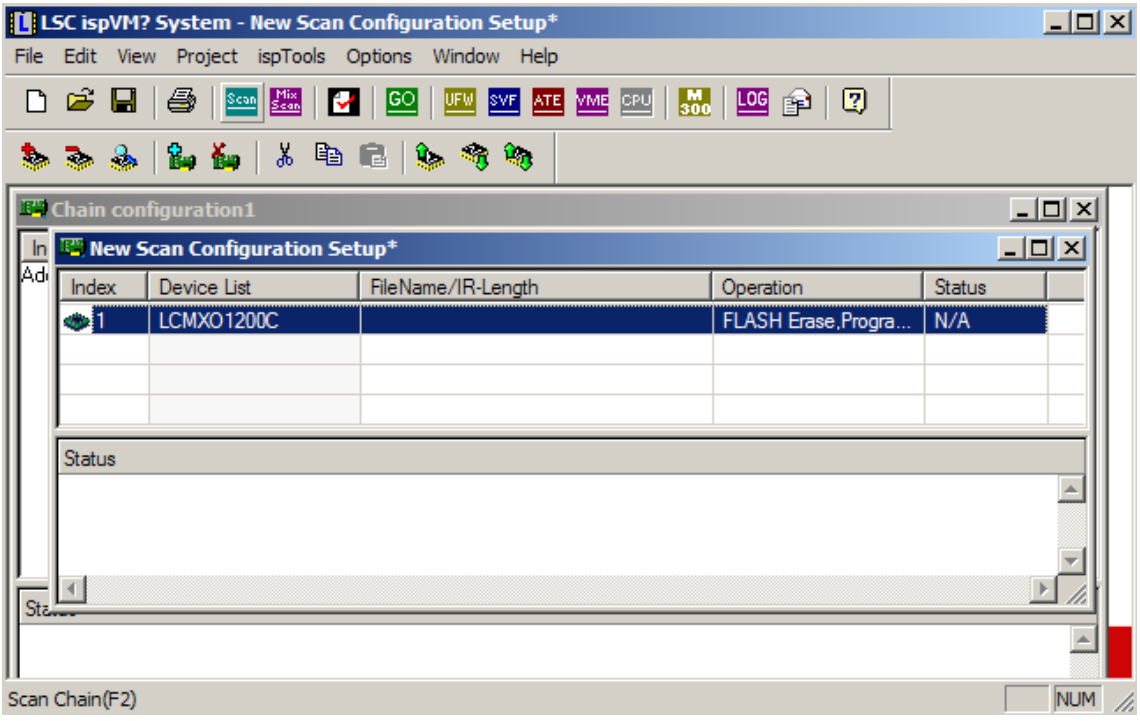

Figure 4-4 Scan CPLD Devices

7. Double-click **LCMXO1200C**.

8. Select the CPLD data file (Figure 4-5).

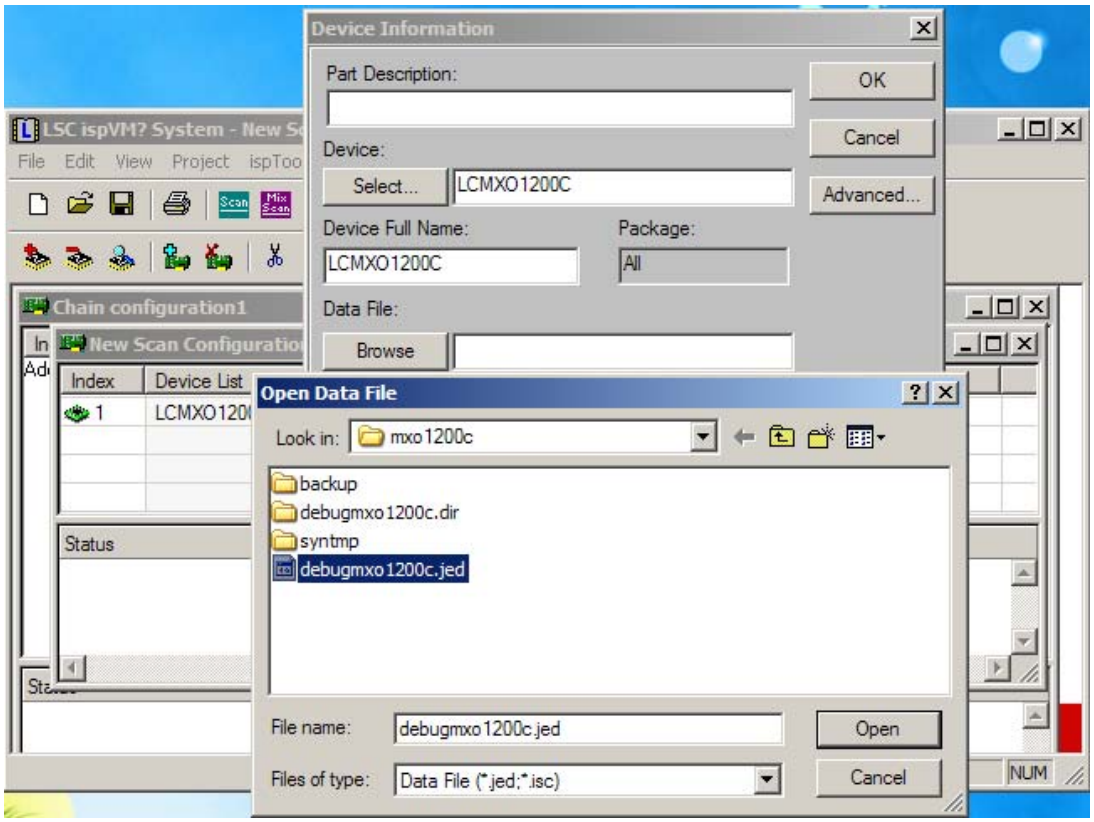

Figure 4-5 Selecting the CPLD Data File

9. Click GO to download the data file in the CPLD.
10. Wait about 10 seconds.

    When the Status section displays **PASS**, programming the CPLD is completed.

4.4 i.MX31 GPIO Grouping

Table 4-3 describes the GPIO pins.

Table 4-3 BPIO Grouping Descriptions

Pin Name	Description	Note
GPIO1_0	To MC13783 User off signal	
GPIO1_1	Debug board Interrupt	Active low
GPIO1_2	ON_OFF button	Active low
GPIO1_3	MC13783 PRI SPI interrupt	
GPIO1_4	MC13783 Low battery indicator signal or end of life indicator signal	
GPIO1_5	MC13783 Power ready signal	
GPIO1_6	MC13783 Regulator Enable	
GPIO3_0	SD card buffer Enable	Active High
GPIO3_1	SD card Detection	Active Low
USB_PWR	USB OTG Reset	Active Low
USB_BYP	GPS and USB Host Reset	Active Low
USB_OC	USB Host Over current signal	
DTR_DCE1	DC Power plug detect	Active High
DCD_DCE1	Wi-Fi and Bluetooth reset	Active Low
BATT_LINE	Headphone plug detect	Active Low
SCLK0	GPS module power enable	Active High
SIMPD0	FM clock enable	Active High
SRST0	CMOS and FM reset	Active Low
SRX0	Accelerometer Interrupt1	Active Low
STX0	Accelerometer Interrupt2	Active Low
SVEN0	GPS interrupt	Active Low
CSI_D5	Camera sensor power down	Active high
SD_D_I	TV-Out chip data enable	Active high
LCS1	TV-Out and LCD reset	Active low
SER_RS	LCD Data Enable signal	Active low

Chapter 5
Connectors and Signals

This chapter provides connector pin assignments and signals for i.MX31 3-Stack CPU, Personality, and Debug boards.

- The tables in this section list signal names as they appear in the board schematics.
- The use of "_B" at the end of a name indicates an active low signal.

5.1 500 Pins Board to Board Connector

Table 5-1 500 Pins Connector Pin-Out

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row J	Row K
1	GND	USB_5V_VBUS	GND	CURRENT_MEAS_1	AUDIO_LIN_R	AUDIO_LIN_L	AUDIO_LOUT_R	AUDIO_LOUT_L	TOUCH_X0	TOUCH_Y0
2	LI_BATTERY	USB_5V_VBUS	VMAIN	CURRENT_MEAS_2	RFU	GND	HEADPHONE_RIGHT	HEADPHONE_LEFT	TOUCH_X1	TOUCH_Y1
3	LI_BATTERY	GND	VMAIN	GND	MIC_IN_P	RFU	HEADPHONE_RETURN	GND	GND	GND
4	GND	3V3	GND	CURRENT_MEAS_3	MIC_BIAS	BOOTSTRAP_0	SPEAKER_RIGHT_P	SPEAKER_LEFT_P	TV_DAC_C_RETURN	TV_DAC_C
5	1V8	3V3	LINEAR_A	CURRENT_MEAS_4	HEADPHONE_DETECT	BOOTSTRAP_1	SPEAKER_RIGHT_N	SPEAKER_LEFT_N	TV_DAC_B_RETURN	TV_DAC_B
6	1V8	GND	LINEAR_B	GND	ADC_1	BOOTSTRAP_2	GND	GND	TV_DAC_A_RETURN	TV_DAC_A
7	GND	WALL_5V_IN	LINEAR_C	CURRENT_MEAS_5	ADC_2	BOOTSTRAP_3	SPDIF1	SPDIF2	SIM_CLK	SIM_RX
8	LCD_BKLT_18MA_RETURN	WALL_5V_IN	GND	CURRENT_MEAS_6	GND	BOOTSTRAP_4	RFU	RFU	SIM_RST	SIM_PD
9	LCD_BKLT_18MA_BOOST	GND	LINEAR_D	GND	ADC_3	BOOTSTRAP_5	RFU	RFU	SIM_VEN	SIM_TX
10	BKLT_5V_60MA_A	2V775	LINEAR_E	CURRENT_MEAS_7	ADC_4	VDD_BOOTSTRAP	RFU	VDD_CSI_IO	VDD_SIM_IO	JTAG_TRST_B
11	BKLT_5V_60MA_K	2V775	LINEAR_F	CURRENT_MEAS_8	ADC_5	RFU	RFU	GND	CHRG_LED	JTAG_TDI
12	DEBUG_INT_B	RFU	SLEEP_VSTBY	CURRENT_MEAS_9	ADC_6	RFU	CSI_RESET_B	CSI_HSYNC	VDD_JTAG	JTAG_TMS
13	MASTER_RESET_B	RFU	GND	CURRENT_MEAS_10	GND	RFU	CSI_PWDN	CSI_VSYNC	RFU	JTAG_TCK
14	OSC_32KHz	BATTERY_TEMP	ON_OFF	PWR_EN	RFU	GND	KP_ROW_7	CSI_MCLK	CPLD_PGM_TDI	GND
15	GND	OSC_26MHz	LI_CELL	WI-FI_PWEN	USB-HS-D0	USB-HS-D4	KP_ROW_6	GND	CPLD_PGM_TDO	JTAG_RTCK
16	UART3_RX	RFU	VDD_I2C_IO	VDD_USB_IO	USB-HS-D1	USB-HS-D5	KP_ROW_5	CSI_PIXCLK	CPLD_PGM_TMS	JTAG_DE_B
17	UART3_TX	RFU	I2C1_DATA	USB-HS_OC	USB-HS-D2	USB-HS-D6	KP_ROW_4	CSI_D0	CPLD_PGM_TCK	JTAG_TDO

18	UART3_CTS	RFU	I2C1_CLOCK	USB-HS_RESET_B	USB-HS-D3	USB-HS-D7	KP_ROW_3	CSI_D1	SSI1_STXD	JTAG_RESET_B
19	UART3_RTS	RFU	GND	HDD_PWR_EN	USB-HS_STP	USB-HS_NXT	KP_ROW_2	GND	SSI1_SRXD	MLB_SIG
20	UART2_RX	GND	I2C2_CLOCK	HDD_DMARQ	USB-HS-CLK	USB-HS_DIR	KP_ROW_1	CSI_D2	SSI1_SFS	MLB_DAT
21	UART2_TX	RFU	I2C2_DATA	HDD_DIOW	GND	RFU	KP_ROW_0	CSI_D3	GND	MLB_CLK
22	UART2_CTS	RFU	CSPI1_MOSI	HDD_DIOR	HDD_D0	FEC_TXD2	KP_COL_7	CSI_D4	SSI1_SCK	RFU
23	UART2_RTS	DEBUG	GND	HDD_IORDY	HDD_D1	FEC_TXD3	KP_COL_6	GND	SSI2_STXD	CAN TX1 RFU
24	UART1_RX	PERSONALITY1	CSPI1_MISO	HDD_DMACK	HDD_D2	FEC_RX_ER	KP_COL_5	CSI_D5	SSI2_SRXD	CAN RX1 RFU
25	UART1_TX	PERSONALITY2	CSPI1_SS0	HDD_INTRQ	GND	FEC_TXD0	KP_COL_4	CSI_D6	GND	CAN TX2 RFU
26	UART1_CTS	PERSONALITY3	CSPI1_SS1	HDD_DA1	HDD_D3	FEC_RXD1	KP_COL_3	CSI_D7	SSI2_SFS	CAN RX2 RFU
27	UART1_RTS	CPU1	GND	HDD_DA0	HDD_D4	FEC_RXD2	KP_COL_2	GND	SSI2_SCK	VDD_MLB
28	RFU	CPU2	CSPI1_SCLK	HDD_CS0	HDD_D5	FEC_RXD3	KP_COL_1	CSI_D8	SD1_D0	SD1_CMD
29	VDD_LCDIO	CPU3	CSPI1_RDY	HDD_DA2	GND	FEC_TXD1	KP_COL_0	CSI_D9(MSB)	SD1_D1	SD1_DET
30	LCD_SD_I	LCD_SD_DIO	LCD_DRDY0	HDD_CS1	HDD_D6	FEC_MDIO	GPS_INT	GPS_PWREN	SD1_D2	SD1_WP
31	LCD_HSYNC	LCD_LSCLK_PLCK_FPSHIFT	GND	HDD_RESET_B	HDD_D7	FEC_MDC	ACC_INT1	GND	SD1_D3	SD1_CLK
32	LCD_VSYNC	LCD_RD	LCD_SER_RS_DEN	ATA_ENABLE_B	HDD_D8	FEC_CRS	ACC_INT2	GPS_RST	VDD_SD2_IO	VDD_SD1_IO
33	LCD_LCS1_RST	LCD_WR	LCD_SD_CLK	ATA_DIR	GND	FEC_INT_B	FM_RST	WI-FI_RST	SD2_D0	SD2_CMD
34	LCD_G-1	LCD_G-2	LCD_LCS0	RFU_LCD2	HDD_D9	FEC_TX_CLK	FM_CLK_EN	BT_RST	SD2_D1	SD2_DET
35	LCD_R-1	LCD_R-2	LCD_VSYNC0	RFU_LCD2	HDD_D10	FEC_RXD0	OSC_CLKO	GND	SD2_D2	SD2_WP
36	LCD_B-1	LCD_B-2	LCD_PAR_RS	RFU_LCD2	HDD_D11	FEC_RX_DV	D14	D15	SD2_D3	SD2_CLK
37	LCD_B0_D0	LCD_CONTRAST	GND	RFU_LCD2	GND	FEC_RESET_B	D12	D13	VDD_EIM_ADDR	GND
38	LCD_B1_D1	LCD_CLS	RFU_LCD2	RFU_LCD2	HDD_D12	FEC_RX_CLK	D10	D11	A24	A25
39	LCD_B2_D2	LCD_SPL_SPR	RFU_LCD2	RFU_LCD2	HDD_D13	FEC_COL	D8	D9	A22	A23
40	GND	LCD_REV	RFU_LCD2	RFU_LCD2	HDD_D14	FEC_TX_ER	VDD_EIM_DATA	GND	A20	A21
41	LCD__R5_D	GND	RFU_LCD2	RFU_LCD2	GND	FEC_ENABL	D6	D7	A18	A19

	17					E				
42	LCD_R3_D15	LCD_R4_D16	RFU_LCD2	RFU_LCD2	HDD_D15	FEC_TX_EN	D4	D5	A16	A17
43	LCD__R2_D14	RFU_LCD2/ GND	RFU_LCD2	RFU_LCD2	VDD_HDD_IO	VDD_FEC_IO	D2	D3	A14	A15
44	LCD_R0_D12	LCD_R1_D13	**GND**	RFU_LCD2	RFU_LCD2	RFU_LCD2	D0	D1	A12	A13
45	LCD__G5_D11	RFU_LCD2/ GND	RFU_LCD2	RFU_LCD2	**GND**	RFU_LCD2	ECB_WAIT	BCLK	A10	A11
46	LCD_G3_D9	LCD__G4_D10	**GND**	RFU_LCD2	RFU_LCD2	EB0	EB1	**GND**	A8	A9
47	LCD_G2_D8	RFU_LCD2/ GND	RFU_LCD2	RFU_LCD2	**GND**	1_WIRE_DATA	OE_B	RW_B	A6	A7
48	LCD_G0_D6	LCD_G1_D7	**GND**	RFU_LCD2	RFU_LCD2	LBA	CS4_B	CS5_B	A4	A5
49	LCD__B5_D5	RFU_LCD2/ GND	RFU_LCD2	**GND**	**GND**	USB_OTG_UID	CS2_B	CS3_B	A2	A3
50	LCD_B3_D3	LCD_B4_D4	**GND**	USB_OTG_D_MINUS	USB_OTG_D_PLUS	**GND**	CS0_B	CS1_B	A0	A1

Table 5-2 500 Pin Connector Signal Descriptions

Signal	Pin	Description
GND	A1, A4, A7, A15, A40, B3, B6, B9, B20, B41, C1, C4, C8, C13, C19, C23, C27, C31, C37, C44, C46, C48, C50, D3, D6, D9, D49, E8, E13, E21, E25, E29, E33, E37, E41, E45, E47, E49, F2, F14, F50, G6, H3, H6, H11, H15, H19, H23, H27, H31, H35, H40, H46, J3, J21, J25, K3, K14, K37	Signal Ground
LI_BATTERY	A2, A3	Li_battery interface
1V8	A5, A6	From MC13783 SW2B, for peripheral devices use
LCD_BKLT_18MA_RETURN	A8	LCD backlight power return
LCD_BKLT_18MA_BOOST	A9	LCD backlight power
BKLT_5V_60MA_A	A10	5V, 60mA backlight drive Anode
BKLT_5V_60MA_K	A11	5V, 60mA backlight drive Negative
DEBUG_INT_B	A12	Debug board interrupt
MASTER_RESET_B	A13	i.MX31 reset signal, low active, from reset button on Personality board or Debug board
OSC_32KHz	A14	32.768KHz frequency output
UART3_RX	A16	i.MX31 UART3 serial data receive
UART3_TX	A17	i.MX31 UART3 serial data transmit
UART3_CTS	A18	i.MX31 UART3 clear to send
UART3_RTS	A19	i.MX31 UART3 request to send
UART2_RX	A20	i.MX31 UART2 serial data receive
UART2_TX	A21	i.MX31 UART2 serial data transmit
UART2_CTS	A22	i.MX31 UART2 clear to send
UART2_RTS	A23	i.MX31 UART2 request to send
UART1_RX	A24	i.MX31 UART1 serial data receive
UART1_TX	A25	i.MX31 UART1 serial data transmit
UART1_CTS	A26	i.MX31 UART1 clear to send
UART1_RTS	A27	i.MX31 UART1 request to send

Signal	Pin	Description
RFU	A28, B12, B13, B16, B17, B18, B19, B21, B22, E2, E14, F3, F11, F12, F13, F21, G7, G8, G9, G10, G11, H7, H8, H9, J13, K22	Reserved for future use
VDD_LCDIO	A29	LCD IO power supply
LCD_SD_I	A30	Data in for Serial Display, used for GPIO
LCD_HSYNC	A31	LCD Line sync
LCD_VSYNC	A32	LCD Vsync
LCD_LCS1_RST	A33	LCD module and TV-Out chip reset
LCD_G-1	A34	LCD data (for future use)
LCD_R-1	A35	LCD data (for future use)
LCD_B-1	A36	LCD data (for future use)
LCD_B0_D0	A37	LCD data0
LCD_B1_D1	A38	LCD data1
LCD_B2_D2	A39	LCD data2
LCD__R5_D17	A41	LCD data17
LCD_R3_D15	A42	LCD data15
LCD__R2_D14	A43	LCD data14
LCD_R0_D12	A44	LCD data12
LCD__G5_D11	A45	LCD data11
LCD_G3_D9	A46	LCD data9
LCD_G2_D8	A47	LCD data8
LCD_G0_D6	A48	LCD data6
LCD__B5_D5	A49	LCD data5
LCD_B3_D3	A50	LCD data3
USB_5V_VBUS	B1, B2	USB OTG 5V VBUS
3V3	B4, B5	3.3V power supply
WALL_5V_IN	B7, B8	DC 5.0V power supply
2V775	B10, B11	2.775V power supply
BATTERY_TEMP	B14	Battery temperature

Signal	Pin	Description
DEBUG	B23	Debug board version code
PERSONALITY1	B24	Personality board version code
PERSONALITY2	B25	Personality board version code
PERSONALITY3	B26	Personality board version code
CPU1	B27	CPU board version code
CPU2	B28	CPU board version code
CPU3	B29	CPU board version code
LCD_SD_DIO	B30	Data in/out for serial Display, can be used for GPIO
LCD_LSCLK_PLCK_FPS HIFT	B31	LCD shift
LCD_RD	B32	LCD Asynch. Port read
LCD_WR	B33	LCD Asynch. Port write
LCD_G-2	B34	LCD data (for future use)
LCD_R-2	B35	LCD data (for future use)
LCD_B-2	B36	LCD data (for future use)
LCD_CONTRAST	B37	LCD backlight contrast adjust
LCD_CLS	B38	LCD CLS
LCD_SPL_SPR	B39	LCD SPL
LCD_REV	B40	LCD REV
RFU_LCD2	B43, B45, B47, B49, C38, C39, C40, C41, C42, C43, C45, C47, C49, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, E44, E46, E48, F44, F45	Reserved for LCD future use
LCD_R4_D16	B42	LCD data16
LCD_R1_D13	B44	LCD data13
LCD__G4_D10	B46	LCD data10
LCD_G1_D7	B48	LCD data7
LCD_B4_D4	B50	LCD data4
VMAIN	C2, C3	Application power supply, from DC power or battery
LINEAR_A	C5	Linear regulator A

Signal	Pin	Description
LINEAR_B	C6	Linear regulator B
LINEAR_C	C7	Linear regulator C
LINEAR_D	C9	Linear regulator D
LINEAR_E	C10	Linear regulator E
LINEAR_F	C11	Linear regulator F
SLEEP_VSTBY	C12	Power management state retention
ON_OFF	C14	System On/Off signal
LI_CELL	C15	Coincell battery
VDD_I2C_IO	C16	I2C power supply
I2C1_DATA	C17	I2C1 data
I2C1_CLOCK	C18	I2C2 clock
I2C2_CLOCK	C20	I2C2 clock
I2C2_DATA	C21	I2C1 data
CSPI1_MOSI	C22	CSPI1 Master out/ Slave in
CSPI1_MISO	C24	CSPI1 Master in/ Slave out
CSPI1_SS0	C25	CSPI1 Slave select 0
CSPI1_SS1	C26	CSPI1 Slave select 1
CSPI1_SCLK	C28	CSPI1 serial clock
CSPI1_RDY	C29	CSPI1 signal ready
LCD_DRDY0	C30	LCD DRDY/VLD
LCD_SER_RS_DEN	C32	Asynch.Serial Port data/comm, used for GPIO
LCD_SD_CLK	C33	Serial Display clock
LCD_LCS0	C34	Asynch. Port chip select
LCD_VSYNC0	C35	LCD frame sync
LCD_PAR_RS	C36	Asynch. Parallel Port data/comm
CURRENT_MEAS_1	D1	Current Measure 1 (SW1 in CPU board)
CURRENT_MEAS_2	D2	Current Measure 2 (SW2A in CPU board)
CURRENT_MEAS_3	D4	Current Measure 3 (VMAIN in CPU board)

Signal	Pin	Description
CURRENT_MEAS_4	D5	Current Measure 4
CURRENT_MEAS_5	D7	Current Measure 5
CURRENT_MEAS_6	D8	Current Measure 6 (EXT_1V8 in Personality board)
CURRENT_MEAS_7	D10	Current Measure 7 (HDD_3V3 in Personality board)
CURRENT_MEAS_8	D11	Current Measure 8 (DC power supply in Personality board)
CURRENT_MEAS_9	D12	Current Measure 9 (battery power supply in Personality board)
CURRENT_MEAS_10	D13	Current Measure 10
PWR_EN	D14	Power enable, from MC13783 GPO
WI-FI_PWEN	D15	Wi-Fi Power enable
VDD_USB_IO	D16	USB IO power supply
USB_HS_OC	D17	USB Host over current
USB-HS_RESET_B	D18	USB Host reset signal
HDD_PWR_EN	D19	HDD power enable
HDD_DMARQ	D20	HDD DMA signal request
HDD_DIOW	D21	HDD IO signal read
HDD_DIOR	D22	HDD IO signalwrite
HDD_IORDY	D23	HDD IO signal ready
HDD_DMACK	D24	HDD DMA signal accept
HDD_INTRQ	D25	HDD Interrupt signal request
HDD_DA1	D26	HDD register address 1
HDD_DA0	D27	HDD register address 0
HDD_CS0	D28	HDD Command Block Registers selection
HDD_DA2	D29	HDD register address 2
HDD_CS1	D30	HDD Control Block Registers selection
HDD_RESET_B	D31	HDD reset signal
ATA_ENABLE_B	D32	HDD buffer enable signal
ATA_DIR	D33	HDD buffer direction signal

Signal	Pin	Description
USB_OTG_D_MINUS	D50	USB OTG data minus
AUDIO_LIN_R	E1	Audio Line in right
MIC_IN_P	E3	Microphone amplifier input
MIC_BIAS	E4	Microphone supply output with integrated bias resistor and detect
HEADPHONE_DETECT	E5	Headphone TV-Out insert detect
ADC_1	E6	ADC input 1(To distinguish the headphone or TV-Out insert)
ADC_2	E7	ADC input 2 (SD card write protect detect)
ADC_3	E9	ADC input 3
ADC_4	E10	ADC input 4
ADC_5	E11	ADC input 5
ADC_6	E12	ADC input 6
USB-HS-D0	E15	USB Host Data 0
USB-HS-D1	E16	USB Host Data 1
USB-HS-D2	E17	USB Host Data 2
USB-HS-D3	E18	USB Host Data 3
USB-HS_STP	E19	USB Host ULPI Stop signal
USB-HS-CLK	E20	USB Host ULPI Clock
HDD_D0	E22	HDD Data 0
HDD_D1	E23	HDD Data 1
HDD_D2	E24	HDD Data 2
HDD_D3	E26	HDD Data 3
HDD_D4	E27	HDD Data 4
HDD_D5	E28	HDD Data 5
HDD_D6	E30	HDD Data 6
HDD_D7	E31	HDD Data 7
HDD_D8	E32	HDD Data 8
HDD_D9	E34	HDD Data 9
HDD_D10	E35	HDD Data 10

Signal	Pin	Description
HDD_D11	E36	HDD Data 11
HDD_D12	E38	HDD Data 12
HDD_D13	E39	HDD Data 13
HDD_D14	E40	HDD Data 14
HDD_D15	E42	HDD Data 15
VDD_HDD_IO	E43	HDD IO Power supply
USB_OTG_D_PLUS	E50	USB OTG data plus
AUDIO_LIN_L	F1	Audio Line in left
BOOTSTRAP_0	F4	Boot Strap 0
BOOTSTRAP_1	F5	Boot Strap 1
BOOTSTRAP_2	F6	Boot Strap 2
BOOTSTRAP_3	F7	Boot Strap 3
BOOTSTRAP_4	F8	Boot Strap 4
BOOTSTRAP_5	F9	Boot Strap 5(Not used for i.MX31)
VDD_BOOTSTRAP	F10	Boot Strap Power supply
USB-HS-D4	F15	USB Host Data 4
USB-HS-D5	F16	USB Host Data 5
USB-HS-D6	F17	USB Host Data 6
USB-HS-D7	F18	USB Host Data 7
USB-HS_NXT	F19	USB Host ULPI Next signal
USB-HS_DIR	F20	USB Host ULPI Direction signal
FEC_TXD2	F22	FEC interface (NC for i.MX31)
FEC_TXD3	F23	FEC interface (NC for i.MX31)
FEC_RX_ER	F24	FEC interface (NC for i.MX31)
FEC_TXD0	F25	FEC interface (NC for i.MX31)
FEC_RXD1	F26	FEC interface (NC for i.MX31)
FEC_RXD2	F27	FEC interface (NC for i.MX31)
FEC_RXD3	F28	FEC interface (NC for i.MX31)

Signal	Pin	Description
FEC_TXD1	F29	FEC interface (NC for i.MX31)
FEC_MDIO	F30	FEC interface (NC for i.MX31)
FEC_MDC	F31	FEC interface (NC for i.MX31)
FEC_CRS	F32	FEC interface (NC for i.MX31)
FEC_INT_B	F33	FEC interface (NC for i.MX31)
FEC_TX_CLK	F34	FEC interface (NC for i.MX31)
FEC_RXD0	F35	FEC interface (NC for i.MX31)
FEC_RX_DV	F36	FEC interface (NC for i.MX31)
FEC_RESET_B	F37	FEC interface (NC for i.MX31)
FEC_RX_CLK	F38	FEC interface (NC for i.MX31)
FEC_COL	F39	FEC interface (NC for i.MX31)
FEC_TX_ER	F40	FEC interface (NC for i.MX31)
FEC_ENABLE	F41	FEC interface (NC for i.MX31)
FEC_TX_EN	F42	FEC interface (NC for i.MX31)
VDD_FEC_IO	F43	FEC interface (NC for i.MX31)
EB0	F46	LSB Byte strobe WEIM data enable; Controls d[7:0]
1_WIRE_DATA	F47	1 Wire data
LBA	F48	WEIM load base address
USB_OTG_UID	F49	USB OTG ID signal
AUDIO_LOUT_R	G1	Audio Line out right
HEADPHONE_RIGHT	G2	Headphone right
HEADPHONE_RETURN	G3	Headphone return(Connect with GND)
SPEAKER_RIGHT_P	G4	Handset loudspeaker and alert amplifier positive terminal
SPEAKER_RIGHT_N	G5	Handset loudspeaker and alert amplifier minus terminal
CMOS_FM_RST	G12	Camera sensor and FM module reset signal
CSI_PWDN	G13	Camera sensor power down
KP_ROW_7	G14	Keypad row 7
KP_ROW_6	G15	Keypad row 6

Signal	Pin	Description
KP_ROW_5	G16	Keypad row 5
KP_ROW_4	G17	Keypad row 4
KP_ROW_3	G18	Keypad row 3
KP_ROW_2	G19	Keypad row 2
KP_ROW_1	G20	Keypad row 1
KP_ROW_0	G21	Keypad row 0
KP_COL_7	G22	Keypad column 7
KP_COL_6	G23	Keypad column 6
KP_COL_5	G24	Keypad column 5
KP_COL_4	G25	Keypad column 4
KP_COL_3	G26	Keypad column 3
KP_COL_2	G27	Keypad column 2
KP_COL_1	G28	Keypad column 1
KP_COL_0	G29	Keypad column 0
GPS_INT_B	G30	GPS Interrupt
ACC_INT1	G31	Accelerometer interrupt 1
ACC_INT2	G32	Accelerometer interrupt 2
CMOS_FM_RST	G33	FM reset signal, low active
FM_CLK_EN	G34	FM clock enable
OSC_CLKO	G35	i.MX31 clock out
D14	G36	EIM data 14
D12	G37	EIM data 12
D10	G38	EIM data 10
D8	G39	EIM data 8
VDD_EIM_DATA	G40	EIM data power supply
D6	G41	EIM data 6
D4	G42	EIM data 4
D2	G43	EIM data 3

Signal	Pin	Description
D0	G44	EIM data 2
ECB_WAIT	G45	End Current burst
EB1	G46	LSB Byte strobe WEIM data enable; Controls D[15:8]
OE_B	G47	Memory output enable
CS4_B	G48	Chip select 4
CS2_B	G49	Chip select 2/ SDRAM sync flash chip select
CS0_B	G50	Chip select 0
AUDIO_LOUT_L	H1	Audio Line out Left
HEADPHONE_LEFT	H2	Headphone Left
SPEAKER_LEFT_P	H4	Handset earpiece speaker amplifier output positive terminal
SPEAKER_LEFT_N	H5	Handset earpiece speaker amplifier output minus terminal
VDD_CSI_IO	H10	Camera sensor power supply
CSI_HSYNC	H12	Camera sensor horizontal Sync
CSI_VSYNC	H13	Camera sensor vertical Sync
CSI_MCLK	H14	Camera sensor master clock
CSI_PIXCLK	H16	Camera sensor data latch clock
CSI_D0	H17	Camera sensor data 0
CSI_D1	H18	Camera sensor data 1
CSI_D2	H20	Camera sensor data 2
CSI_D3	H21	Camera sensor data 3
CSI_D4	H22	Camera sensor data 4
CSI_D5	H24	Camera sensor data 5
CSI_D6	H25	Camera sensor data 6
CSI_D7	H26	Camera sensor data 7
CSI_D8	H28	Camera sensor data 8
CSI_D9(MSB)	H29	Camera sensor data 9
GPS_PWEN	H30	GPS module power enable
GPS_USBHS_RST	H32	GPS reset, active low

Signal	Pin	Description
WI-FI_RST	H33	Wi-Fi reset, active low
BT_RST	H34	Bluetooth reset, active low
D15	H36	EIM data 15
D13	H37	EIM data 13
D11	H38	EIM data 11
D9	H39	EIM data 9
D7	H41	EIM data 7
D5	H42	EIM data 5
D3	H43	EIM data 3
D1	H44	EIM data 1
BCLK	H45	EIM burst clock
RW_B	H47	EIM read/write signal
CS5_B	H48	Chip select 5
CS3_B	H49	Chip select 3
CS1_B	H50	Chip select 1
TOUCH_X0	J1	Touch screen X0
TOUCH_X1	J2	Touch screen X1
TV_DAC_C_RETURN	J4	TV DAC return (reserved for future use)
TV_DAC_B_RETURN	J5	TV DAC return (reserved for future use)
TV_DAC_A_RETURN	J6	TV DAC return (reserved for future use)
SIM_CLK	J7	Sim card interface (reserved for future use)
SIM_RST	J8	Sim card interface (reserved for future use)
SIM_VEN	J9	Sim card interface (reserved for future use)
VDD_SIM_IO	J10	Sim card power supply
CHRG_LED	J11	Charge LED
VDD_JTAG	J12	JTAG power supply
CPLD_PGM_TDI	J14	CPLD JTAG interface (Reserved for future use)
CPLD_PGM_TDO	J15	CPLD JTAG interface (Reserved for future use)

Signal	Pin	Description
CPLD_PGM_TMS	J16	CPLD JTAG interface (Reserved for future use)
CPLD_PGM_TCK	J17	CPLD JTAG interface (Reserved for future use)
SSI1_STXD	J18	SSI1 interface TxD signal
SSI1_SRXD	J19	SSI1 interface RxD Signal
SSI1_SFS	J20	SSI1 interface Frame Sync
SSI1_SCK	J22	SSI1 interface Serial Clock
SSI2_STXD	J23	SSI2 interface TxD signal
SSI2_SRXD	J24	SSI2 interface RxD Signal
SSI2_SFS	J26	SSI2 interface Frame Sync
SSI2_SCK	J27	SSI2 interface Serial Clock
SD1_D0	J28	SD card 1 data 0
SD1_D1	J29	SD card 1 data 1
SD1_D2	J30	SD card 1 data 2
SD1_D3	J31	SD card 1 data 3
VDD_SD2_IO	J32	SD card 2 power supply
SD2_D0	J33	SD card 2 data 0
SD2_D1	J34	SD card 2 data 1
SD2_D2	J35	SD card 2 data 2
SD2_D3	J36	SD card 2 data 3
VDD_EIM_ADDR	J37	EIM address power supply
A24	J38	EIM address 24
A22	J39	EIM address 22
A20	J40	EIM address 20
A18	J41	EIM address 18
A16	J42	EIM address 16
A14	J43	EIM address 14
A12	J44	EIM address 12
A10	J45	EIM address 10

Signal	Pin	Description
A8	J46	EIM address 8
A6	J47	EIM address 6
A4	J48	EIM address 4
A2	J49	EIM address 2
A0	J50	EIM address 0
TOUCH_Y0	K1	Touch screen Y0
TOUCH_Y1	K2	Touch screen Y1
TV_DAC_C	K4	TV DAC (reserved for future use)
TV_DAC_B	K5	TV DAC (reserved for future use)
TV_DAC_A	K6	TV DAC (reserved for future use)
SIM_RX	K7	Sim card interface (reserved for future use)
SIM_PD	K8	Sim card interface (reserved for future use)
SIM_TX	K9	Sim card interface (reserved for future use)
JTAG_TRST_B	K10	JTAG TAP Reset
JTAG_TDI	K11	JTAG TAP Data In
JTAG_TMS	K12	JTAG TAP Mode select
JTAG_TCK	K13	JTAG TAP clock
JTAG_RTCK	K15	JTAG ARM Debug Test Clock
JTAG_DE_B	K16	JTAG Debug Enable
JTAG_TDO	K17	JTAG TAP data out
JTAG_RESET_B	K18	JTAG reset signal
MLB_SIG	K19	Reserved for Future use
MLB_DAT	K20	Reserved for Future use
MLB_CLK	K21	Reserved for Future use
CAN TX1 RFU	K23	Reserved for Future use
CAN RX1 RFU	K24	Reserved for Future use
CAN TX2 RFU	K25	Reserved for Future use
CAN RX2 RFU	K26	Reserved for Future use

Signal	Pin	Description
VDD_MLB	K27	Reserved for Future use
SD1_CMD	K28	SD card 1 Command signal
SD1_DET	K29	SD card 1 Detect signal
SD1_WP	K30	SD card 1 write protect
SD1_CLK	K31	SD card 1 clock signal
VDD_SD1_IO	K32	SD card 1 power supply
SD2_CMD	K33	SD card 2 Command signal
SD2_DET	K34	SD card 2 Detect signal
SD2_WP	K35	SD card 2 write protect
SD2_CLK	K36	SD card 2 clock signal
A25	K38	EIM Address 25
A23	K39	EIM Address 23
A21	K40	EIM Address 21
A19	K41	EIM Address 19
A17	K42	EIM Address 17
A15	K43	EIM Address 15
A13	K44	EIM Address 13
A11	K45	EIM Address 11
A9	K46	EIM Address 9
A7	K47	EIM Address 7
A5	K48	EIM Address 5
A3	K49	EIM Address 3
A1	K50	EIM Address 1

5.2 TV/Headphone Jack

The TV/Headphone jack is used for both TV and headphone. The pin-out works with off-the-shelf cables for Microsoft Zune® and Apple® iPod®. Figure 5-1 shows the pin-out and schematic.

The Chrontel® TV encoder chip enables the software to detect the host device into which the jack is plugged (TV or headphone).

- By default, pin 2 of the jack is pulled up and is for headphone detection.
- Upon power up, the software detects the status of pin 2. If pulled up, a headphone has been detected; otherwise, video is detected.

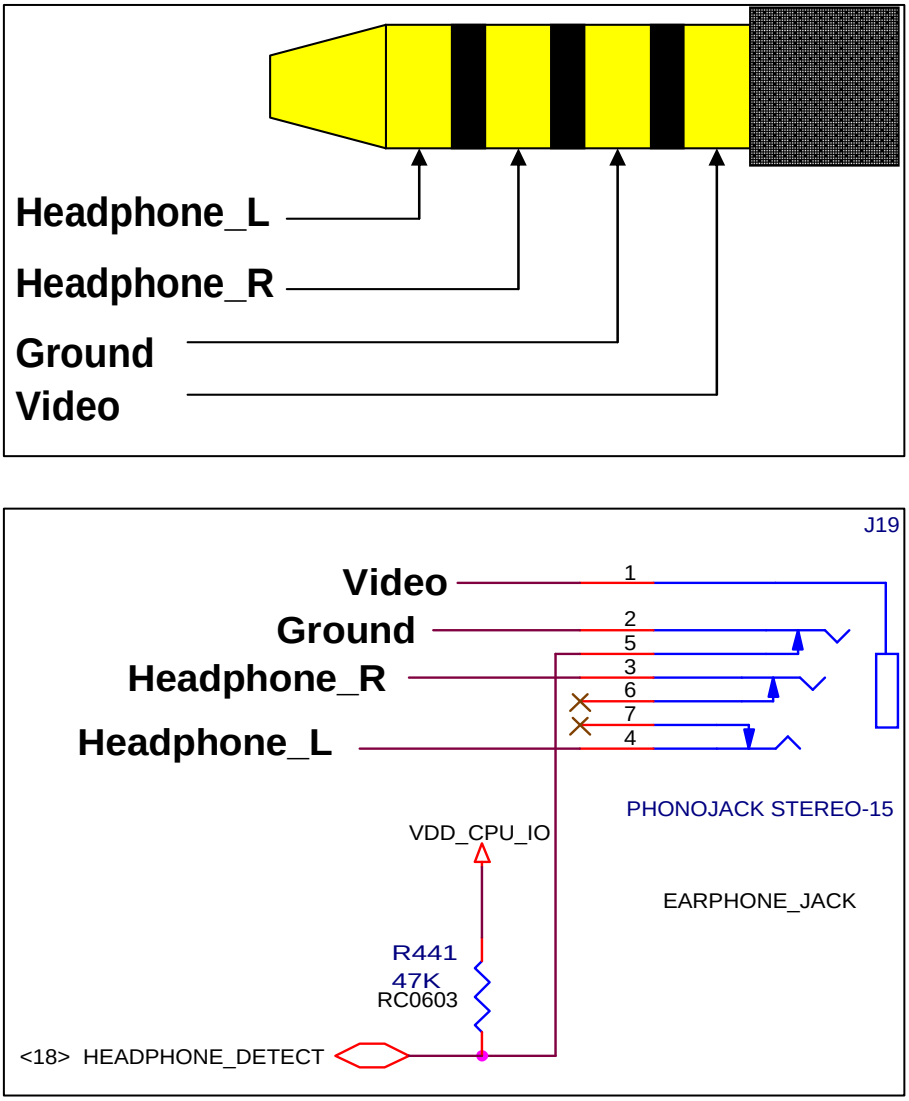

Figure 5-1 TV/Headphone Jack Pin-out and Schematics

5.3 LCD Connector

On the Personality board, J14 is the connector to the EPSON® 2.7 VGA Display L4F00242T03. Table 5-3 provides the pin information, where the column abbreviations are as follows:

```
I=input pin, O=output pin, R=reference pin, P=power supply pin, NC = not
connected
```

Table 5-3 LCD Connector Pin-Out

Pin No.	Symbol	Function	I/O	Remarks
1	YU	Y-Top	R	Touch Panel
2	XR	X_Right	R	Touch Panel
3	YD	Y_Bottom	R	Touch Panel
4	XL	X_Left	R	Touch Panel
5	GND	Ground	P	
6	GND	Ground	P	
7	VSYNC	Vertical Synchronous Signal	I	Display Interface
8	HSYNC	Horizontal Synchronous Signal	I	Display Interface
9	DE	Data Enable Signal	I	Display Interface
10	GND	Ground	P	
11	PCLK	Data Clock	I	Display Interface
12	GND	Ground	P	
13	B0	Display Data	I	Blue Data LSB
14	B1	Display Data	I	Blue Data
15	B2	Display Data	I	Blue Data
16	B3	Display Data	I	Blue Data
17	B4	Display Data	I	Blue Data
18	B5	Display Data	I	Blue Data MSB
19	GND	Ground	P	
20	G0	Display Data	I	Green Data LSB
21	G1	Display Data	I	Green Data
22	G2	Display Data	I	Green Data
23	G3	Display Data	I	Green Data
24	G4	Display Data	I	Green Data
25	G5	Display Data	I	Green Data MSB
26	GND	Ground	P	
27	R0	Display Data	I	Red Data LSB

Pin No.	Symbol	Function	I/O	Remarks
28	R1	Display Data	I	Red Data
29	R2	Display Data	I	Red Data
30	R3	Display Data	I	Red Data
31	R4	Display Data	I	Red Data
32	R5	Display Data	I	Red Data MSB
33	GND	Ground	P	
34	XRESET	Reset	I	L: Reset Active
35	XCS	Chip Select	I	I: Chip Select Active
36	SCLK	Serial Clock	I	Command Interface
37	DIN	Serial Data	I	Command Interface
38	NC		N.C.	not connected
39	GND	Ground	P	
40	VDDI	VDDI	P	1.8 volts
41	VDDI	VDDI	P	1.8 volts
42	VDD	VDD	P	2.8 volts
43	VDD	VDD	P	2.8 volts
44	LED_K	LED Cathode	P	Cathode
45	LED_A	LED Anode	P	Anode

5.4 Keypad

The keypad is implemented on the Personality board. The keypad provides nine buttons, and is used for applications that require control and navigation capabilities.

As shown in Figure 5-2, the buttons provide the following navigation functions:

Red arrows: LEFT, RIGHT, UP, DOWN

ENTER: at the center of the red arrows

Menu 1 through **Menu 4**

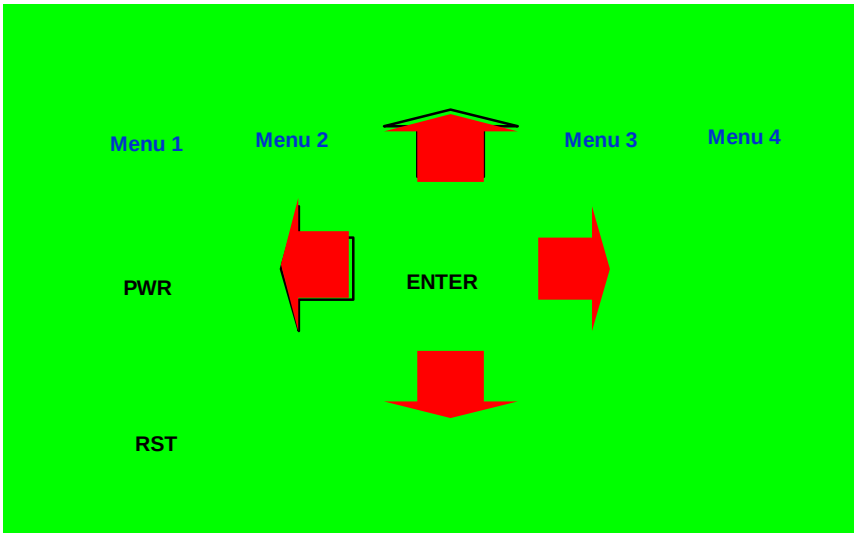

Figure 5-2 Keypad

The Personality Board also provides the following:

- An expansion connector to support an 8 x 8 matrix Keypad for a diverse set of low-cost applications requiring a keyboard or keypad-like interface.
- (Currently not implemented). A 24-pin connector (**CN20**) is ready for use as a Keypad expansion.

5.5 Current Measurement Connector

For this 3-Stack system, measuring the current at various points of the CPU engine and Personality board is important to device development and power tracking.

The current measurement connector (J3 on the Debug board) is used to determine overall power management and efficiency. Figure 5-3 displays the J3 Pin-out.

The following areas are monitored:

- CURRENT_MEAS_1: Core Power Supply output from PMIC chip
- CURRENT_MEAS_2: Memory voltage power output from PMIC chip
- CURRENT_MEAS_3: 3.3V power output from PMIC chip
- CURRENT_MEAS_6: 1.8V for external device power supply in
- CURRENT_MEAS_7: 3.3V for HDD power supply in
- CURRENT_MEAS_8: DC power supply in
- CURRENT_MEAS_9: Battery power supply in

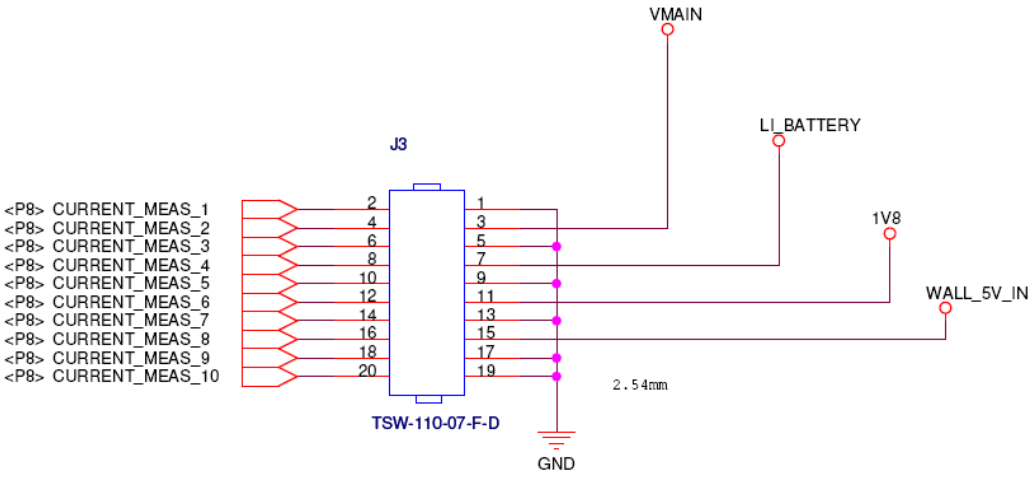

Figure 5-3 Current Measurement Connector Pin-out

5.6 Battery Operation

You can also use an Apple iPod battery or an iPod replacement battery to provide power to the Personality board. The battery is not included with the 3-Stack system. The CN15 battery connector is compatible with the iPod battery connector.