UG10146

MCXW71 Hardware Design Guide

Rev. 1.0 — 10 September 2024 **User guide**

Document information

Information	Content
Keywords	UG10146, MCX, MCX W, MCXW71, Bluetooth LE, HVQFN, microstrip topology, coplanar waveguide
Abstract	This document provides guidelines related to printed-circuit board (PCB) design and layout for hardware platforms based on an NXP MCXW71 MCU.

1 Introduction

This document provides guidelines related to printed-circuit board (PCB) design and layout for hardware platforms based on an NXP MCXW71 MCU. The document describes the following packages for the MCXW71 devices:

- 48-pin heat sink very-thin quad-flat pack no-lead (HVQFN) wettable flank plastic package
- 40-pin HVQFN wettable flank plastic package

The document also describes the MCXW71 device footprint and provides recommendations for EMC layout, DC-DC supply layout, radio layout, crystal layout, RF circuit, and antenna.

Note: *The design guidelines provided in this document are for reference purposes only. Depending on board hardware assembly and other board components, the guidelines may vary slightly from one board to another.*

2 MCXW71 device package marking

Figure 1 shows the markings on an example MCXW71 device HVQFN package.

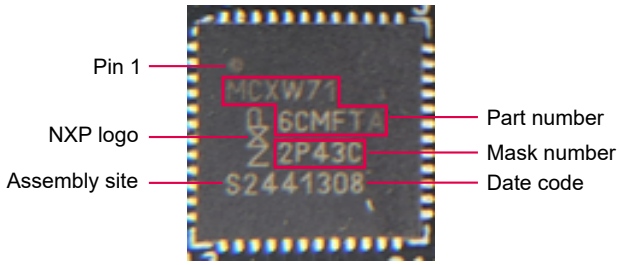


Figure 1. MCXW71 device HVQFN package marking

Note: *The part number shown in Figure 1 is an example part number and not all MCXW71 devices have the same part number.*

3 48-pin HVQFN package

This section contains the following subsections:

- Section 3.1 "48-pin package dimensions"
- Section 3.2 "48-pin package component copper layer"

3.1 48-pin package dimensions

The 48-pin HVQFN package (SOT619-17(D)) has the following dimensions:

- Length: 7 mm
- Width: 7 mm
- Height: 0.85 mm
- Pitch: 0.5 mm

Figure 2 shows the 48-pin HVQFN package dimensions.

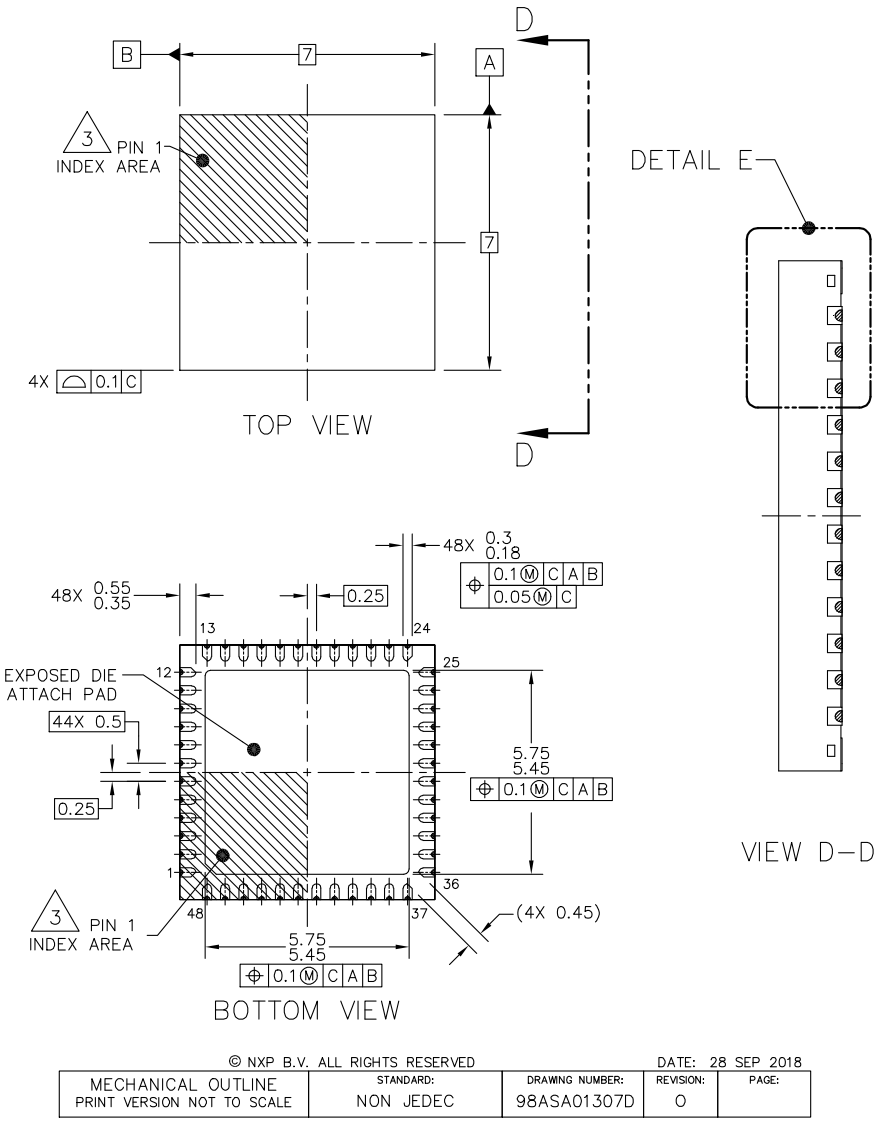


Figure 2. 48-pin package dimensions

3.2 48-pin package component copper layer

The top layer of the 48-pin package is the metal (copper) layer where components are soldered. The package footprint contains 48 copper-exposed (chip contact) pads and 1 centered ground pad. Figure 3 shows the package top layer with the recommended solderable area.

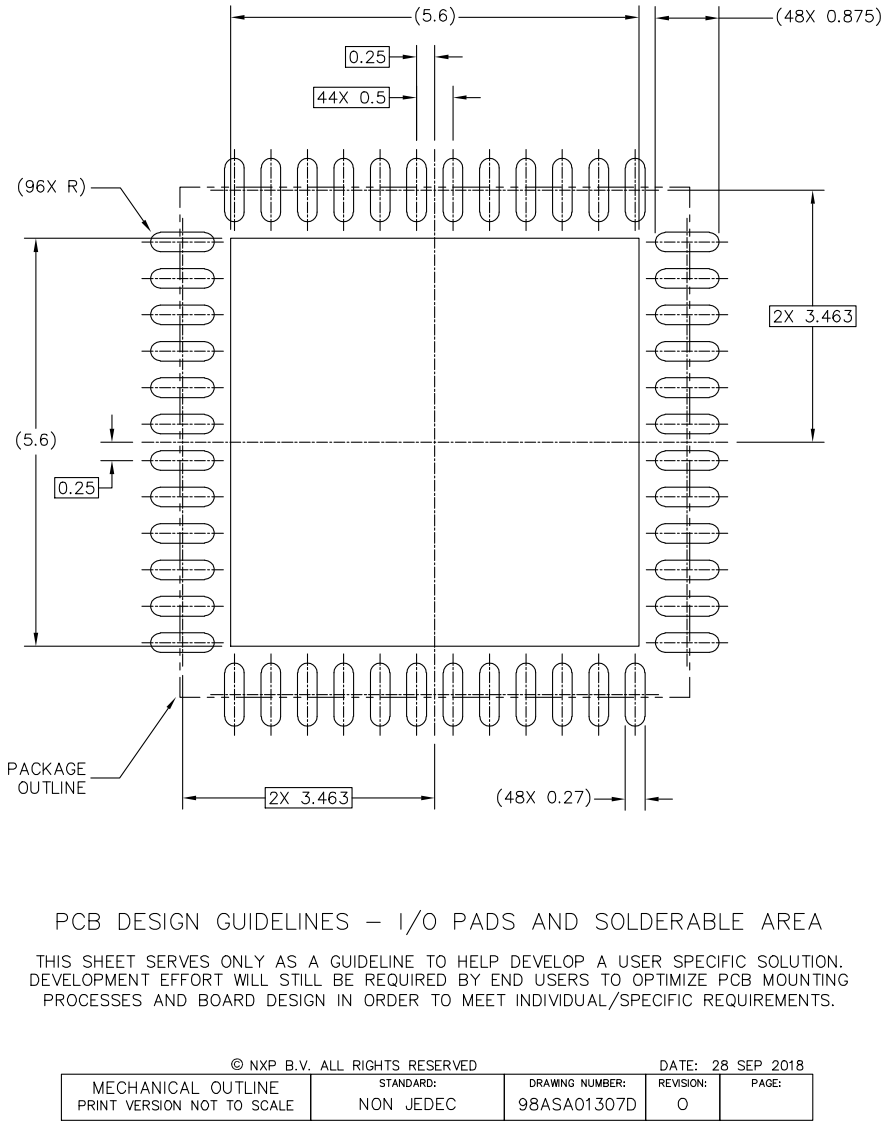
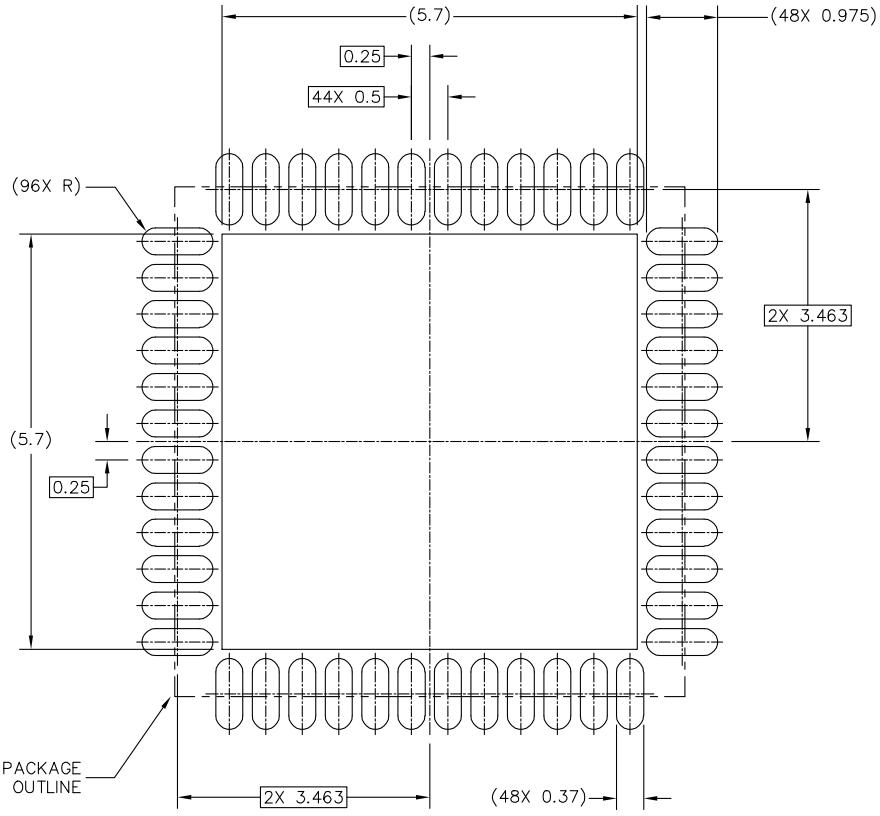


Figure 3. 48-pin package I/O pads and solderable area

To connect the top layer to the ground plane layers, use 0.25 mm via holes. The via holes are required for RF grounding. They also prevent the solder paste from floating.

3.2.1 48-pin package solder mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 4 shows the recommended solder mask pattern for a 48-pin HVQFN package. The pattern represents openings in the solder mask.



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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Figure 4. 48-pin package solder mask opening pattern

3.2.2 48-pin package solder paste stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 5 shows the recommended solder paste stencil pattern for a 48-pin HVQFN package. The stencil thickness should be approximately 0.1 mm.

If too much solder paste is applied, alternative patterns and opening sizes can be used. For more information and recommendations on how to avoid the solder paste leakage between the vias, see Section 7.1.

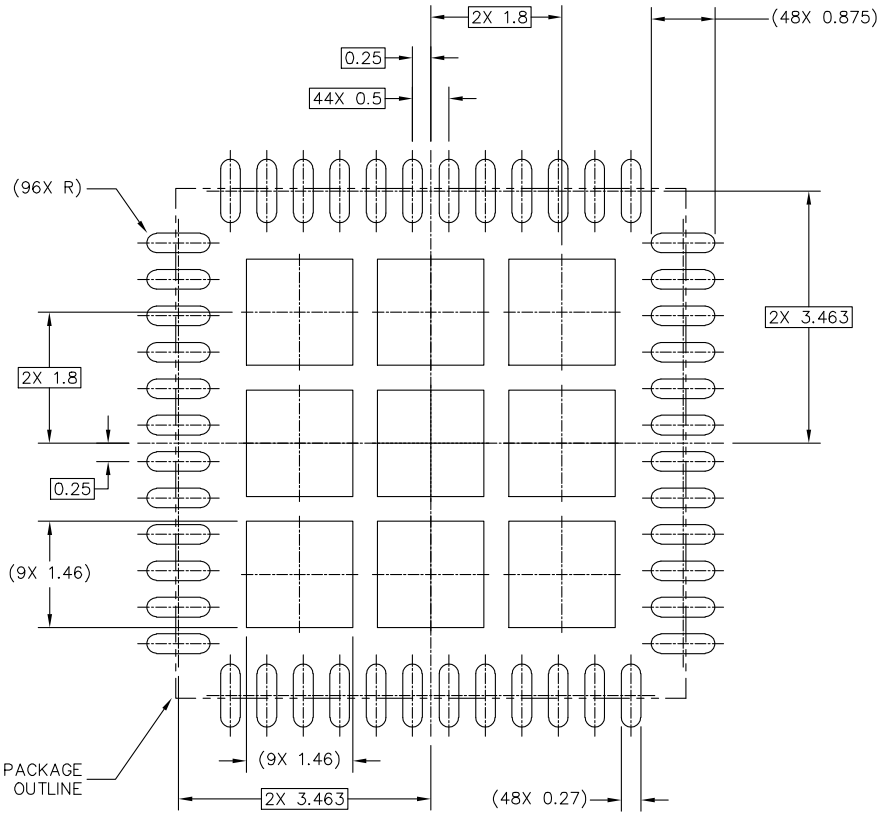


Figure 5. 48-pin package solder paste stencil

4 40-pin HVQFN package

This section contains the following subsections:

- Section 4.1 "40-pin package dimensions"
- Section 4.2 "40-pin package component copper layer"

4.1 40-pin package dimensions

The 40-pin HVQFN package (SOT618-13(DD)) has the following dimensions:

- Length: 6 mm
- Width: 6 mm
- Height: 0.85 mm
- Pitch: 0.5 mm

Figure 6 shows the 40-pin HVQFN package dimensions.

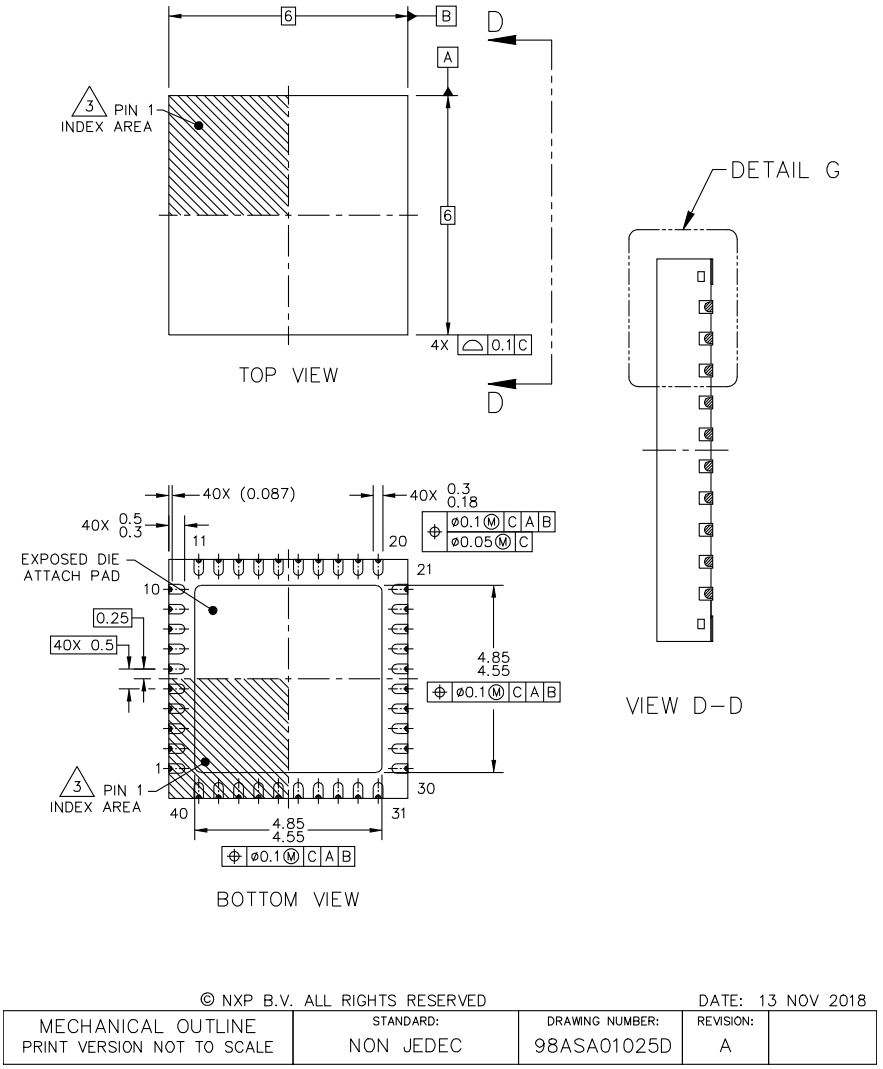
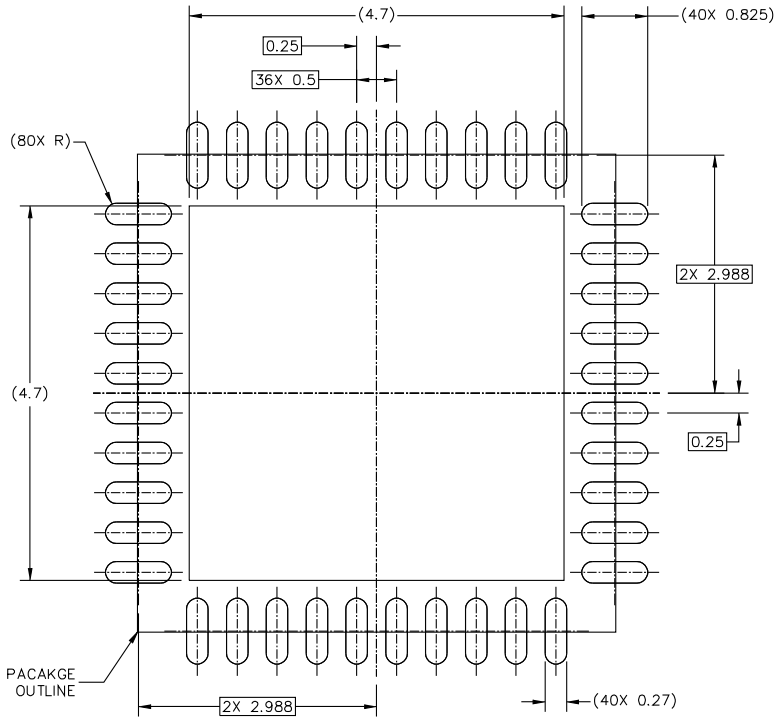


Figure 6. 40-pin package dimensions

4.2 40-pin package component copper layer

The top layer of the 40-pin package is the metal (copper) layer where components are soldered. The package footprint contains 40 copper-exposed (chip contact) pads and 1 centered ground pad. Figure 7 shows the package top layer with the recommended solderable area.



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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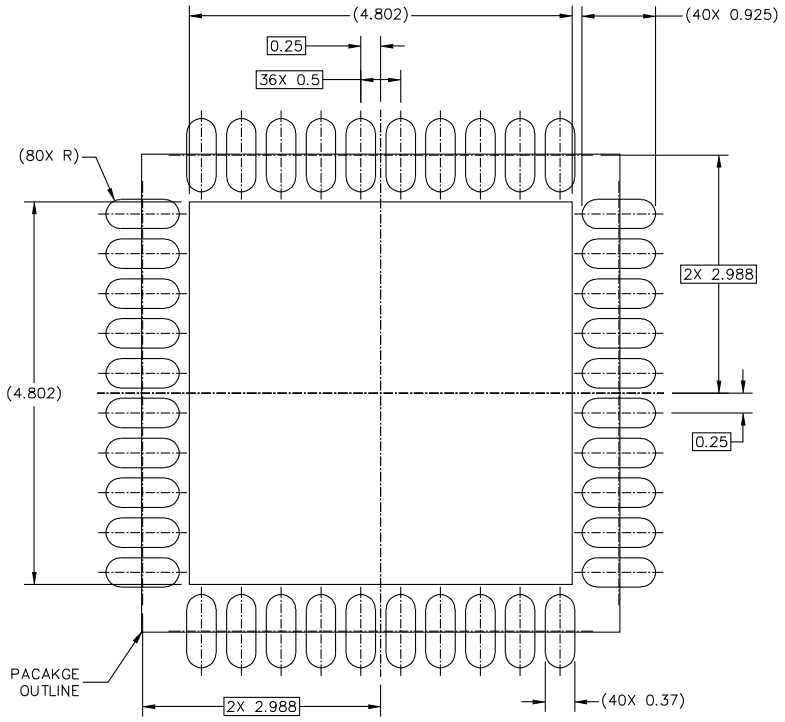
Figure 7. 40-pin package I/O pads and solderable area

To connect the top layer to the ground plane layers, use 0.25 mm via holes. The via holes are required for RF grounding. They also prevent the solder paste from floating.

4.2.1 40-pin package solder mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 8 shows the recommended solder mask pattern for a 40-pin HVQFN package. The pattern represents openings in the solder mask.



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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Figure 8. 40-pin package solder mask opening pattern

4.2.2 40-pin package solder paste stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 9 shows the recommended solder paste stencil pattern for a 40-pin HVQFN package. The stencil thickness should be approximately 0.1 mm.

If too much solder paste is applied, alternative patterns and opening sizes can be used. For more information and recommendations on how to avoid the solder paste leakage between the vias, see Section 7.1.

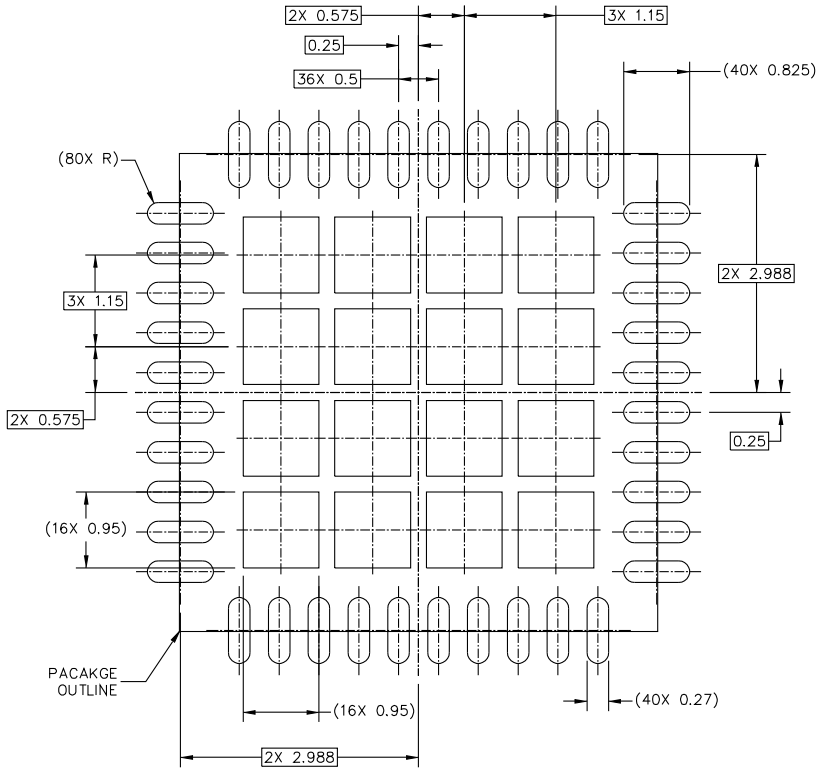

Figure 9. 40-pin package solder paste stencil

5 QFN package soldering profile

Figure 10 shows the recommended soldering profile for a 48-pin HVQFN package, in a board size of approximately 3.2 inches x 2.1 inches.

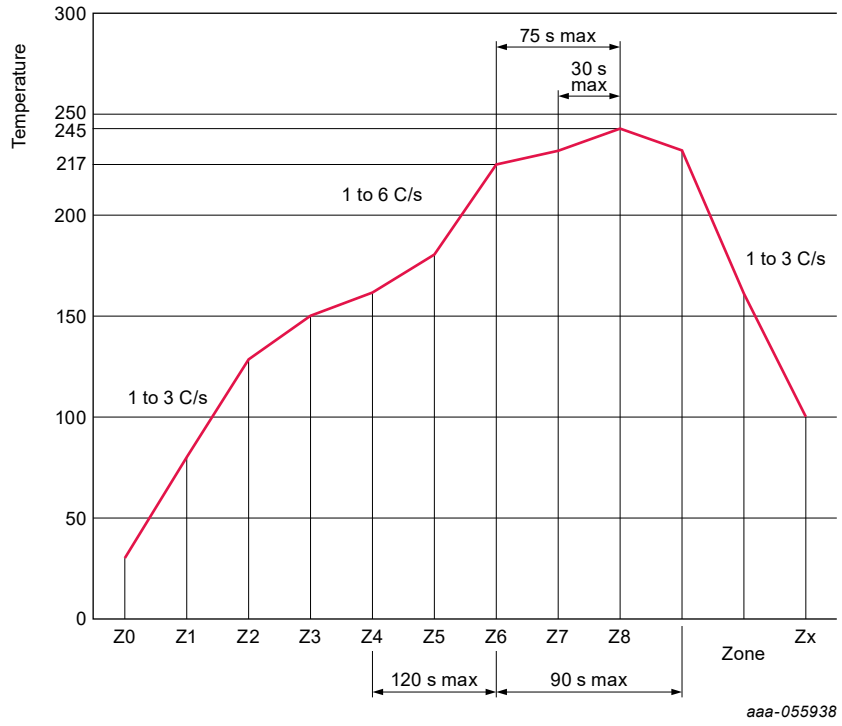

Figure 10. QFN soldering profile

6 QFN package excess solder paste problem

Excess solder paste may cause the QFN package to float or bridge between the package contacts. To apply the right amount of solder paste to the PCB, consider the following factors:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

Note: *For details on package assembly guidelines, refer to Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages (AN1902).*

7 Board design and layout recommendations

To create a successful wireless hardware design, you have to put special attention on device footprint, RF layout, circuit matching, antenna design, and RF measurement capability. RF circuit design, layout, and antenna design require specialized knowledge, expertise, and tools.

With hardware reference designs from NXP, RF design guideline documents, and guidelines provided in this document, hardware engineers can design Bluetooth Low Energy (LE) radio boards with good performance levels.

Figure 11 shows the NXP FRDM-MCXW71 board, containing the MCXW71 device and all necessary I/O connections.

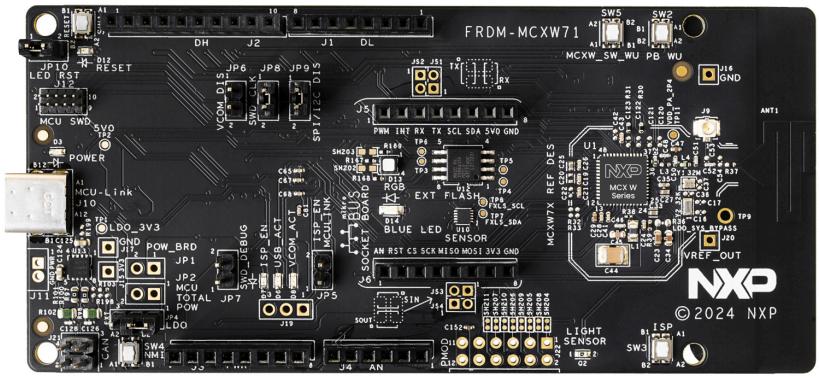

Figure 11. FRDM-MCXW71 board

Device footprint and layout are critical factors of a board design and their design implementation impacts the radio frequency (RF) performance. Therefore, to achieve optimal RF performance, you should use NXP-recommended RF hardware reference designs that are optimized for radio performance. If the recommended footprint and design are followed exactly in the RF region of the board, you are likely to get first-time success with your board on the following parameters:

- Sensitivity
- Output power
- Harmonic and spurious radiation
- Frequency range

Figure 12 shows an example board layout with the critical RF section highlighted. For optimal RF performance, the critical RF section must be copied exactly. The remaining layout area is less critical, and it can be modified without reducing RF performance.

Note: *For exact dimensions, refer to the FRDM-MCXW71 board design files.*

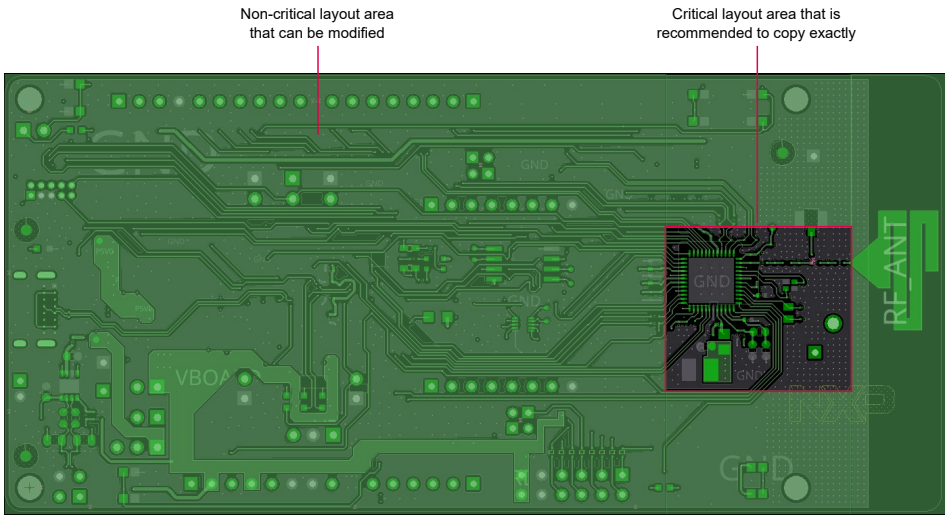

Figure 12. Critical layout area

The subsections that follow provide design and layout recommendations related to device footprint, RF circuit, and antenna for a wireless hardware design.

7.1 MCXW71 device footprint recommendations

Device footprint greatly impacts the performance of the wireless link. Therefore, a device footprint must be created with a lot of care and attention. To enable board matching and minimize the component count, keep the receiver sensitivity and output power optimized while creating the device footprint.

Figure 13 highlights the critical factors of the device die flag area in the FRDM-MCXW71 board. The critical factors include:

- Ground vias and locations
- RF output and ground traces
- Solder paste opening shapes
- Die flag shape
- Test pins

NXP strongly recommends you to keep the die flag of your MCXW71 board exactly the same (including via locations) as shown in Figure 13. Any deviation from the recommended die flag may cause performance degradation.

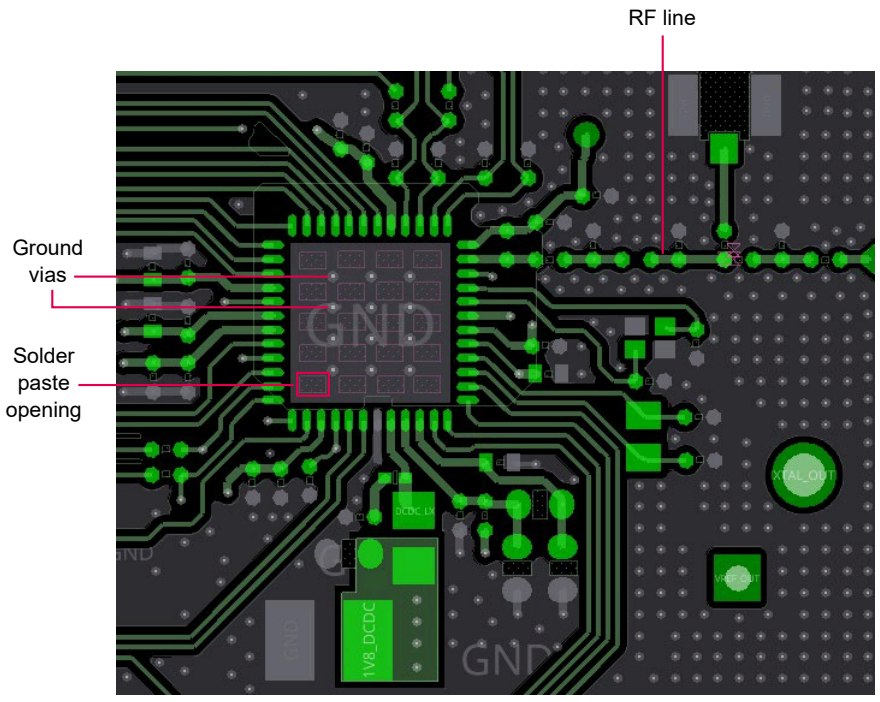

Figure 13. Critical factors of die flag area

To replicate the transmission lines shown in Figure 13, you must copy the PCB stackup, along with the physical layout of the circuit. A small change in the thickness of the dielectric substrate under the transmission line may have a significant impact on the impedance. For example, consider a 50 Ω trace that is 18 mils wide over 10 mils of FR4. If the thickness of FR4 is changed from 10 mils to 6 mils, the impedance becomes 36 Ω. Such information is available in the fabrication notes for a board design.

When the top layer dielectric becomes too thin, the layers do not act as a true transmission line, even if all the dimensions are correct. Although no universal industry agreement is available on the minimum dielectric thickness, NXP prefers to use a top layer dielectric thickness of no less than 8-10 mils. Using a correct substrate (for example, FR4) with a dielectric constant of 4.3 helps in achieving a good RF design.

To summarize, a wide transmission line (coplanar waveguide) and a thick interlayer of substrate are two key factors to create a robust RF design during the manufacturing phase.

7.1.1 DC-DC supply layout recommendations

Figure 14 shows example DC-DC supply circuit diagrams from the FRDM-MCXW71 board schematics.

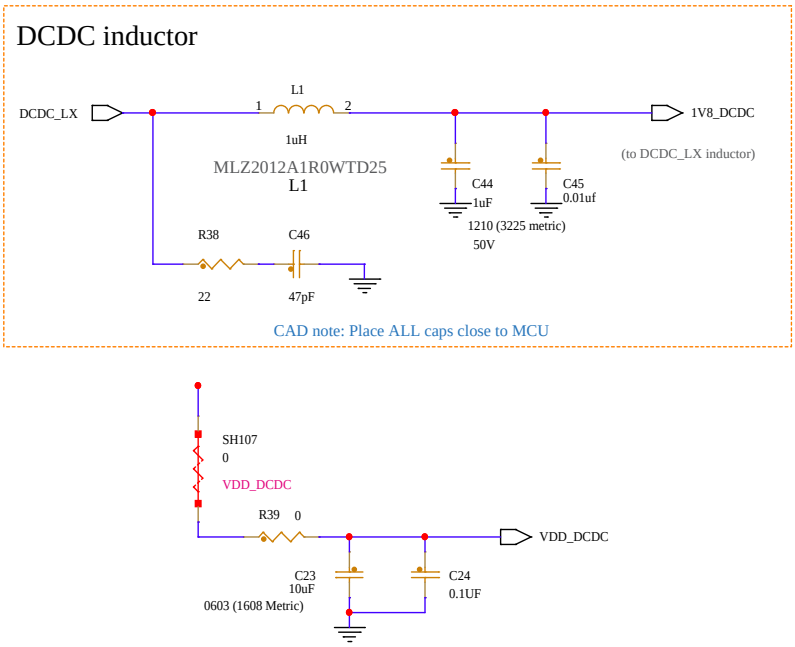

Figure 14. DC-DC supply circuit diagrams

Figure 15 shows the DC-DC supply layout for the FRDM-MCXW71 board.

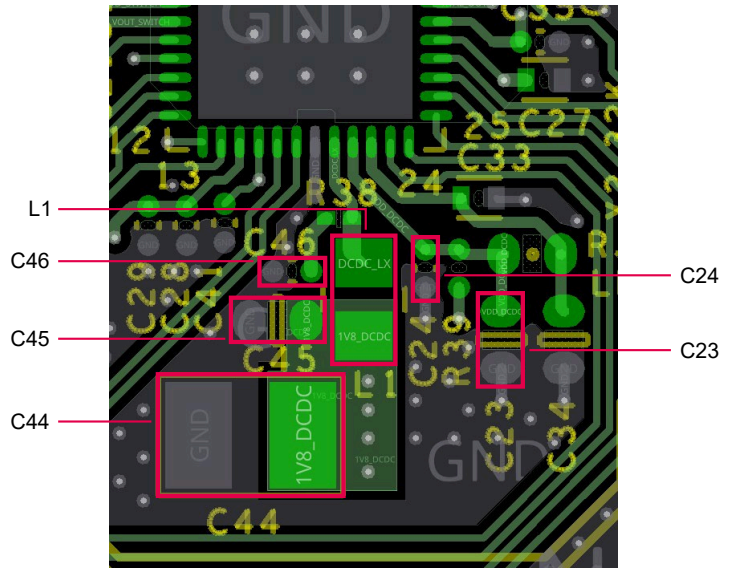

Figure 15. DC-DC supply layout

The following are some recommendations for creating an optimal DC-DC supply layout:

- Place the C23 and C24 capacitors as near as possible to the VDD_DCDC pin, as compared to the VSS_DCDC pin. NXP recommends placing these capacitors such that the LX connection to the inductor passes between their terminals. Try to reduce the number of loops formed between the VDD_DCDC / VSS_DCDC pins and the C23 and C24 capacitors. If needed, add more vias to the ground plane.

- Place the C45 capacitor such that its connection to the inductor L1 is as shown in Figure 15. Also, keep the VSS connection as near as possible to the MCXW71 chip. To create a better VSS connection to the ground plane, you can add more vias.
- Place the C44 capacitor as near as possible to the chip and add vias as shown in Figure 15.
- Similar to the C45 capacitor, correct placement of the C46 capacitor may also help achieve better performance for emissions higher than 300 MHz.
- In the FRDM-MCXW71 board, the L1 inductor for the MCXW71 device has a value of 1 µH.

To summarize, having short connections and small area loops help reduce emissions. Placing the capacitors mentioned above near the chip also helps to achieve this goal. In addition, having the ground plane well preserved underneath the mentioned components (as done in the current layout) greatly helps reduce the impact of not having the inductor near the chip.

7.1.2 Crystal layout recommendations

The following are some recommendations for creating an optimal crystal layout:

- For each of the 32 MHz and 32.768 kHz crystals, try to keep the crystal wires symmetric to each other.
- Placing the 32.768 kHz crystal near the MCXW71 chip is not required.

Figure 16 shows an example crystal layout.

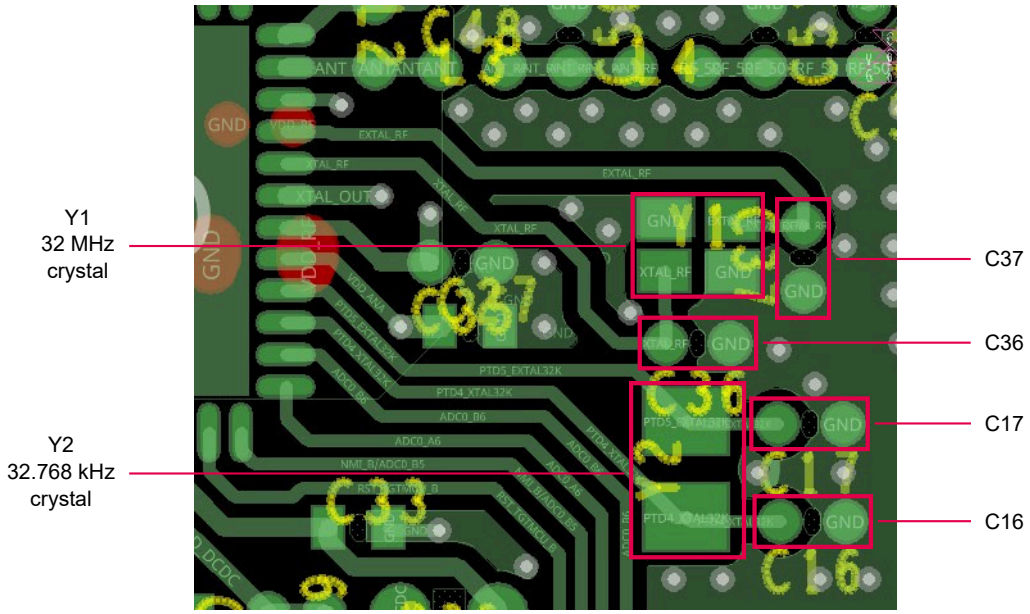

Figure 16. Crystal layout

The subsections below provide some other recommendations for 32 MHz crystal layout:

- Section 7.1.2.1 "Ensure isolation from antenna signal"
- Section 7.1.2.2 "Open ground and power planes"
- Section 7.1.2.3 "Apply shielding"

7.1.2.1 Ensure isolation from antenna signal

Ensure proper isolation for crystal circuit components from antenna signal. For better isolation:

- Place crystal circuit components perpendicular to the antenna signal path.
- Extend vias under the XTAL and EXTAL wires up to layer 3.

Figure 17 shows isolation recommendations for crystal circuit components.

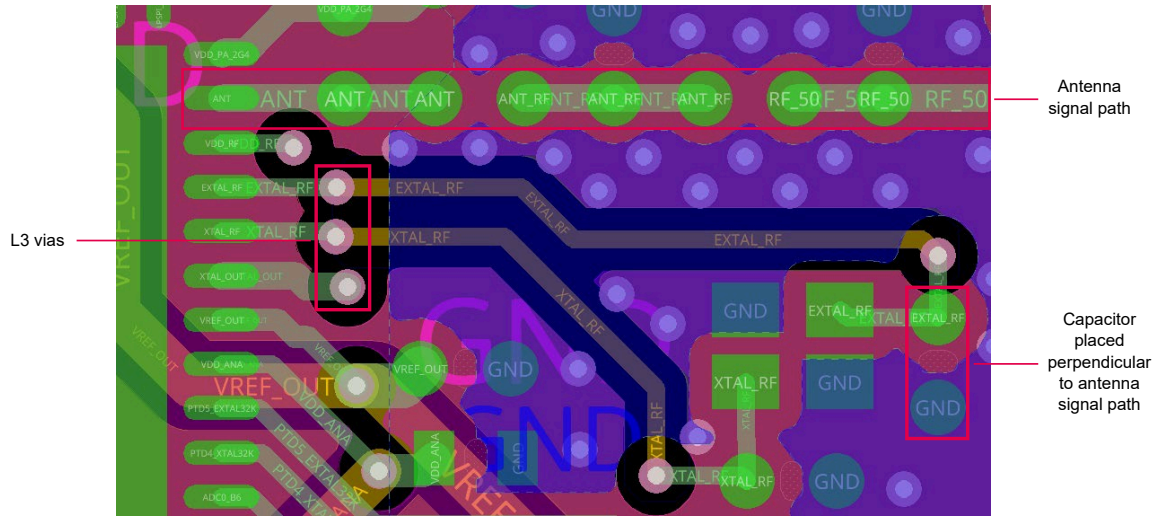

Figure 17. Crystal circuit component isolation (layer 1 - top)

7.1.2.2 Open ground and power planes

To reduce capacitance on the XTAL and EXTAL wires, you can open the ground plane over these wires (see Figure 18). Opening the ground plane on the top layer (layer 1) also provides shielding for the components.

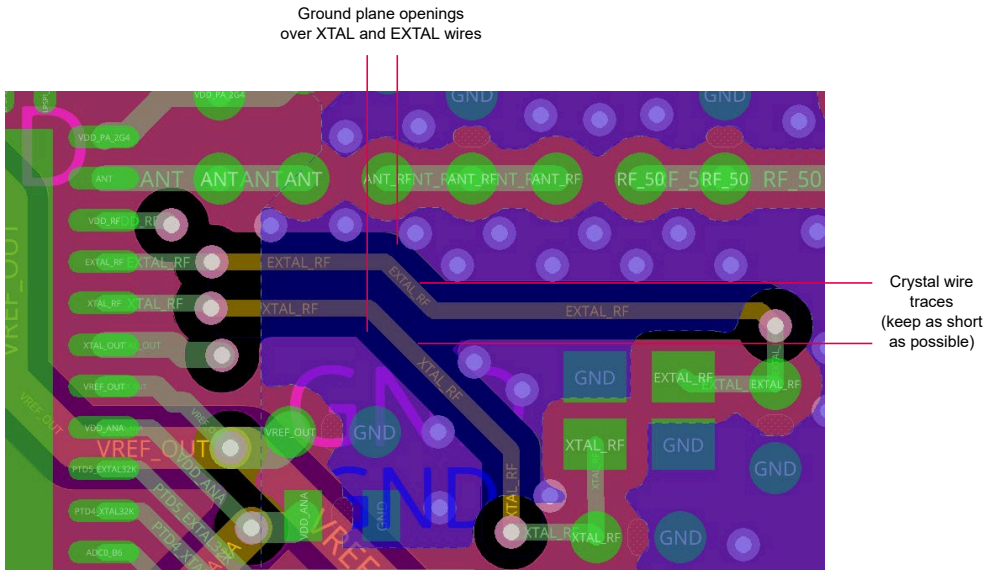

Figure 18. Ground plane openings (layer 2 - ground)

To reduce coupling capacitance to the power signal, open the power nets under the XTAL and EXTAL wires, as shown in Figure 19.

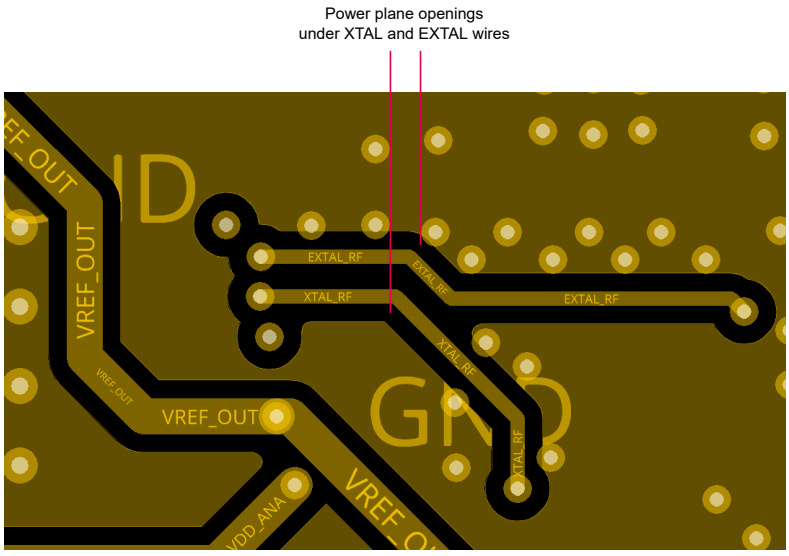

Figure 19. Power plane openings (layer 3 - power)

7.1.2.3 Apply shielding

To avoid any couplings between the XTAL_RF and XTAL_OUT wires, shielding is applied on the power plane. Similarly, to avoid any couplings on the 32 MHz crystal, shielding is applied on the top layer (see Figure 20).

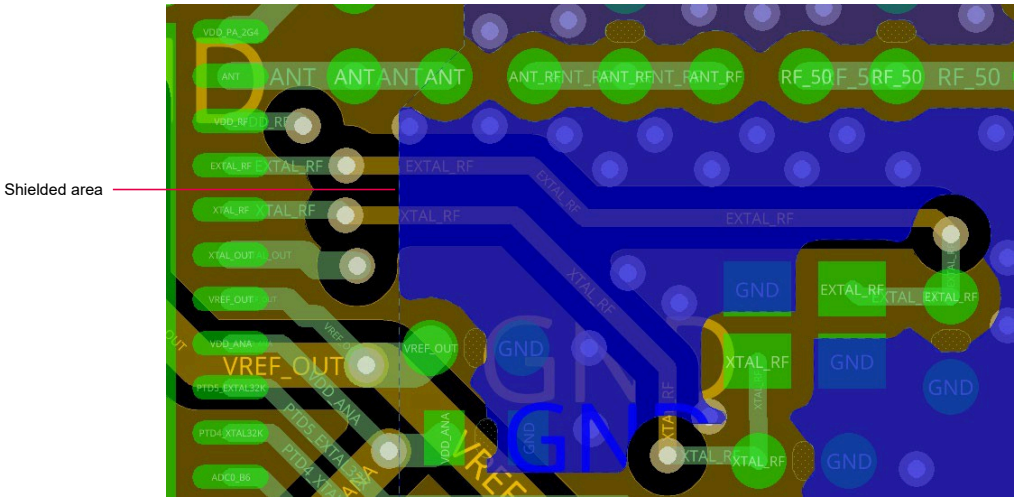

Figure 20. Shielding in top layer

7.1.3 EMC layout recommendations

For radio certification, your board design must meet acceptable electromagnetic compatibility (EMC). The following are some recommendations to achieve better EMC layout:

- If your hardware design uses MCXW71 pins PTC0, PTC1, PTC2, and PTC3; try creating an optimal layout for the circuitry related to these pins.
- For each of these pins, place a decoupling capacitor of 3 pF as near as possible to the pin. It helps in enchaining EMC.

- To enhance EMC, you can add a 3 pF decoupling capacitor with 4.8 GHz resonance for each pin. For each pin, place its decoupling capacitor as near as possible.
- Wires from the four pins must be under the current layer.
- If your hardware design rules allow, put vias under the MCXW71 package.

Figure 21 shows an example layout with EMC recommendations.

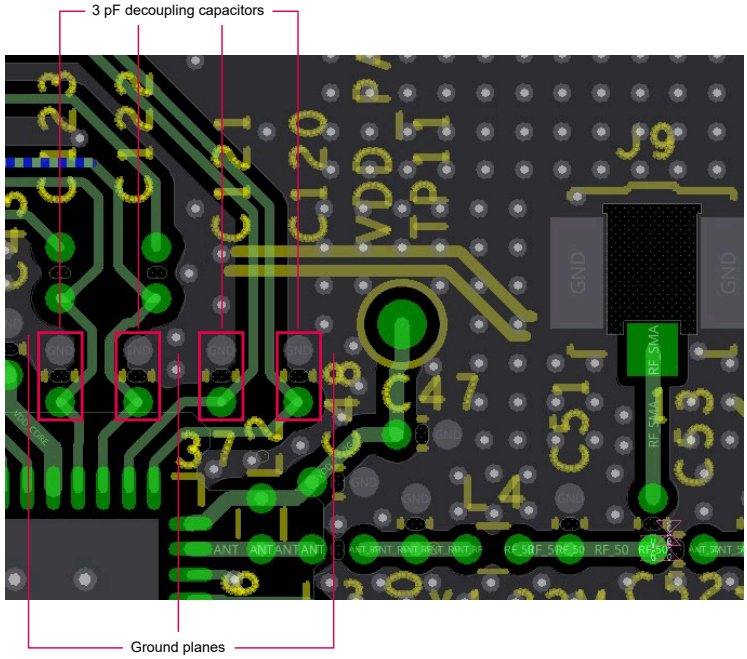

Figure 21. Recommended EMC layout

7.1.4 Radio layout recommendations

The following are some recommendations for creating an optimal radio layout:

- Place the pull-up inductor L2 as shown in the example layout of Figure 22.
- Place the C48 capacitor as near as possible to the L2 inductor.
- To isolate the VDD_RF line from the ANT_RF line, use the 12 pF capacitor C31 as a shorting capacitor. To ensure proper isolation, keep your radio layout exactly the same as in the example layout of Figure 22
- Also, isolate the VDD_RF line from the UART signals.
- Isolate the VDD_PA_2G4 line from the PTC0 pin.
- The 10 µF capacitor C32 on the VDD_RF line can be kept as DNP.
- The antenna-matching components must be placed near to each other and to the MCXW71 chip, as shown in Figure 22.

Note: *The power planes for VDD_ANA and VDD_SYS create huge fat nets. You should not reduce these power planes.*

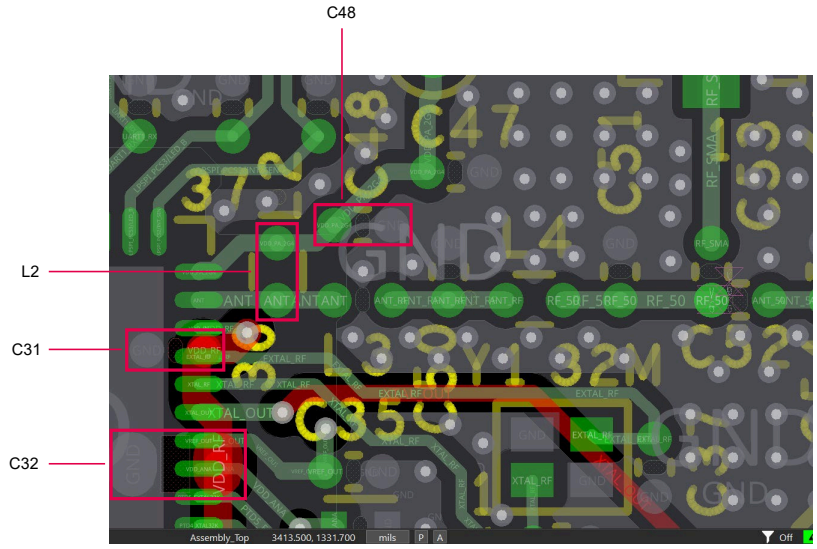

Figure 22. Radio layout

7.1.5 RF circuit layout recommendations

The transmission lines are of several shapes, for example, microstrip, coplanar waveguide, and stripline. For Bluetooth LE applications built on the FR4 substrate, the transmission lines typically take the form of a microstrip or coplanar waveguide (CPW). The two types of structures differ on the following parameters:

- Dielectric constant of the board material
- Trace width
- Board thickness between the trace and the ground

For CPW, the gap between the trace and the top edge ground plane defines the transmission line. These parameters are used to define the characteristic impedance of the transmission line (trace) that is used to transmit the RF energy between the radio and the antenna.

Figure 23 shows a recommended RF circuit layout for the MCXW71 MCU. The layout includes a single-ended RF output, along with a four-component RF matching network for the MCU. The four RF matching components (from left to right) are as follows:

- 1.5 nH series inductor L3
- 2.4 pF shunt capacitor C50
- 1.2 nH series inductor L4
- 1 pF shunt capacitor C51

The RF matching components transform the device impedance to 50 Ω. Depending on the board layout, the values of these components may vary.

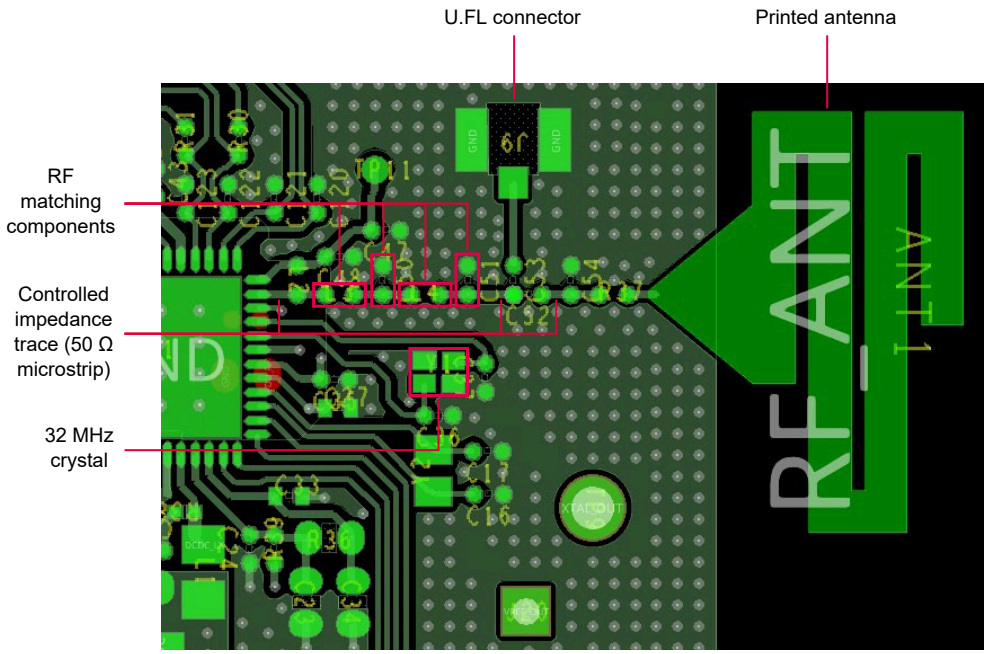

Figure 23. RF matching network

The following are some recommendations for creating an optimal RF circuit layout:

- Avoid routing traces near or parallel to the RF transmission lines or crystal signals. Maintaining a continuous ground under an RF trace is critical to maintaining the characteristic impedance of that trace. Avoid any routing on the ground layer that may result in disrupting the ground under the RF traces.
- Complexity is the main factor that determines whether an application board design includes two layers, four layers, or more layers. The recommended board stackups for two-layer and four-layer board designs are as follows:
  - Two-layer stackup:
    - Top: RF routing of transmission lines, signals, and ground
    - Bottom: RF reference ground, signal routing, and general ground
  - 4-layer stackup:
    - Top: RF routing of transmission lines
    - L2: RF reference ground
    - L3: DC power
    - Bottom: Signal routing

For more information on board stackup, refer to *Freescale IEEE 802.15.4 / ZigBee Package and Hardware Layout Considerations Reference Manual* (ZHDCRM).

7.2 Antenna recommendations

While choosing an antenna for a wireless system design, several types of antennas are available, for example:

- Small-footprint chip antenna
- Trace antenna
- Loop monopole
- Dipole

Each antenna type has its pros and cons. Choose a suitable antenna based on the intended goal of the application. In addition, follow a proven antenna implementation already followed in a hardware reference

design from NXP. For details on compact antenna designs, refer to *Compact Planar Antennas for 2.4 GHz Communication* (AN2731).

The following are some recommendations for creating an optimal antenna circuit layout:

- Copy critical dimensions exactly from an NXP reference board layout.
- The final dimensions of the customer board may differ from the dimensions of an NXP reference board. Therefore, make the last leg of the trace antenna long enough to allow final board tuning.
- To operate at the desired frequency, antenna tuning may be required. The minimum return loss must be centered at 2440 MHz. A 10 dB return loss looking into the antenna at the band edges is sufficient for good range and receive sensitivity.
- From the RF-matched port/pin to the antenna feed, maintain an antenna impedance of 50 Ω.
- The example board layout mentioned in this document uses microstrip topology; however, you can instead use a coplanar waveguide with ground. Remember that changing the topology also changes the board dimensions.
- The antenna must be placed away from metallic objects and must be oriented properly with the ground plane.
- Always check the antenna in its final environment, including the PCB, components, case enclosure, hand effects (if appropriate), and battery. Plastic and other materials in the near field may cause detuning.
- Actual antenna performance can be evaluated in various ways, such as:
  - Frequency range testing
  - Measuring the radiated signal level under controlled conditions
  - Characteristic testing in an anechoic chamber

8 References

The following are some additional documents that you can refer to for more information on the MCXW71 devices:

- MCXW71x Reference Manual (MCXW71RM)
- MCXW71 Product Family Data Sheet (MCXW71)
- FRDM-MCXW71 Board User Manual (UM12063)
- FRDM-MCXW71 board design files
- Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages (AN1902)
- Freescale IEEE 802.15.4 / ZigBee Package and Hardware Layout Considerations Reference Manual (ZHDCRM)
- Compact Planar Antennas for 2.4 GHz Communication (AN2731)

Note: *Some of these documents may only be available under a non-disclosure agreement (NDA). To access such a document, contact a local NXP field applications engineer (FAE) or sales representative.*

9 Acronyms

Table 1 lists the acronyms used in this document.

Table 1. Acronyms

Acronym	Description
CPW	Coplanar waveguide
DNP	Do not populate / do not place
EMC	Electromagnetic compatibility
HVQFN	Heat sink very-thin quad-flat pack no-lead

Table 1. Acronyms...*continued*

Acronym	Description
LE	Low Energy
PCB	Printed-circuit board
MCU	Microcontroller unit
QFN	Quad-flat pack no-lead
RF	Radio frequency
SON	Small outline no-lead
UART	Universal Asynchronous Receiver/Transmitter

10 Revision history

Table 2 summarizes the revisions to this document.

Table 2. Revision history

Document ID	Release date	Description
UG10146 v.1.0	10 September 2024	Initial public release

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