# Advanced modelling of distortion effects in bipolar transistors using the Mextram model

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## ABSTRACT

The modelling of distortion effects in bipolar transistors due to the onset of quasi saturation is considered. Computational results obtained using Mextram and Gummel Poon models as implemented in a harmonic balance simulator are compared with measured results.

## I. INTRODUCTION

The use of epitaxially grown layers in bipolar transistors is common practice since performance can be considerably improved with respect to breakdown voltage and power handling capability. The epilayer, while decreasing the base-collector depletion capacitance, will increase the base-collector transit time. This increase in base-collector transit time is one of the limiting factors for the maximum switching speed of this type of transistor (conventional transistors are normally limited by the base-emitter transit time). The use of a relatively lightly doped epitaxial layer also increases the internal resistance of the collector, limiting the power drive capability of the transistor.

In applications such as mobile telecommunication receivers and transmitters there are several constraints on the power consumption and the supply voltage. These will, in general, lead to a limit on the collector emitter voltage. It is clear that at higher current levels or at a relatively low collector emitter voltage, the voltage drop over the epilayer of the collector can lead to forward biasing of the internal junction. This effect is called quasi saturation (q.s.) and has been the subject of several publications [1,3,4]. Quasi saturation leads to current gain (β) and cut-off frequency ($f_T$) fall-off at higher current levels. Less well known to designers is the fact that the onset of q.s. also has a dominant influence on the distortion behaviour of the bipolar transistor [2]. In conventional transistor models the modelling of q.s. is limited to the voltage drop over the fixed internal collector resistance ($R_c$) which can lead to "unexpected" results when realized circuits are measured. Quasi saturation effects are of particular interest under high drive conditions as in power stages or mixers.

## I. THE MODELLING OF THE EPILAYER

In conventional transistor models such as Gummel Poon the voltage drop in the collector is modelled by a single ohmic resistor $R_c$ (see figure 1). In the Mextram model the voltage drop in the collector region is modelled by an ohmic resistor $R_{CC}$ and a voltage-controlled current source $I_{C1C2}$ (see figure 2). The controlled source is used to account for the voltage drop over the variable epilayer resistance which is modulated by the injected space charge in the collector region [1,3]. The extra voltage drop in the Mextram model

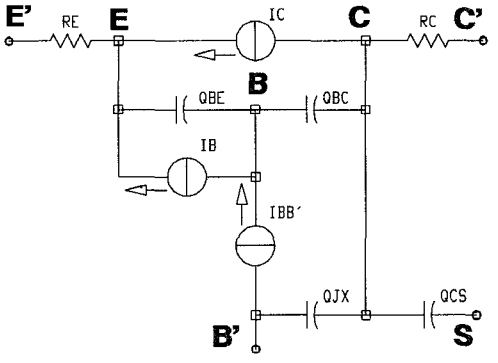


**Figure 1** The standard GP large signal model.

leads to earlier forward biasing of the internal base collector junction than in the Gummel Poon model. This is best illustrated by considering the simulation results obtained using the Gummel Poon and Mextram models for the same

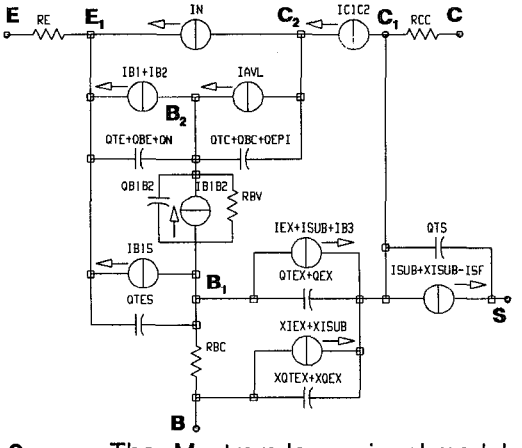


**Figure 2** The Mextram large signal model.

transistor. We have chosen the BFR520 transistor which is a standard Philips device commonly used in RF circuits. The $I_c(V_{ce})$ characteristic for the BFR520 transistor is compared with measurement data in figure 3. Study of the

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internal base collector junction voltage in the Mextram model leads to the conclusion that q.s. is significant over a larger area than is often assumed. In figure 3 lines representing a constant internal base collector voltage ≈ +0.7 V, are plotted for the GP and Mextram model. In the case of the GP model the internal junction is either not or insignificantly forward biased in most of the $I_c$ - $V_{ce}$ plane. In fact, when using the GP model, q.s. effects will often be modelled as an Early effect giving a reasonable fit for the $I_c(V_{ce})$ characteristic but failing to properly describe distortion behaviour at higher current levels or at low collector emitter voltages. This will be explained in section IV.

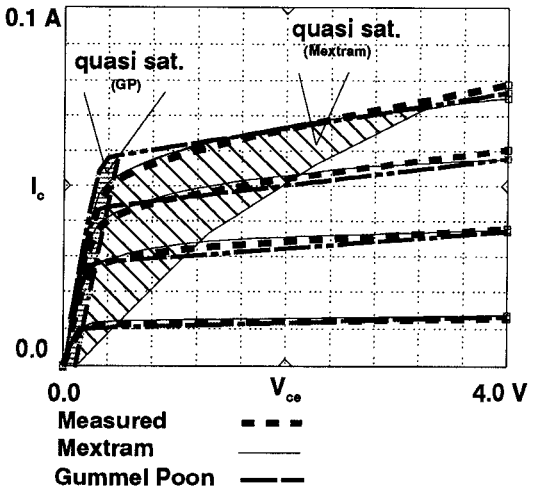


**Figure 3** $I_c(V_{ce})$ characteristic of the BFR520 transistor.

## III. LOW CURRENT DISTORTION EFFECTS

Distortion effects at low current levels in bipolar transistor are well understood [5,6,7]. At low frequencies there will be minima in the amplitude of the higher harmonics. These minima are caused by the nonlinearity of the emitter in combination with the input impedance $R_{in}$. This phenomenon has been the subject of several papers [e.g. 7] and can be used to cancel out one of the higher harmonics for a given bias point. Conventional transistor models like Gummel Poon [6] as well as the Mextram model can model most of the distortion effects for moderate driving conditions.

## IV. HIGH CURRENT DISTORTION EFFECTS

At high current levels or at lower collector emitter voltages q.s. will set in at a certain point for a given device. The onset of q.s. will lead to an increase in the third order distortion component [2].

Distortion increase due to q.s.

This increase in distortion is caused by the internal base collector junction becoming forward biased. When this happens the injection of minority carriers in the epilayer (related to the built-in base collector junction voltage) will lead to a strong reduction of the epilayer resistance and the build up of storage charge. This strong reduction of the epilayer resistance combined with the increase of the reverse component of the main current will lead to a significant change in the small signal transfer of the device under consideration. The distortion behaviour of the device under test may be approximated by studying the small signal transfer of the circuit in figure 4. This is due to the fact that at sufficiently low frequencies (ignoring reactive elements) the higher harmonics at the output of the transistor will be related to the input voltage by a Taylor series [8]. Consequently, the distortion behaviour of a device can be studied at low frequencies and low driving conditions by investigating the derivatives of the AC transfer characteristics with respect to the input voltage $V_{b2e1}$.

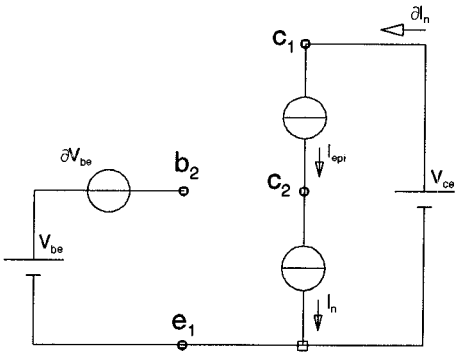


**Figure 4** Simplified circuit model of a bipolar transistor with a lightly doped epilayer.

The small signal definitions of the epilayer current and the main current in the Mextram implementation are:

$$dI_n = g_x . \partial V_{b2e1} + g_y . \partial V_{b2c2}$$

$$dI_{epi} = grcvy . \partial V_{b2c2} + grcvz . \partial V_{b2c1}$$

where:

$$gx = \frac{\partial I_n}{\partial V_{b2e1}},\ gy = \frac{\partial I_n}{\partial V_{b2c2}},\ grcvy = \frac{\partial I_{epi}}{\partial V_{b2c2}},\ grcvz = \frac{\partial I_{epi}}{\partial V_{b2c1}}$$

Since the output of the circuit is AC-shorted: $\partial V_{b2c1} = \partial V_{b2e1}$ and with the given network topology: $dI_n = dI_{epi}$. Making use of these conditions we can solve for the small-signal transconductance $\partial I_n / \partial V_{b2e1}$, leading to:

$$\frac{\partial I_n}{\partial V_{b2e1}} = gx + gy . \left[\frac{grcvz - gx}{gy - grcvy}\right] \qquad (1)$$

Plotting equation (1) as a function of the collector current we can get a clear picture of the influence of the epilayer parameters on the distortion behaviour.

no saturation In this situation the main current is given by: $I_n = I_f = I_s.\exp(V_{b2e1}/V_t)$, gx = $I_f$ / $V_t$ (linear with the collector current) and gy = 0.

quasi saturation ($V_{b2c2} > 0$) In this situation the main current is given by: $I_n = I_f - I_r = I_s.(\exp(V_{b2e1}/V_t) - \exp(V_{b2c2}/V_t))$, gx = $I_f$ / $V_t$ (grows faster than the collector current) and gy = -$I_r$/$V_t$ (negative, decreasing faster than the collector

current), because: $gx+gy = I_c/V_t$.

Considering equation (1) we note that $\partial I_n / \partial V_{b2e1}$ in q.s. is nonlinearly dependent on the collector current when the multiplication term related to gy is not equal to one. In practice this will always be the case. This change in dependency of $\partial I_n$ with respect to the collector current and thus also with respect to $V_{b2e1}$, will lead to an increase in the value of the derivatives of the small signal transfer as the transistor goes into q.s. This causes an increase in the higher order harmonics.

The influence of the parameters VDC and RCV

For simplicity we will use the Kull model [4] for our epilayer description and neglect hot carrier effects. In this case $I_{epi}$ is only affected by two parameters, namely RCV (the epilayer resistance) and VDC (the built-in base collector junction voltage). Due to the nature of the epilayer model, RCV will (only) influence the value of the collector current at which the internal junction becomes forward biased for a given external base collector voltage, but not the shape of $\partial I_n/\partial V_{b2e1}$ (see figure 5) In contrast, the internal junction voltage VDC hardly affects the timing when the transistor enters q.s. but does affect the junction knee voltage at which the epilayer resistance really starts to shrink. This is of major importance for the increase in distortion when the device enters the q.s. region. In summary, we note that a device with a high built-in junction voltage will result in more distortion when it enters q.s. than a similar device with a lower built-in voltage. This is illustrated in figure 6 which is based on the Kull model for the circuit of figure 4.

## V. SIMULATIONS AND MEASUREMENTS

The calculated data for the BFR520 has been obtained using our Mextram implementation in Hewlett Packard's harmonic balance simulator MDS. This has proven to be a particularly valuable tool during the project. When comparing Mextram to Gummel Poon simulations we can see that the third order distortion maximum is manifest when approaching the $V_{b2c2} \approx 0.7$ V lines of figure 3. Since in the case of Gummel Poon this line is reached much later, bipolar transistor distortion at higher current levels is improperly modelled (see figure 7). In this figure the amplitude of the fundamental frequency (10 MHz) as well as the second and third order distortion components of the collector voltage are plotted as a function of $I_c$ for $V_{bc}$ = 0,-1 and -3 V. (The collector voltage is directly related to the collector current via a 50 ohm load resistor).

When considering RF power conditions these phenomena, although less pronounced, will give differences in simulation results for the Gummel Poon and Mextram models as demonstrated in [9].

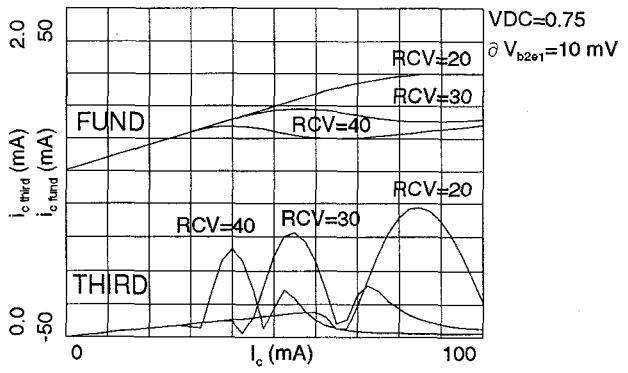


**Figure 5** The influence of RCV on the fundamental frequency and third harmonic of $\partial I_n$.

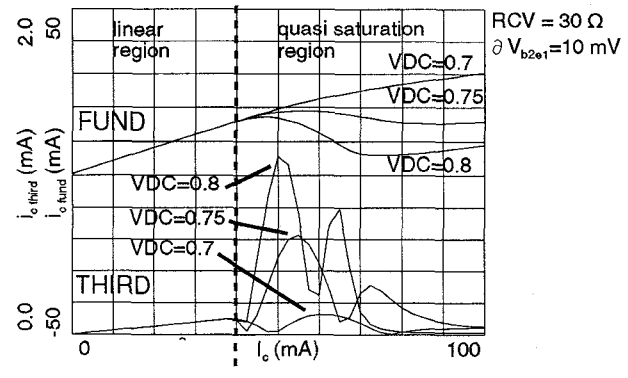


**Figure 6** The influence of VDC on the fundamental frequency and the third harmonic when a transistor enters quasi saturation.

During the measurements, power consumption of the DUT causes self heating which is of major influence on the results obtained. To minimize these effects pulsed bias voltages should be applied. Even when using pulsed bias voltages the DUT will generally heat-up within 0.1 ms leading to an increase in the collector current. To avoid corruption of the distortion data the RF measurement should be short in time and take place at exactly the same moment when the bias current Ic is measured.

At lower current levels distortion measurements can be carried out using a spectrum analyzer (SPA). At higher current levels self heating of the device under test (DUT) will give temperature related errors due to the minimum sweep time (e.g. 20 ms) allowed by the instrument. In principle, faster measurements should be possible by setting the SPA to a bandwidth span of zero and locking the signal source to the SPA. In practice, SPA firmware related problems make it impossible to achieve the desired measurement time (e.g. 0.1 ms).

Distortion measurements can be carried out using a 100 MHz 500 Ms / sec data acquisition scope to maintain the phase information. An illustration of this measurement setup is given in figure 8. The network analyzer is used as a 10 MHz signal source. At a constant $V_{ce}$, the $V_{be}$ of the transistor will be pulsed for 1 ms, after 50 µs the amplified signal will be stable at the output of the DUT and the

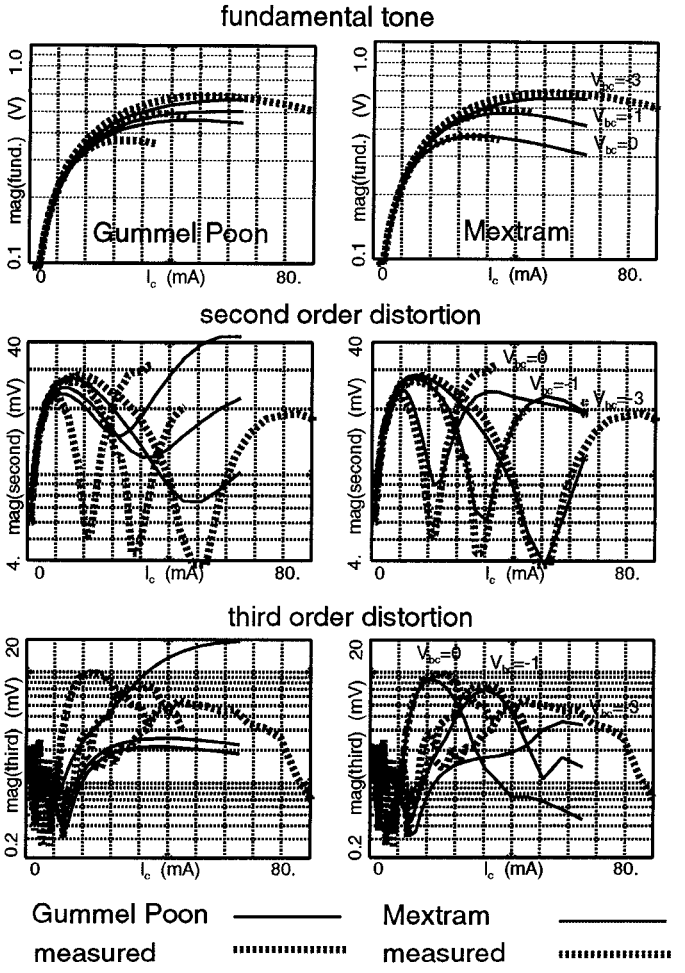


**Figure 7** Simulated and measured distortion components in the collector voltage of the BFR520 at a driving input voltage of 7 mV.

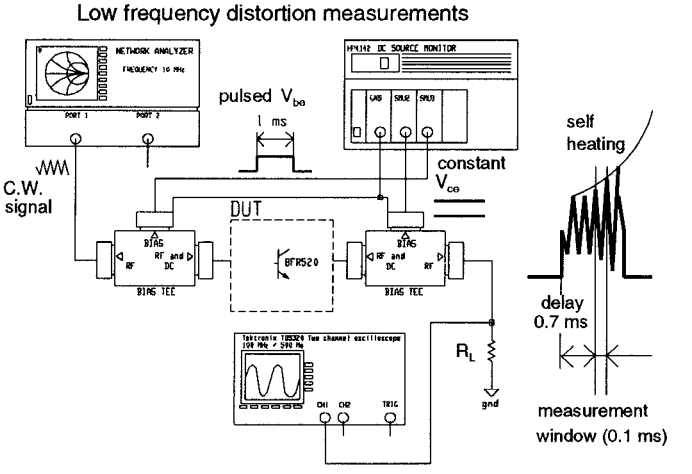


**Figure 8** Low frequency distortion measurement setup using a 100 MHz / 500 Ms oscilloscope.

sample scope will be triggered. After a delay of approximately 0.7 ms the DC collector current as well as the AC voltage over the 50 ohm load resistance during a time span of 0.1 ms are measured and read by HP's data acquisition program VEETEST. For each bias point a trace of the load resistance voltage is taken and a Fast Fourier transformation (FFT) is performed to find the proper distortion components. Due to the fact that a large number of periods are measured the FFT will work like an averaging filter, leading to good accuracy. For the higher frequencies a mixer is used to down-convert the desired HF components to an IF frequency within the bandwidth of the sampling scope.

## VI. CONCLUSIONS

Incorporation of the latest developments in the formulation of epilayer behaviour in Mextram, has provided the first compact transistor model capable of accurately describing the distortion behaviour of a transistor when operation extends into the region of quasi saturation. Implementation of Mextram in the simulator package MDS has resulted in a very powerful combination facilitating the use of harmonic balance techniques in strongly non-linear circuit design.

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