Semiconductors

BLF6G20-45

BLF6G20-45 LDMOS Transistor Model

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Document information

Info	Content
Keywords	BLF6G20-45, LDMOS, model
Abstract	This document describes the BLF6G20-45 LDMOS transistor model including its installation, usage, verification and application circuit.

PHILIPS

Revision history

Rev	D	Description
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1. Introduction

The purpose of this document is to provide the customer with a comprehensive description of the BLF6G20-45 LDMOS transistor model, extraction procedure, installation procedure, verification, limitations and application.

The BLF6G20-45 is a 45W RF power transistor in a SOT 608 package (see Fig 1). The device has been optimized for WCDMA base station applications in the 1805-1880 MHz frequency band. For more information about the device performance, see the Data Sheet.

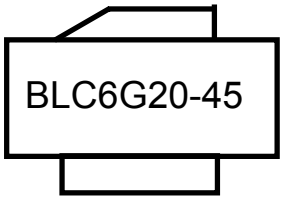

Fig 1. Drawing of the BLC6G20-45 device.

2. Model Description

Table 1 summarizes the model information.

Table 1. Summary of model information

Device name	BLF6G20-45
Model name	PHI_BLF6G20-45V1p0_PHI_BLF6G20_45
Model version	1.0
Simulator	ADS 2004A, ADS 2005A
Library version	SiMKit 2.2.03

The electrical behavior of the transistor die is described by a scalable, physics based Sub-Circuit model[1]. This model is based on the Philips standard models MM11 for the channel region and MM31 for the drain extended region. MM11 is a surface potential based MOST model providing a smooth transfer from sub- to super threshold including the sign swap of the temperature coefficient of the drain current. This improves inter-modulation distortion modeling. In addition, parasitic resistances and capacitances have been included to model the interconnect lines on the die. The model scales with the

1. See: M.P.J.G. Versleijen, V.J. Bloem, J.A. van Steenwijk, O.I. Yanson, "*A new physics based dynamic electro thermal large signal model for RF LDMOS FETs*", IEEE MTT-S 2004 International Microwave Symposium Digest, Volume 1, pgg. 39 – 42.

number of cells and the length of the gate fingers. Temperature scaling of the model is a static one and is based on the standard temperature scaling rules of the building blocks (MM11, MM31).

At present, lumped element components are used to model the matching capacitors, package parasitic capacitance and bond-wire inductances.

3. Model Parameters

The ADS symbol for the BLF6G20-45 device is shown in Fig 2.

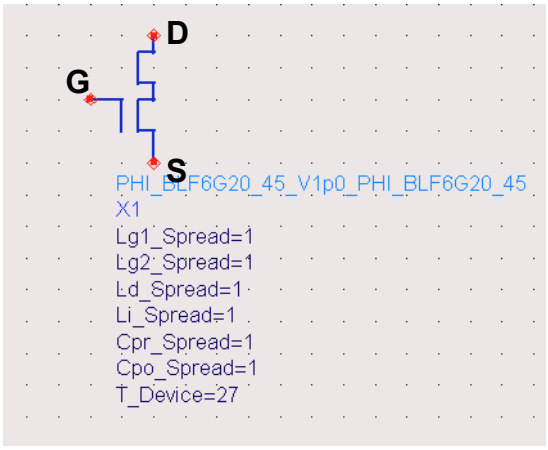

Fig 2. ADS symbol of the BLF6G20-45 device.

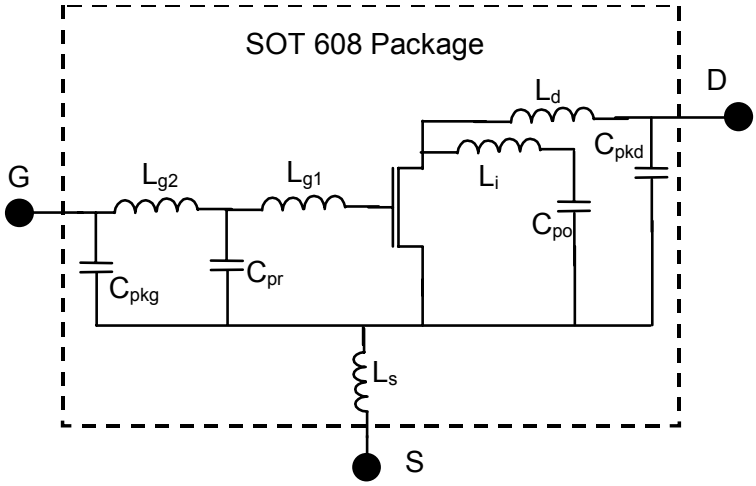

Fig 3. Schematic of the package model as in Fig 2.

The parameters L_{g1}_Spread, L_{g2}_Spread, etc. allow controlling the spread of the values of the bond-wire inductances and matching capacitances. In practice, the parameters set the ratio between the actual and nominal values of each element[2]. By default, these parameters are set to 1.

The expected statistical distributions of the spreading of the bond-wire inductances and matching capacitances can be provided by Philips on special request.

The T_Device parameter controls the device temperature used in the simulation.

2. For instance, by setting L_{g1}_Spread to 0.95, the actual value of the L_{g1} inductance becomes 95% its nominal value.

4. Parameter extraction procedure

The model parameters of the BLF6G20-45 were extracted with the following procedure:

i. Extraction of the parameters of the active die model
   a. The DC characteristics were measured in wide bias and temperature ranges (V_{gs} up to 15V, V_{ds} up to 30V, T up to 125 °C).
   b. The s-parameter were measured in a wide frequency band
   c. Dedicated structures were used for the de-embedding of the parasitics due to metal structures and interconnects from the s-parameter data.
   d. A semi-automated procedure implemented with the Agilent's IC-CAP program was used to extract the model parameters

ii. Extraction of the parameters of the package model
   a. The values of the matching capacitances were obtained from design information
   b. The value of the package parasitic capacitance was measured with a low-frequency CV meter
   c. The starting values of the bond-wire inductances were obtained from design information.
   d. The device S-parameters were measured using both an unmatched test fixture[3] and the application circuit.
   e. The inductance values were then optimized by fitting the S-parameters data. The package parasitic source inductance was also optimized.

5. Model limitations

The current version of the model includes only *"static"* thermal effects. This means that only the simulation temperature can be specified. As a consequence, it is expected that the model will provide a slight overestimation of the P_{1dB} and P_{3dB} values. The amount of this overestimation depends on the specific simulation conditions. However, it is expected not to exceed 1 dB.

Another consequence of the absence of electro-thermal effects is that the applied bias voltage (V_{gs}) needed to obtain the required I_{dq} is expected to be 0.1V-0.2V higher in simulations than in measurements.

The absence of dynamic thermal effects also implies that the model is at present not capable to take in to account thermal memory effects.

In addition, since the model is based on a quasi-static formulation, it does not predict memory effects due to non-quasi-static (NQS) phenomena.

3. This test fixture is composed by a simple 50Ω transmission line and, therefore, provides 50Ω loadings at the input and output of the device.

Some of these limitations will be overcome in the near future when a new, fully electro-thermal, version of the model (at present under testing) will be made available.

6. Installation Instructions

In order to run properly, the Design Kit requires the latest version of the Philips model library SiMKit to be installed (see Table 1 for version information). The SiMKit model library provides the definitions of the primitive submodels employed by the main device model. The installation procedure is described for three possible cases.

6.1 Case 1: No SiMKit installed

i. Close all ADS schematics
ii. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
iii. Install the Philips SiMKit
iv. Exit and restart ADS
v. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
vi. Install the model Design Kit
vii. Exit and restart ADS
viii. Now the model will function properly

6.2 Case 2: Old version of the SiMKit installed

i. Close all schematics
ii. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
iii. REMOVE the older version of the SiMKit (DO NOT just DISABLE the old SiMKit)
iv. Apply the changes
v. Exit and restart ADS
vi. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
vii. Install the Philips SiMKit
viii. Exit and restart ADS
ix. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
x. Install the model Design Kit
xi. Exit and restart ADS
xii. Now the model will function properly

6.3 Case 3: Updated version of the SiMKit installed

i. Close all schematics
ii. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
iii. Install the Design Kit of the model
iv. Exit and restart ADS
v. Now the model will function properly

NOTE: failing to have the proper version of the Philips SiMKit installed will result in an error message during the simulations.

7. Application circuit model

The layout drawing of the modeled application circuit is shown in Fig 4. The properties of the layers are shown in Table 2. The ADS equivalent circuits for the input and output sections are shown in and, respectively.

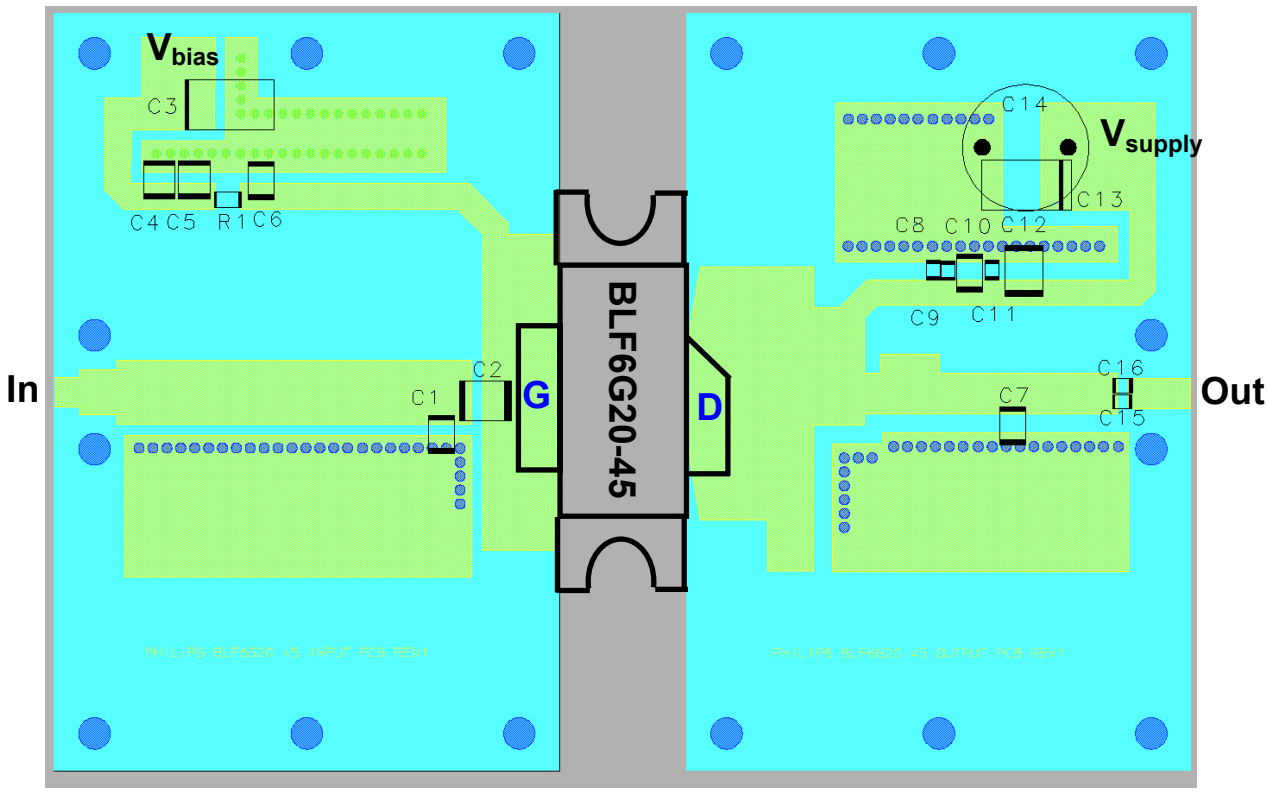

Fig 4. Layout of the application circuit of the BLF6G20-45 device.

Table 2. Characteristics of the layers of the application circuit board

Layer	Material	Thickness
Substrate	Rodgers (ε_r = 2.2)	0.79 mm
Conductor	Copper	35 μm

The values of the components in Fig 4 are listed in the tables below.

Table 3. Resistances

Component	Value
R_1	5.6 Ω

Table 4. Capacitances

Component	Type	Value
C_1	ATC 100B	2.0 pF
C_2	ATC 100B	2.7 pF
C_3	AVX Tantalum	10 μF
C_4	TDK Ceramic	1.5 μF
C_5	TDK Ceramic	1.5 μF
C_6	ATC 100B	10 pF
C_7	ATC 100B	1.2 pF
C_8	Murata	100 nF
C_9	Murata	100 nF
C_{10}	ATC 100B	10 pF
C_{11}	AVX Ceramic	220 nF
C_{12}	TDK Ceramic	4.7 μF
C_{13}	AVX Tantalum	10 μF
C_{14}	Philips electrolytic	220 μF, 63V
C_{15}	ATC 100A	6.8 pF
C_{16}	ATC 100A	6.8 pF

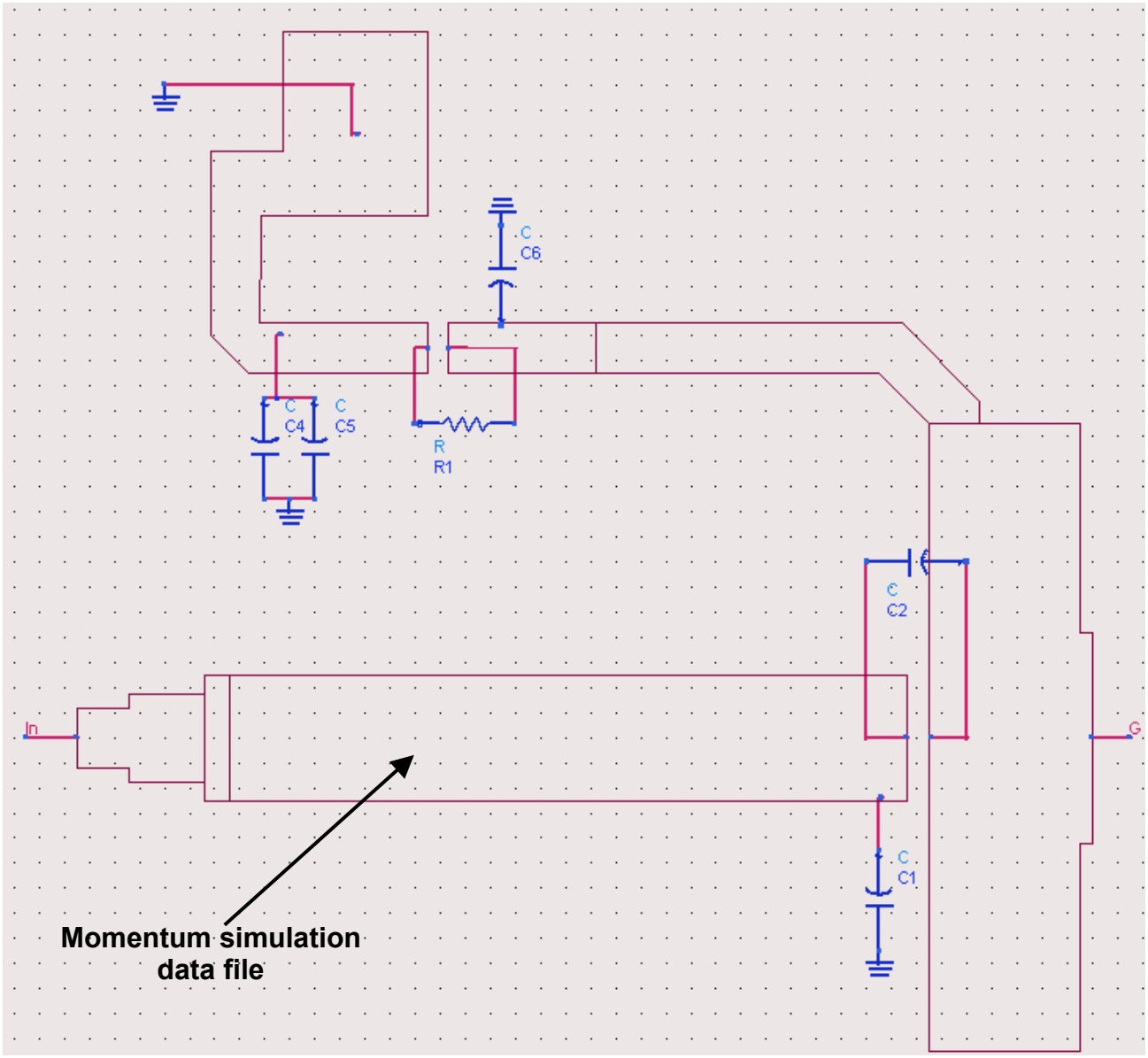

Fig 5. Simplified ADS schematic of the input circuit of Fig 4. Note that bias pad has been grounded. As a consequence, the biasing is applied though a separate DC-feed component (see the Simulation Template for more details).

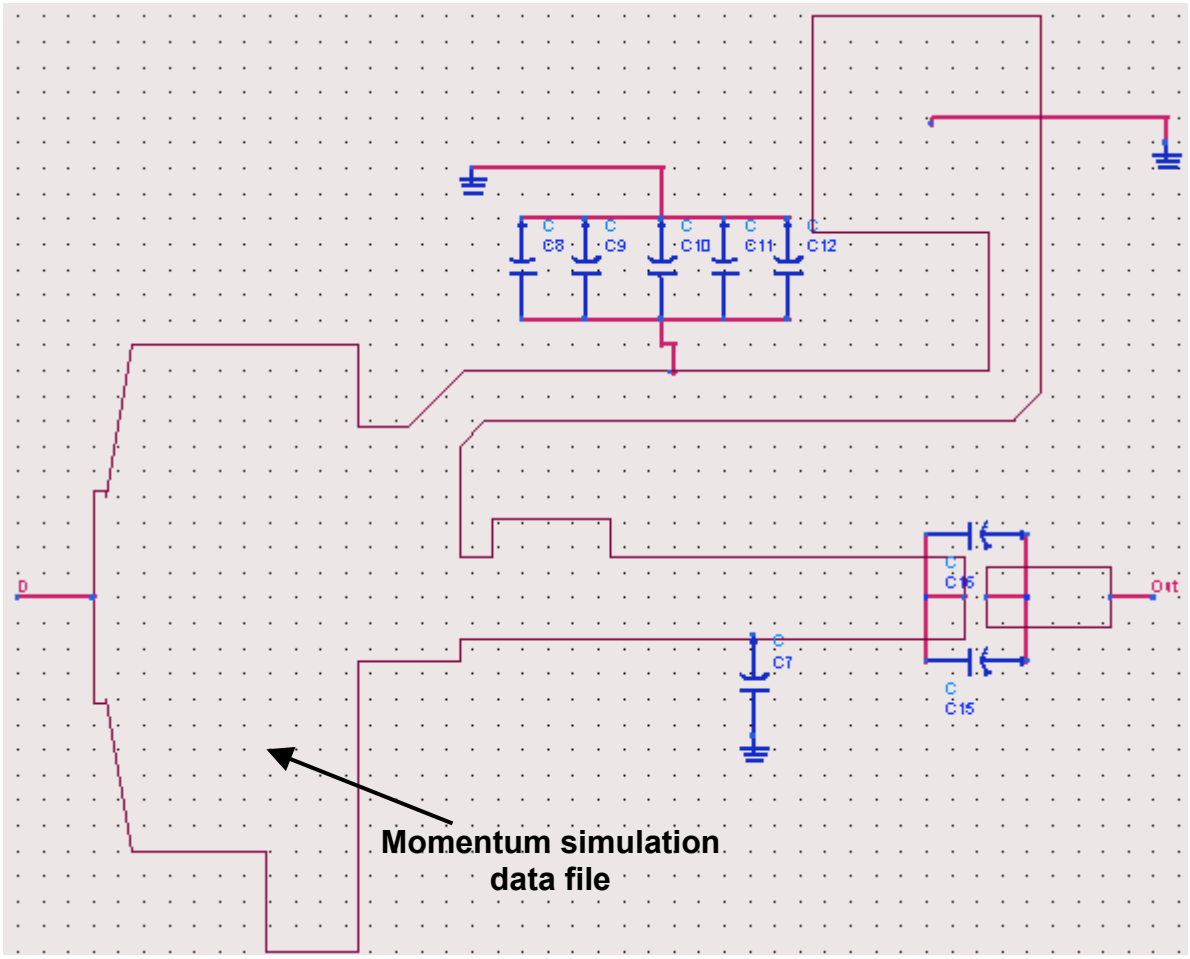

Fig 6. Simplified ADS schematic of the output circuit of Fig 4. Note that bias pad has been grounded. As a consequence, the biasing is applied though a separate DC-feed component (see the Simulation Template for more details).

8. Model Verification

8.1 DC Verification

At present, no DC verification data is available.

8.2 Small-signal verification

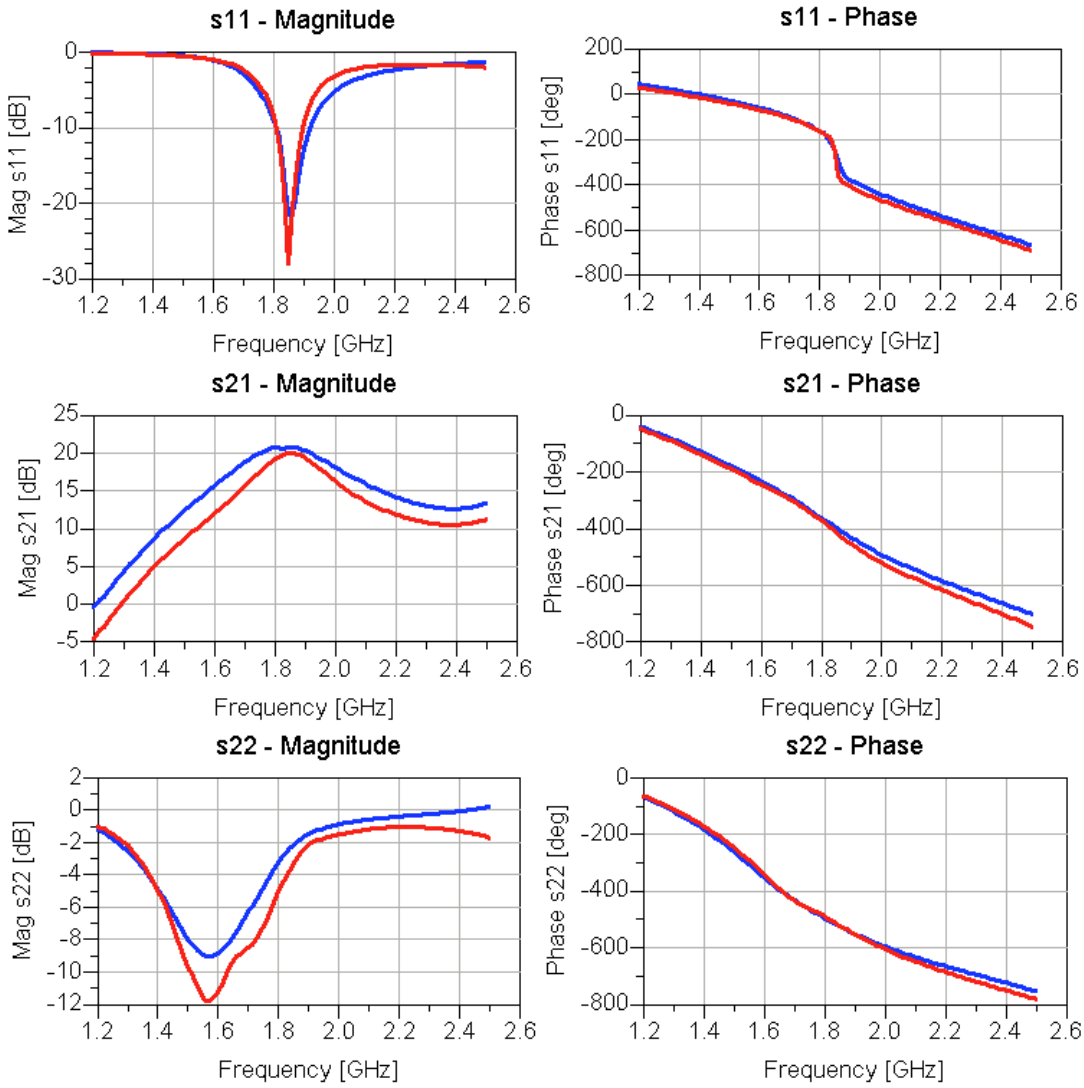

Fig 7. Measured (red lines) and simulated (blue lines) magnitudes and phases of the s_{11}, s_{21} and s_{22} parameters of the BLF6G20-45 LDMOS device.

The conditions for the above graphs are: I_{dq}=405mA, V_{ds}=28V.

8.3 One Tone Verification

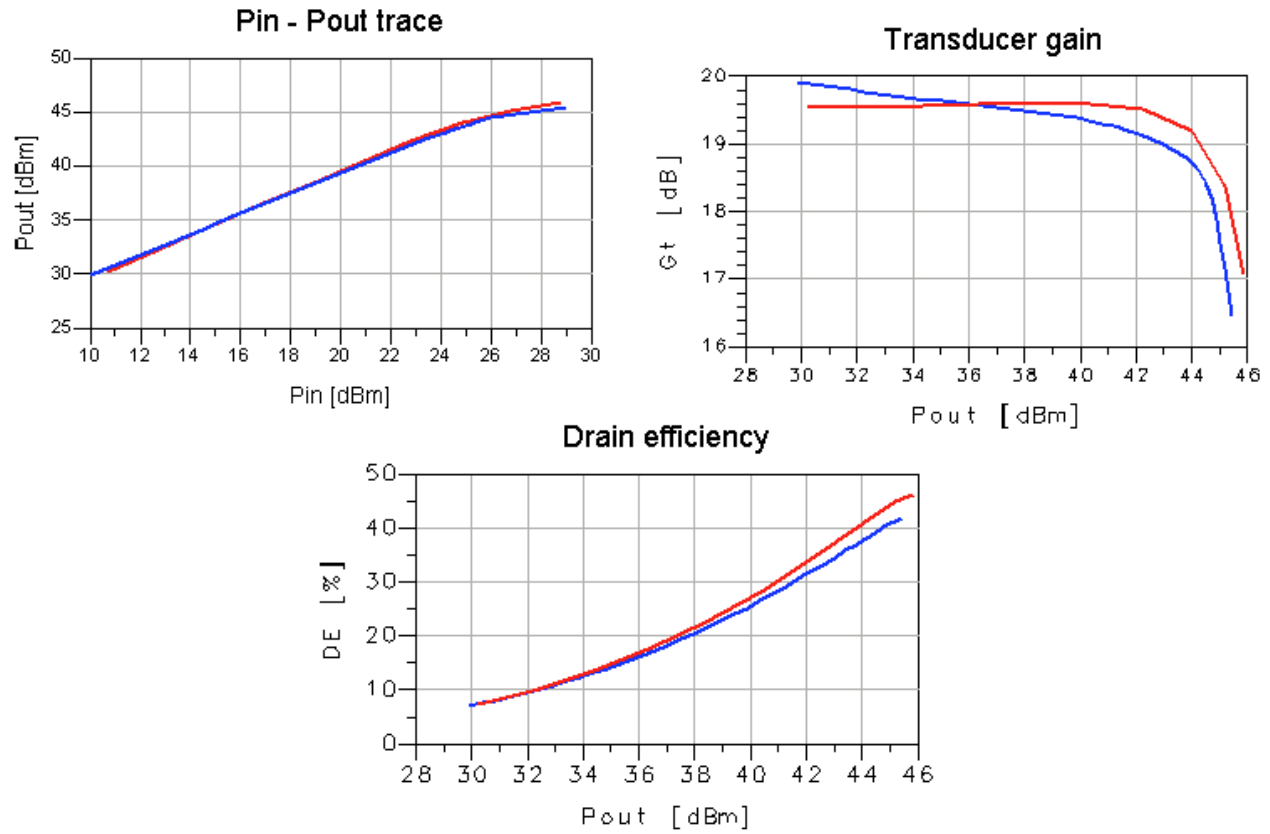

Fig 8. Measured (red lines) and simulated (blue lines) 1-tone large-signal performance of the BLF6G20-45 LDMOS device.

The conditions for the above graphs are: I_{dq}=350mA, V_{ds}=28V, f=1.880 GHz.

8.4 Two Tone Verification

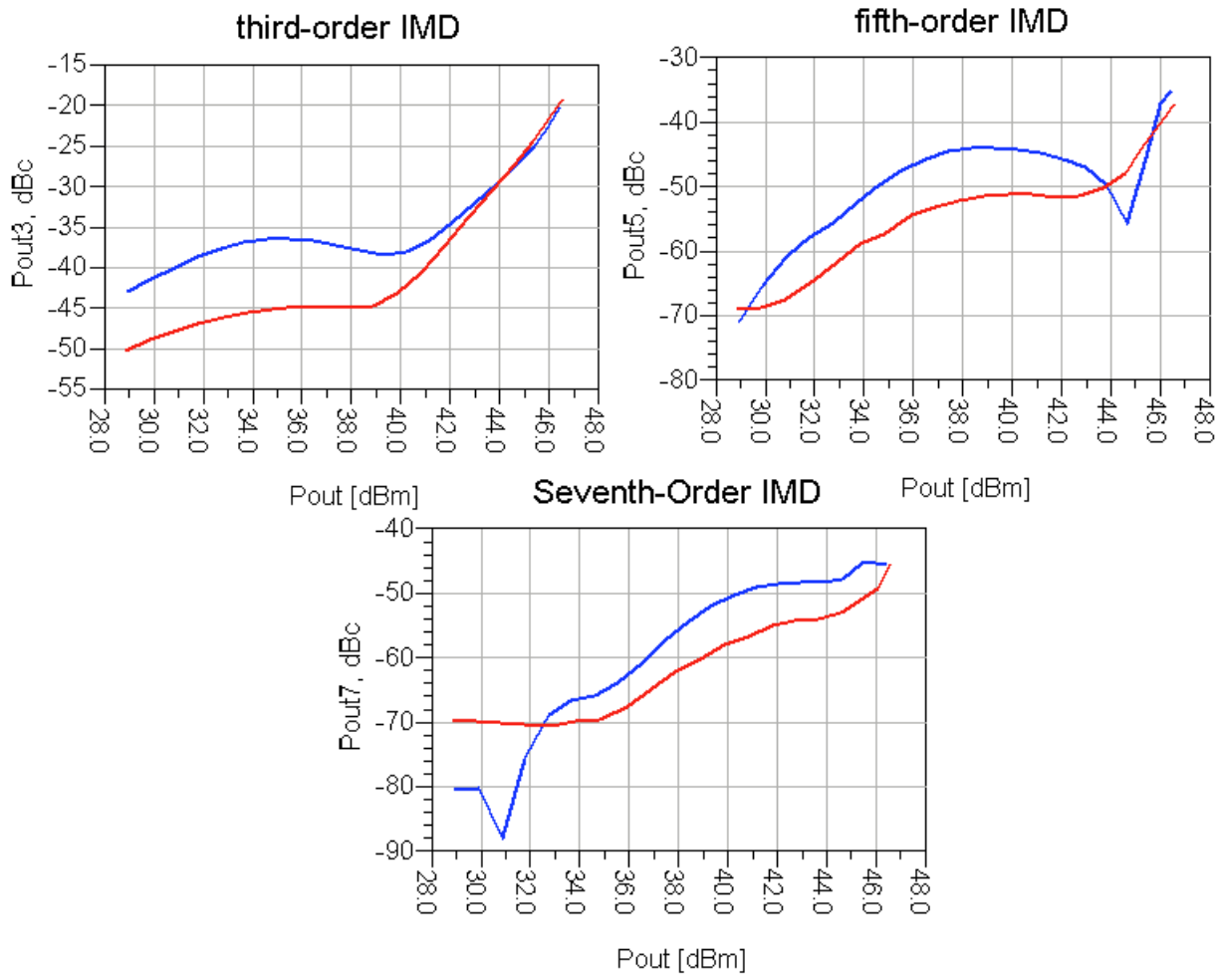

Fig 9. Measured (red lines) and simulated (blue lines) 2-tone large-signal performance of the BLF6G20-45 LDMOS device.

The conditions for the above graphs are: I_{dq}=400mA, V_{ds}=28V, f=1.880GHz, Δf=100kHz.

Summary of the model performance:

- In-band input return loss well predicted
- Gain well-predicted
- Peak power and PAE well predicted
- Trend of IMD3 predicted

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