FTF | FREESCALE TECHNOLOGY FORUM
POWERING INNOVATION

BSC913x IPC Architecture

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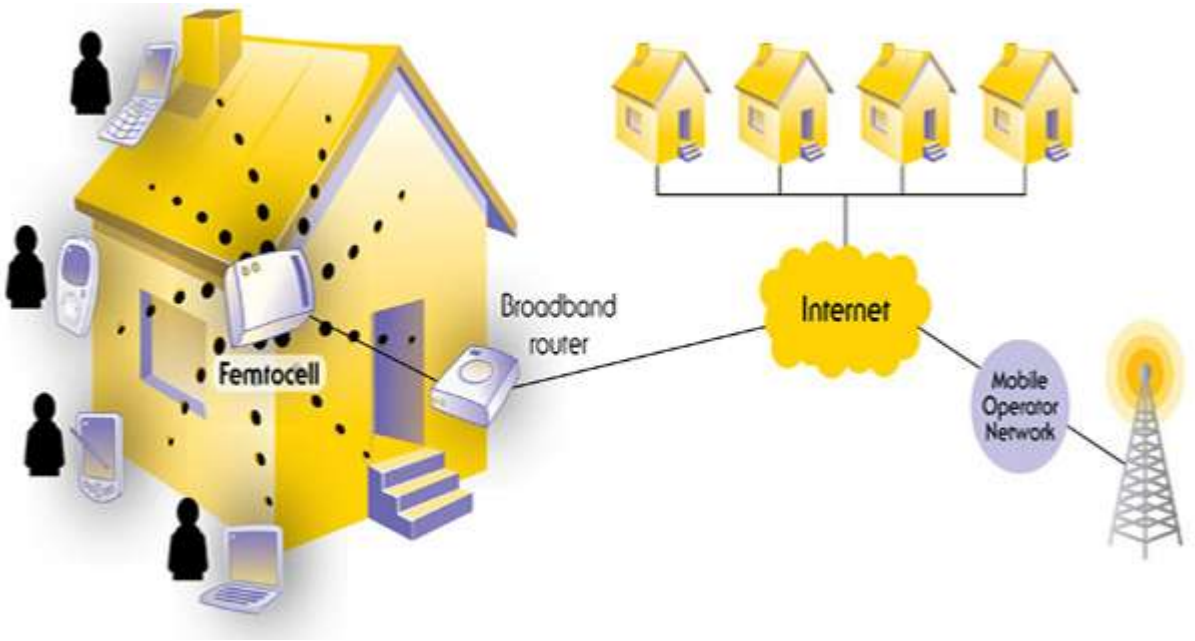
Agenda

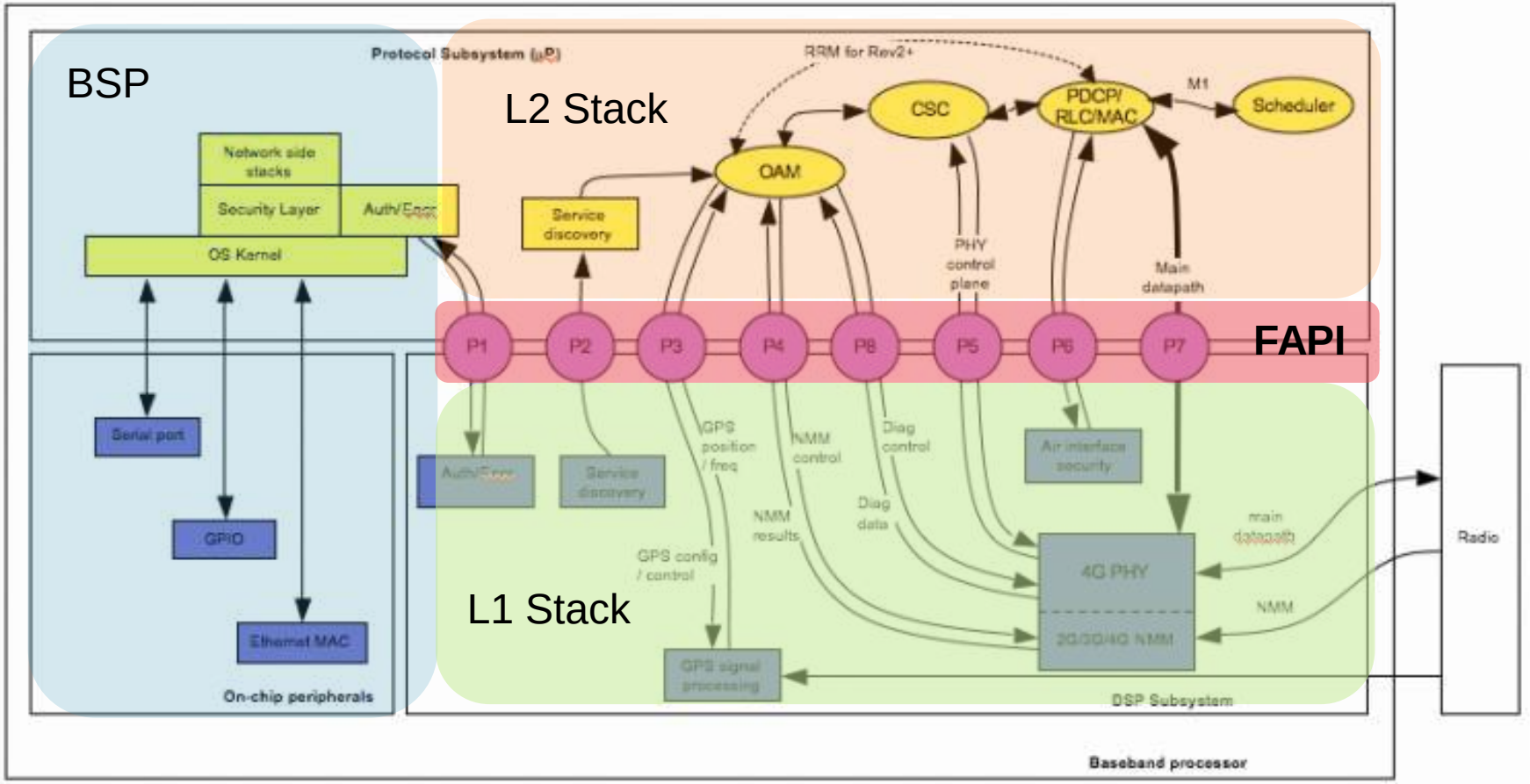
- Small-Cell Internals
- Small Cell based on BSC9131
- BSC913x Software Architecture
- IPC Architecture
- FAPI Messages to IPC Channel binding
- Use Cases
- Q&A

Small Cell

- Small Cell = Home or small office cellular base stations supporting the following standards:
- LTE-FDD/TDD
- WCDMA (HSPA+)
- CDMA2K
- TD-SCDMA



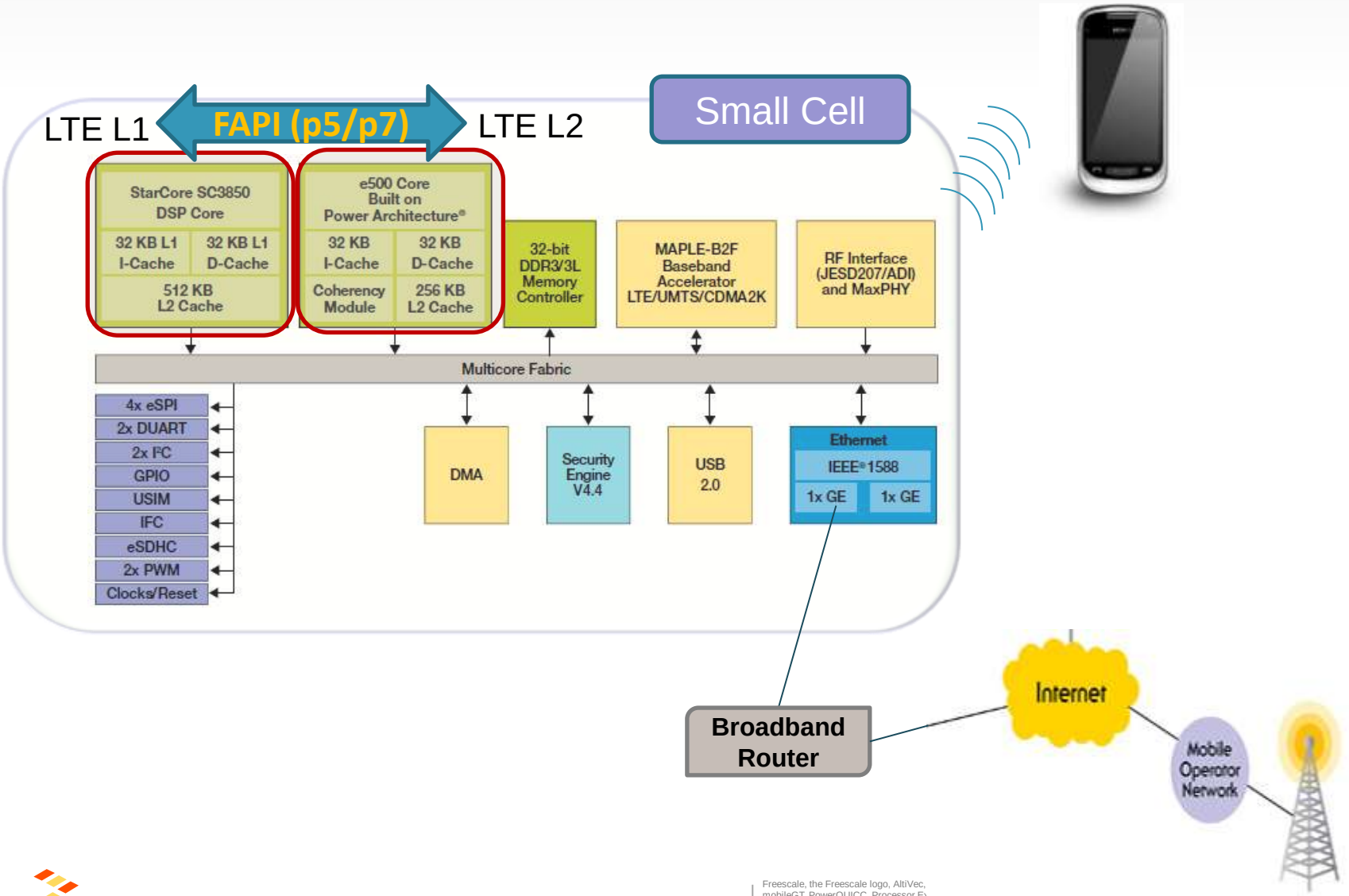
Software Components in a Small Cell



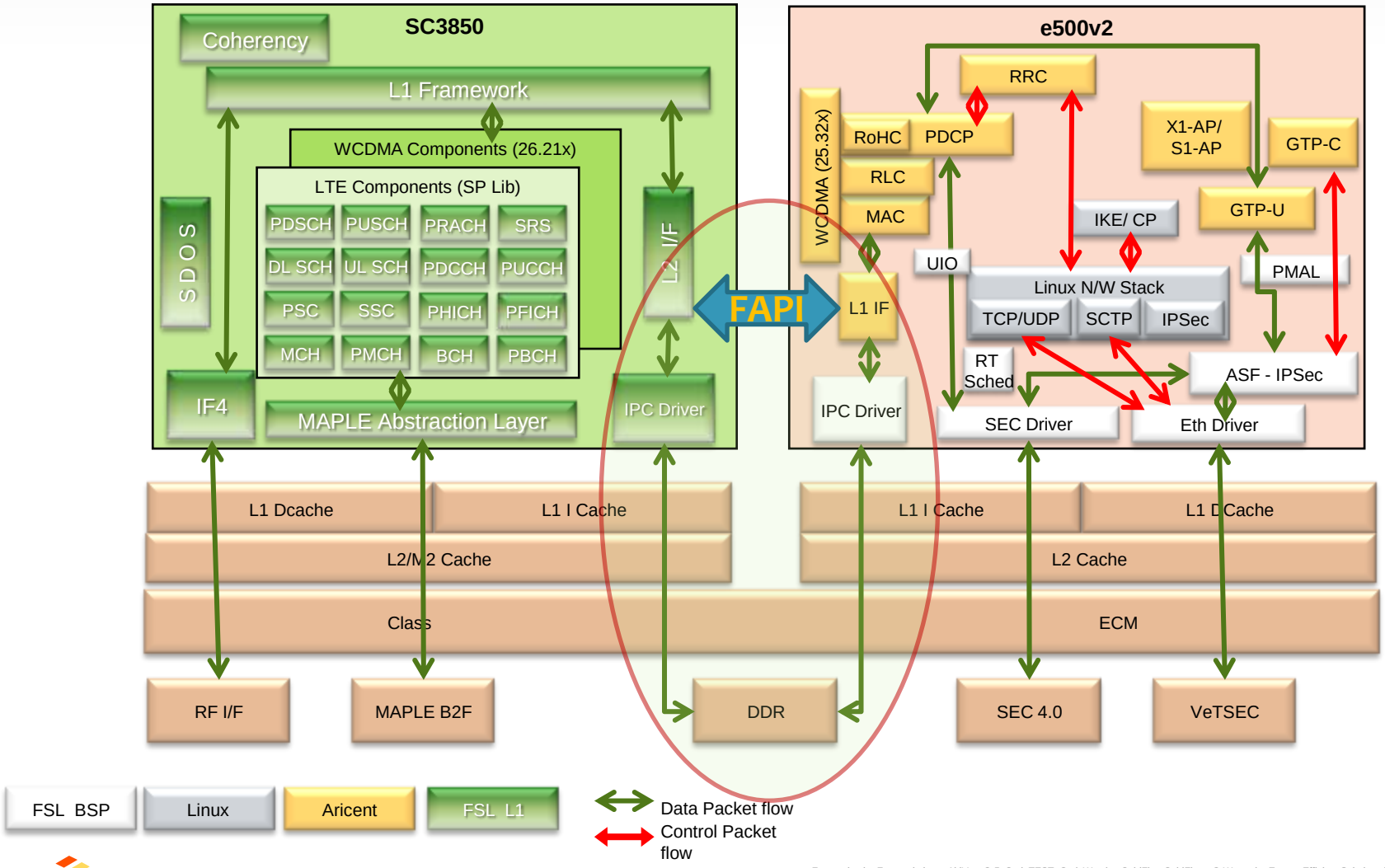
FAPI :

- Small Cell Forum Femto Application Programming Interface

Internals of a Freescale-Powered Small Cell



Femto/Pico-Cell (913x) System Architecture

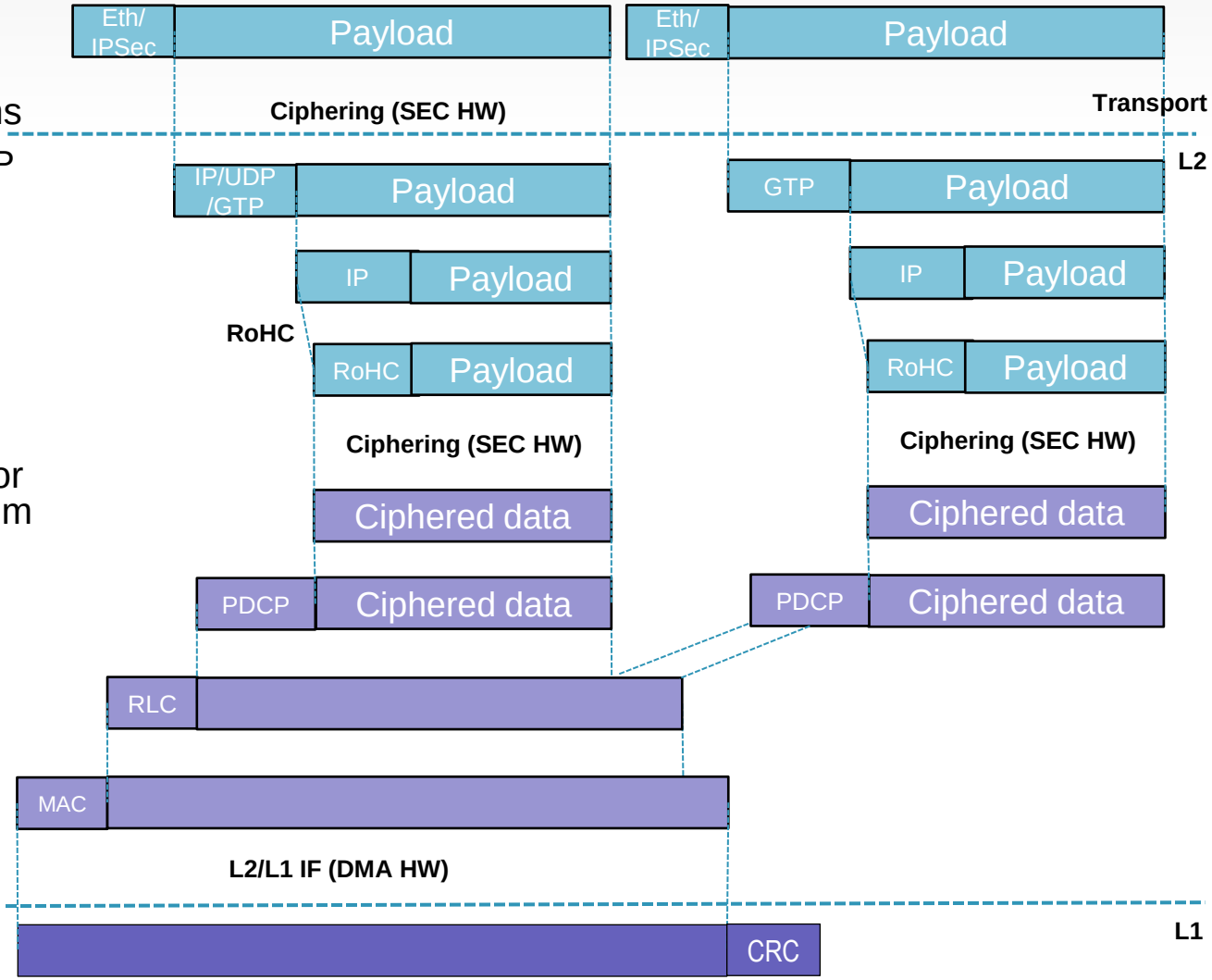


IPC Design Highlights

- Shared Library
- Provides Zero Copy
- Lock Free, No synchronization required
- Independent Unidirectional Channels
  - Single Producer – Single Consumer
- Multicore Ready

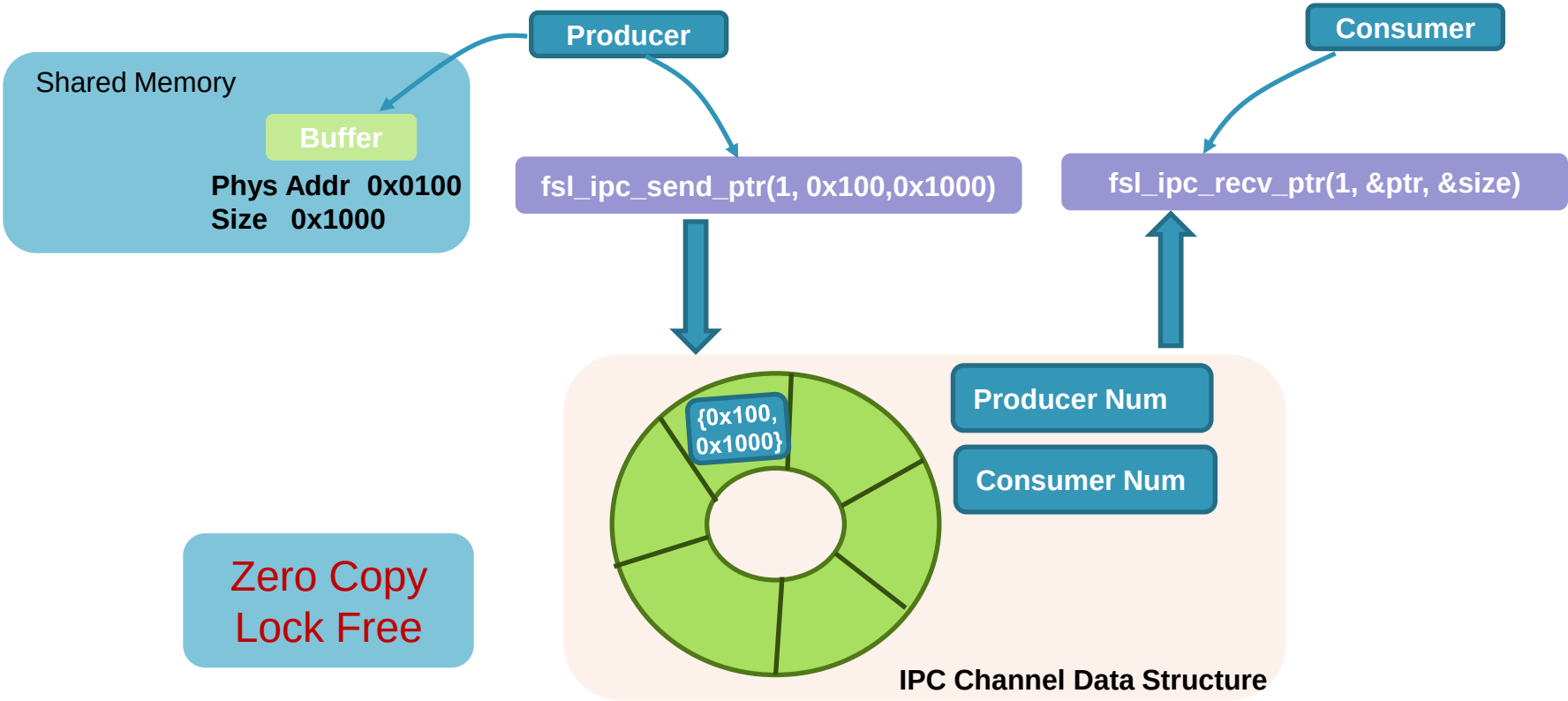
Achieving zero-copy operation

- Mutliple buffer domains
  - Transport, GTP/PDCP
  - L2
  - L1
- zero-copy operation through use of SEC engine between domains
- Custom buffer pools for all domains for optimum performance
- Optimized implementation of virtual ↔ physical address translation APIs as required for HW accelerator interfacing
- Asynchronous buffer return



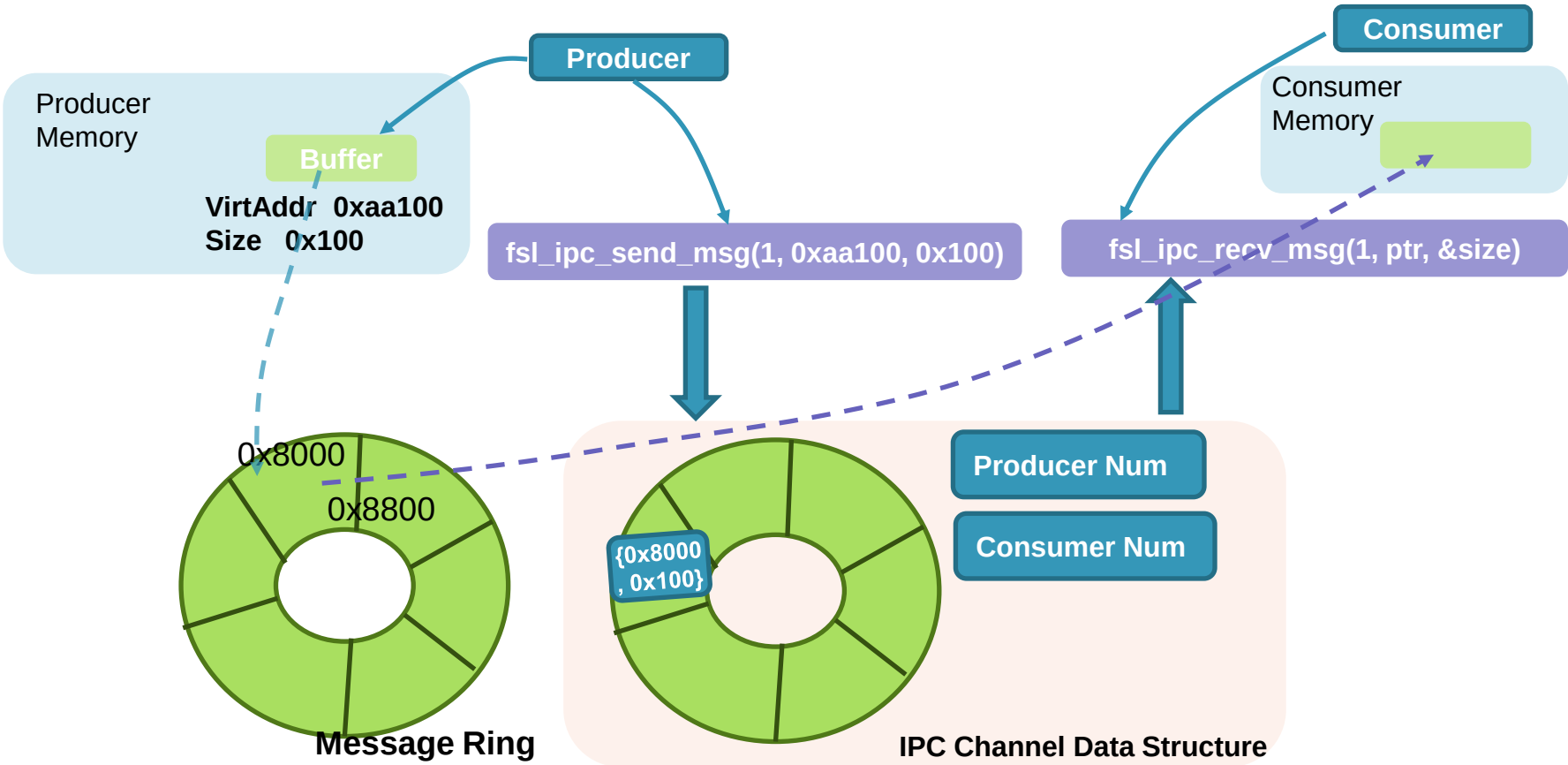
IPC Channels

- Pointer Channel
  - Producer allocates memory and provides consumer the pointer via this channel.



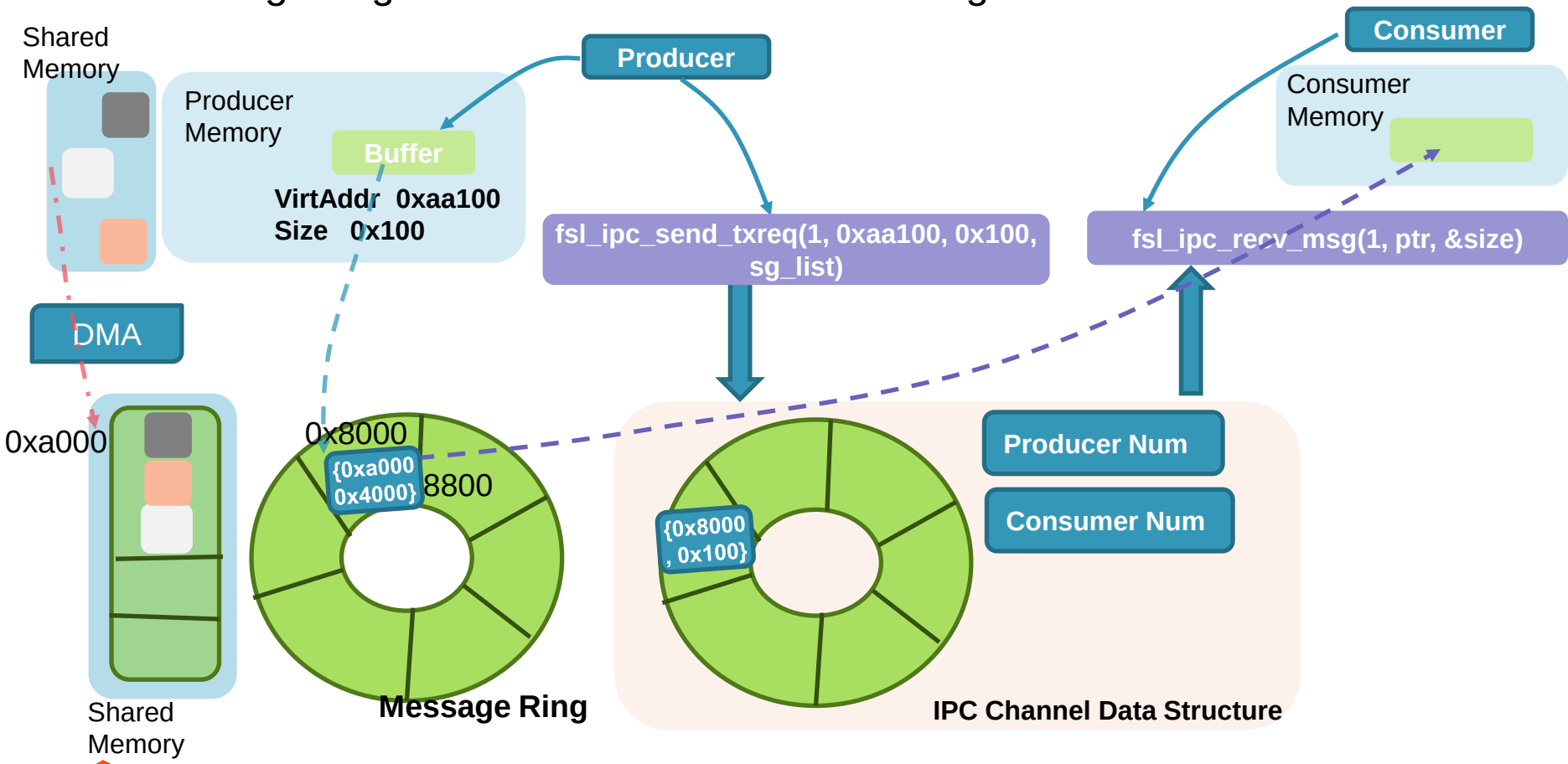
IPC Channels

- MSG Channel
  - For small messages. IPC copies producer buffer in a message ring. IPC later copies the message from message ring to consumer buffer.

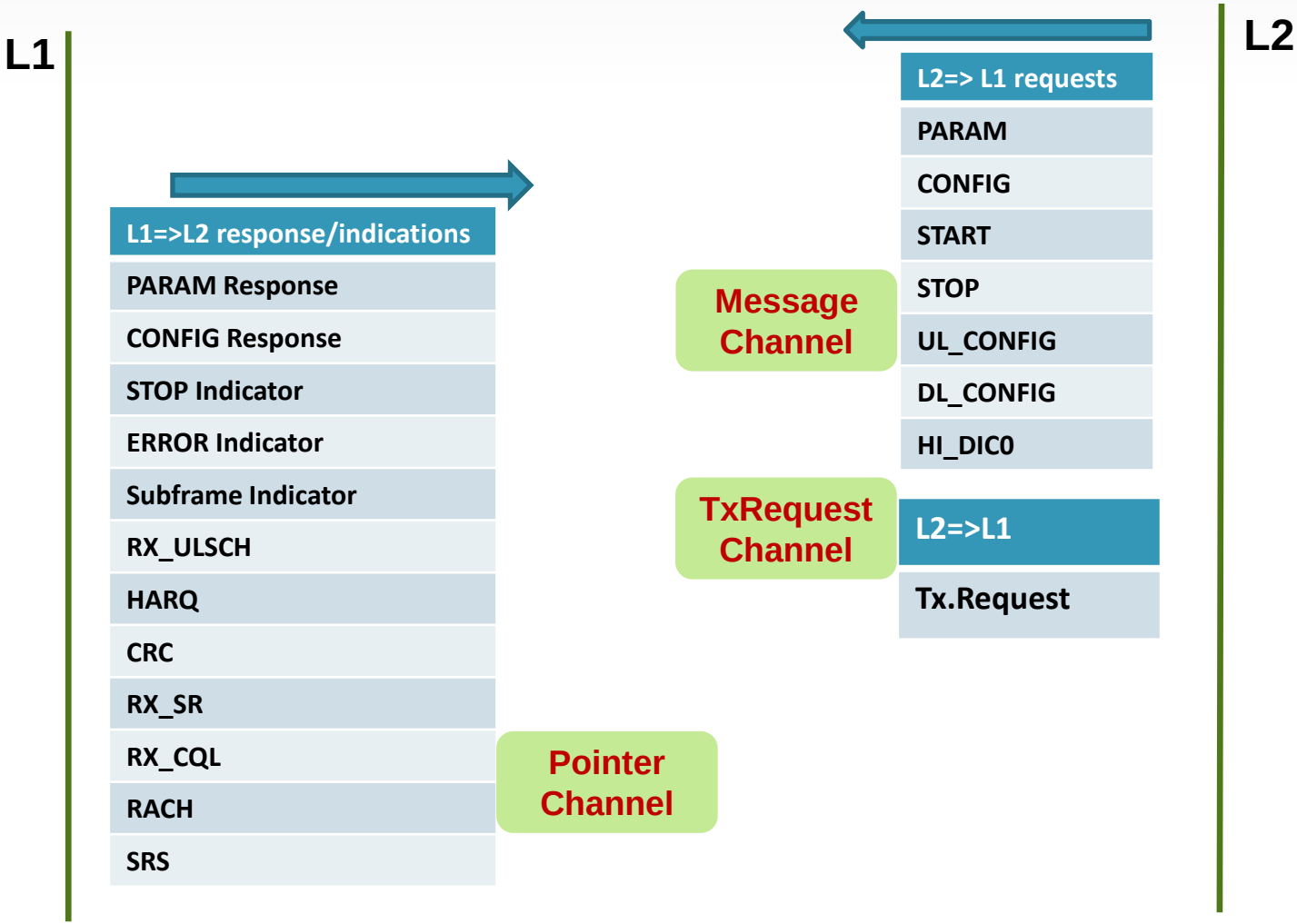


IPC Channels

- Tx Request Channel
  - For small messages and large PDU's. IPC copies producer buffer in a message ring and uses DMA to linearize fragmented PDUs.



FAPI Messages to IPC Channels Binding



Performance and Optimizations

- Consumer Message Channels towards DSP can be placed in **M2 memory for faster access**
- **Zero Copy** is achieved in Tx.Request where the average buffer size is 9k, as DMA is involved
- IPC uses **static binding of channels** at compile time, channel numbers are integer values.
- **L1/L2 share a common header file** with channel numbers as constants

Scalability

- On a multicore system Channels can be distributed among cores to do load balancing.
- Same L2 stack can run on 9131,9132 and future architectures with minimal changes.

Conclusions

- SW optimization is key to achieve performance
  - Zero-copy through use of DMA engine
  - Driver optimization to application
- Tight integration with L1 and L2 stacks drives optimized solution

References

- [1] Small Cell Forum Specifications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