IBIS Overview and Model Usage

APF-NET-T0882

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Agenda

- **IBIS Overview**
  - What is IBIS
- **How is IBIS Used?**
  - IO buffer timing and noise issues
  - Need for IO buffer models
- **IO Buffer Modeling Options**
  - SPICE vs IBIS
- **IBIS Details**
  - Details of Electrical Models and Full Device IBIS
- **Examples**
  - Clock, edge rate, DDR

IBIS Overview

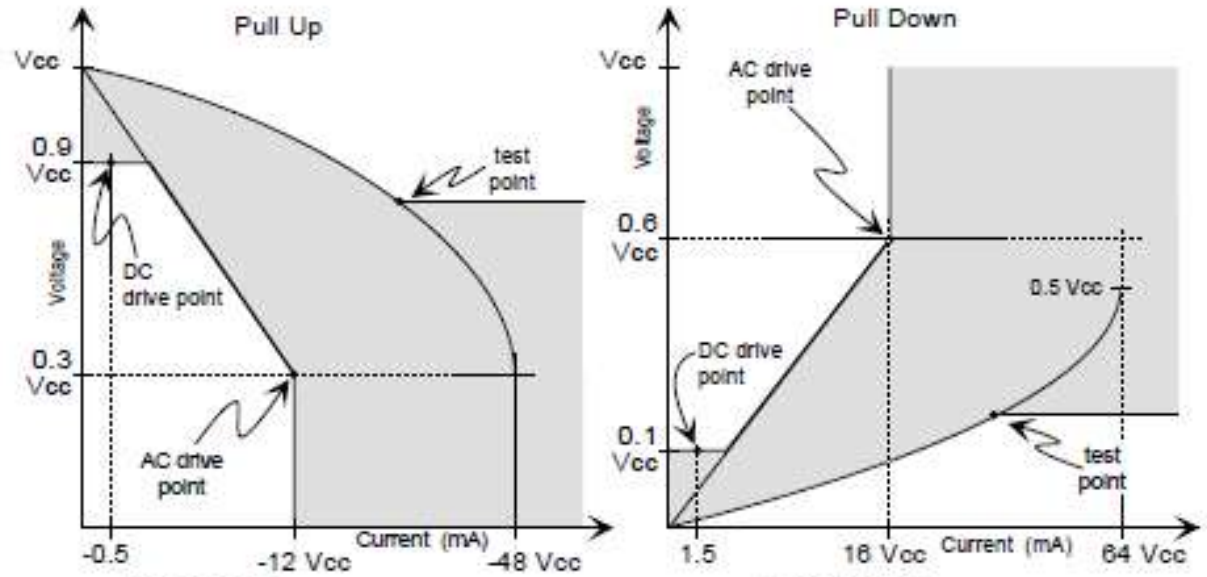
What is IBIS?

- IBIS is one piece of design collateral that FSL NMSG/NPD delivers
- Fills the need to simulate the IO buffers from the devices on a bus
  - Not a power model, not a bus functional model
- IBIS: Input/Output Buffer Information Specification
- What is IBIS?
  - Not a model, like a SPICE model
  - Tabular description of the IO buffer characteristics
  - Simulators interpret data in IBIS to produce a model

What is IBIS?

- Background – when/where did it start?
  - Behavioral Modeling
  - Based on properties of IO
  - IBIS Specification 1.0: April 1993
    - Intel credited with driving standard development for use with PCI Bus analysis and simulation
  - Same Era as PCI Spec:
    - Edge Rates Faster
    - Lumped Loads not as prevalent; move to distributed loads and transmission lines
      - Load 2-10x Edge Rate □ treat as transmission line
  - Subsequent key versions:
    - 2.1: December 1995
    - 3.2: September 1999
    - 5.0: August 2008
    - 5.1: August 2012

IV data spec from PCI Spec



Equation C:

$I_{oh} = (98.0/Vcc)*(V_{out}-Vcc)*(V_{out}+0.4Vcc)$

for $Vcc > V_{out} > 0.7\ Vcc$

Equation D:

$I_{ol} = (256/Vcc)*V_{out}*(Vcc-V_{out})$

for $0v < V_{out} < 0.18\ Vcc$

Figure 4-5: V/I Curves for 3.3V Signaling

Receiver Data from PCI Spec

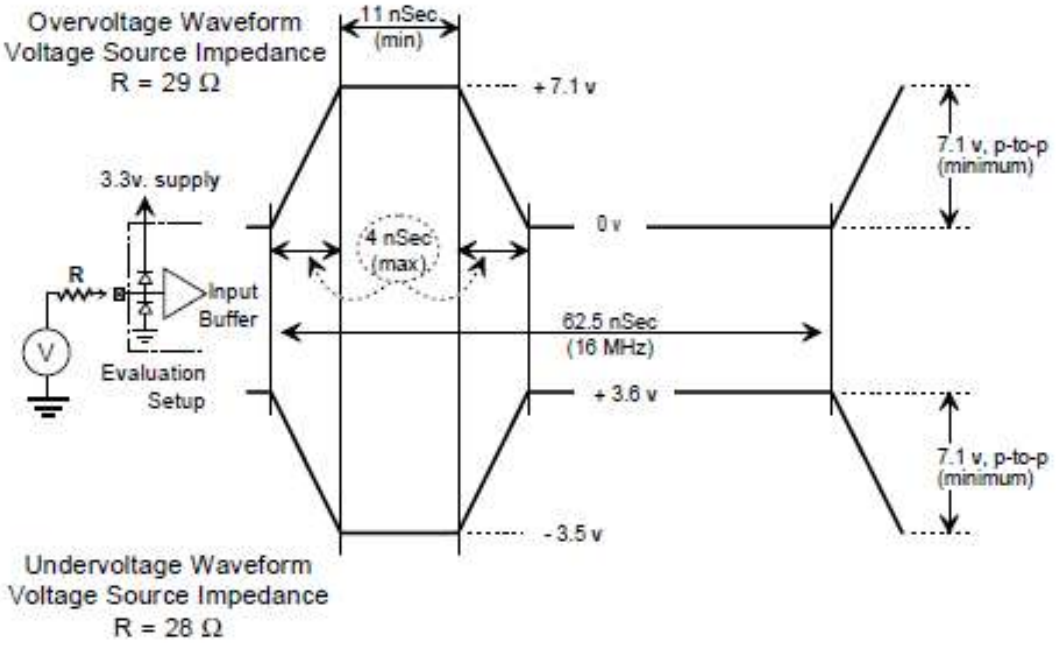


Figure 4-6: Maximum AC Waveforms for 3.3V Signaling

What is IBIS – Where is it used?

- What consumes/uses IBIS? What does IBIS feed?
  - Used by multiple EDA tools for signal integrity and timing simulations
  - EDA tools have models for the interconnect between devices
  - IO buffer models are needed to drive and receive signals that use the interconnect in the design (typically PCB)

  - EDA tools customers use:
    - Cadence PCB SI (translates to Cadence DML model)
    - Mentor Hyperlynx
    - Synopsys HSPICE
    - Agilent ADS
    - Sigrity Speed 2000
    - Altium

How is IBIS Used?

Example Timing Budget

- Timing Budgets Include Driver, Receiver, Interconnect
  - IBIS is used for predicting how the driver interacts with the interconnect
  - IBIS is used for predicting how the receiver interacts with the interconnect

Element	Skew Component	DDR3-800		DDR3-1066		Unit	Comments
		Setup	Hold	Setup	Hold		
Clock	Data/strobe chip PLL jitter	45	45	45	45	ps	
	DRAM tJITper	50	50	45	45	ps	Derate what the DRAM is tested for
	Clock skew	0	0	0	0	ps	
Transmitter	Controller skew	267	267	209	209	ps	Assume similar to DRAM and use DRAM's specifications
Interconnect	DQ crosstalk and ISI	52	52	32	32	ps	1 victim (1010...), 4 aggressors (PRBS)
	DQS crosstalk and ISI	23	23	23	23	ps	1 shielded victim (1010...), 2 aggressors (PRBS)
	Vref reduction	10	10	10	10	ps	±30mV in DRAM skew, additional ±10 mV/(1 V/ns)
	Reff mismatch	0	0	0	0	ps	±6% accounted for by DRAM specification
	Path matching (board)	10	10	10	10	ps	Within byte lane: 165 ps/in; mismatch within DQS to DQ
	Path matching (module)	5	5	5	5	ps	Module routing skew (30% reduction with leveling)
	Input capacitance matching	5	5	5	5	ps	Strobe to data variation
	ODT skew (1%)	5	5	5	5	ps	Estimated
	Total interconnect	110	110	90	90	ps	
Receiver	DRAM skew	215	215	165	165	ps	tDS, tDH from DRAM specification, derated for faster slew rates
Total loss	Total skew	592	592	464	464	ps	Transmitter + receiver + interconnect skews
MAX eye	Time available	625	625	469	469	ps	Total time available
Budget (4L)	Timing margin	33	33	5	5	ps	4-layer (microstrip) 40Ω, 0.135mm trace to trace

Predicting Effect of the Interconnect

How to calculate the system effects when interfacing with our devices?

How is the digital design implemented in the physical world (typically printed circuit board)?

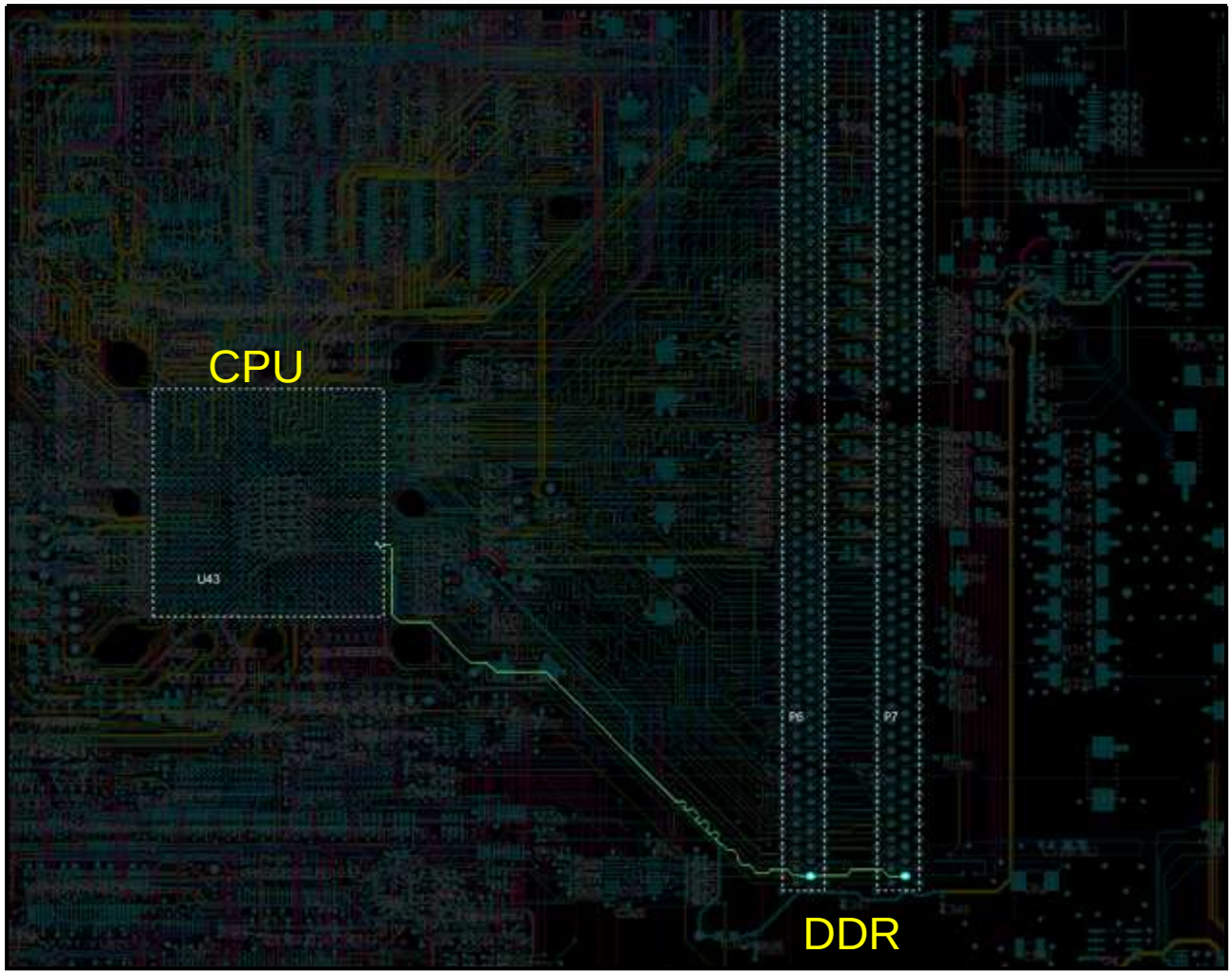
Drivers interact with interconnect

- Driver impedance
- Driver edge rate
- De-emphasis/Equalization

Receivers interact with interconnect and effect driver

- Capacitive load
- Receiver clamping
- Termination
- Equalization

Board Layout Example: DDR Memory



How to predict behavior of the CPU driving the DDR DIMMs?

Driver: CPU

- Drive strength

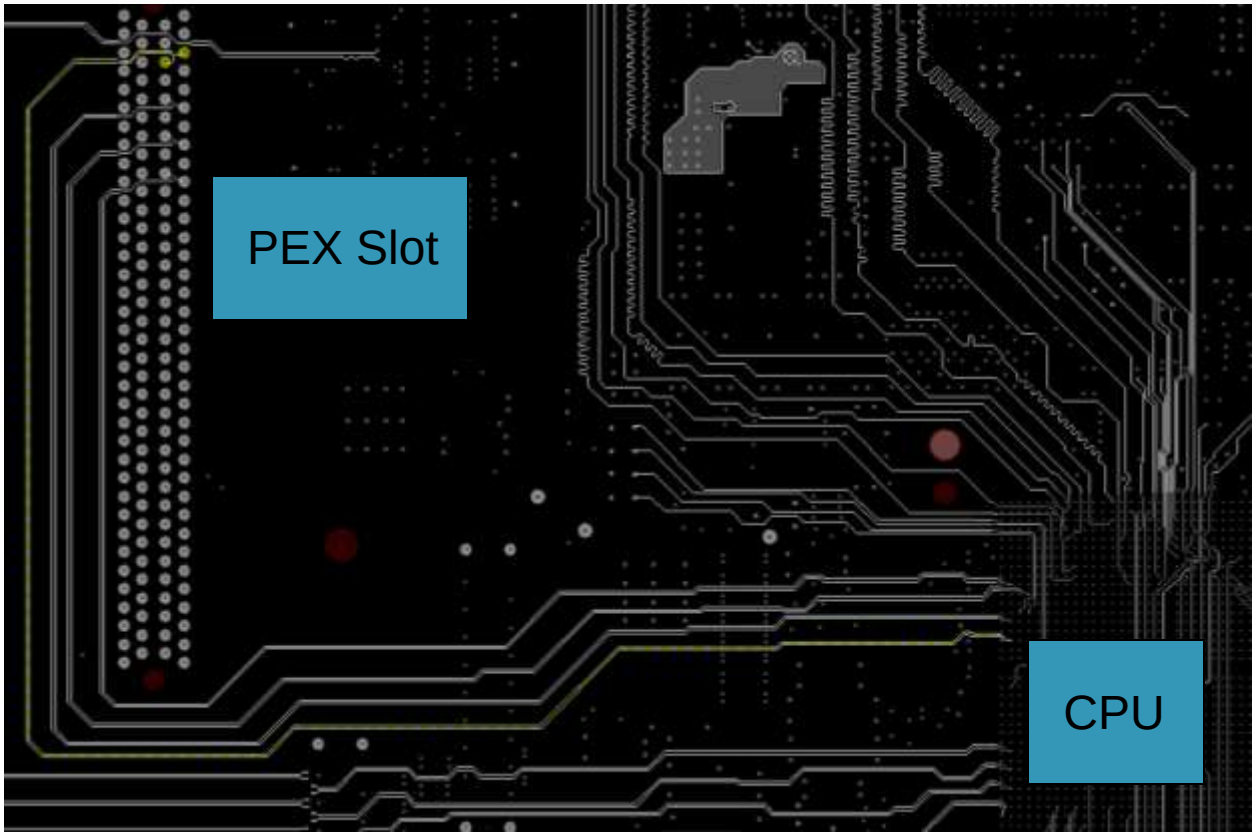
Interconnect:

- Package
- PCB Traces
- DIMM Sockets
- DIMM routing
- Crosstalk

Receiver: Memory

- ODT

Board Layout Example: SERDES



Will the PCB Interconnect degrade data eye from CPU to connector?

Driver: CPU

- Equalization

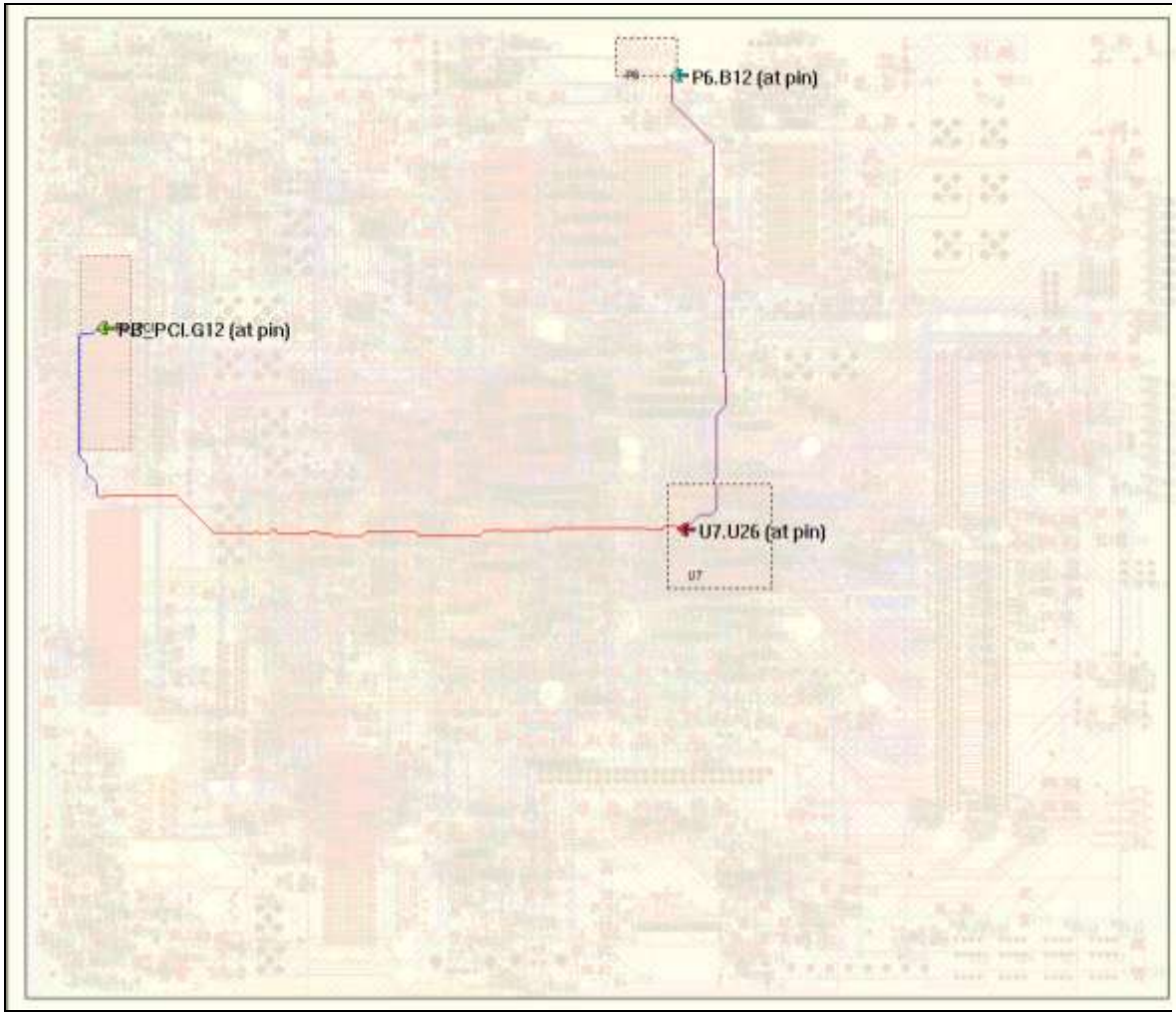
Interconnect:

- Package
- PCB Traces/Vias
- Connector
- Crosstalk

Receiver:

- Termination
- Equalization

Board Layout Example: Slower Speed Bus



Slow Clock

What if Routing to Clock Load is not at end of net?

How do edge rates affect solution?

What simulation options are available?

IO Buffer Modeling Background

IO Buffer Modeling

How to model the IO buffers?

Driver Model:

- Linear value: $Z_D = R_D$
- IV data – use in Bergeron Plots
- Circuit Model

Receiver Models:

- Lumped capacitor
- IV data
- Circuit Model

Transmission Line Effects

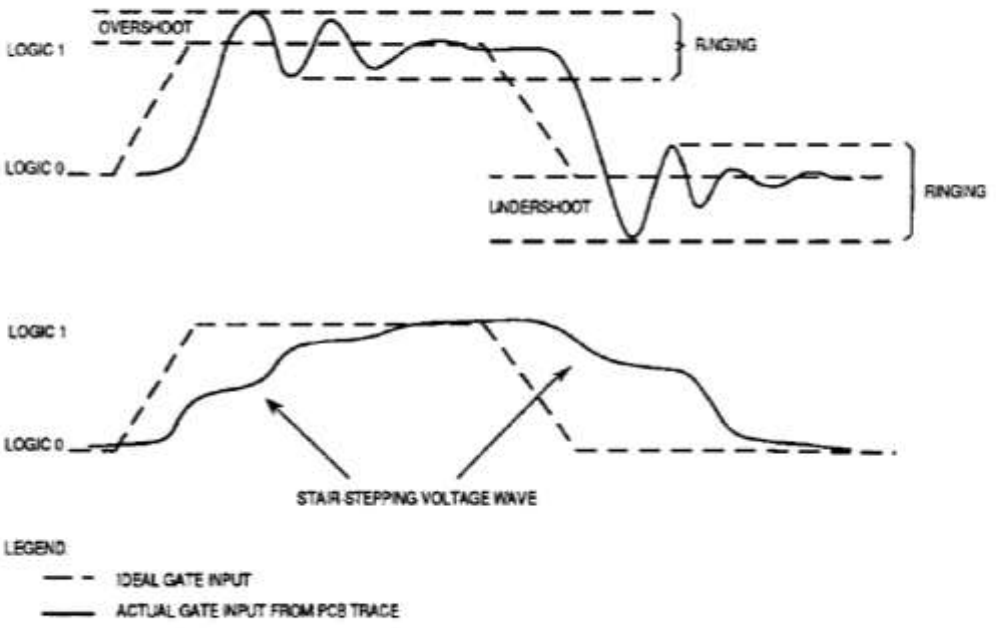
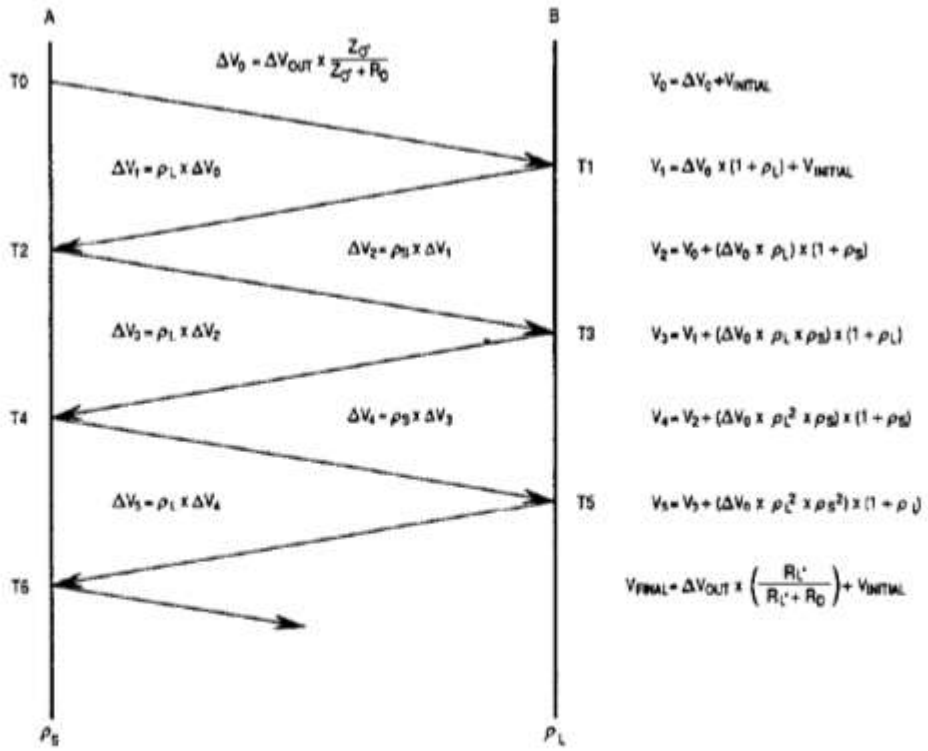


Figure 1. Transmission Line Effects

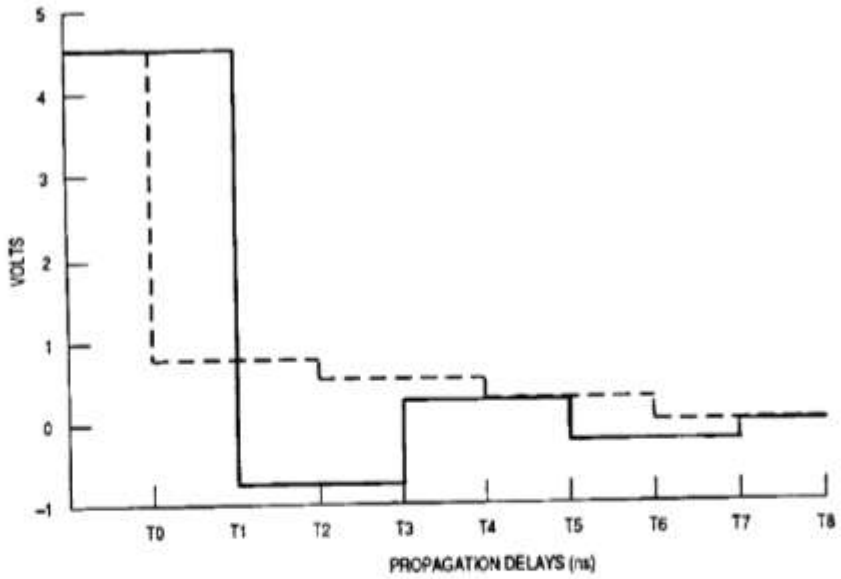
Lattice Diagram



NOTE: ρ_L and ρ_S are reflection coefficients and $V_{INITIAL}$ is the steady-state voltage prior to the switching of the gate. Each TD is a propagation delay(T_{PD}) in duration. A and B indicate the driving and receiving ends of the trace, respectively.

(a) Lattice Diagram

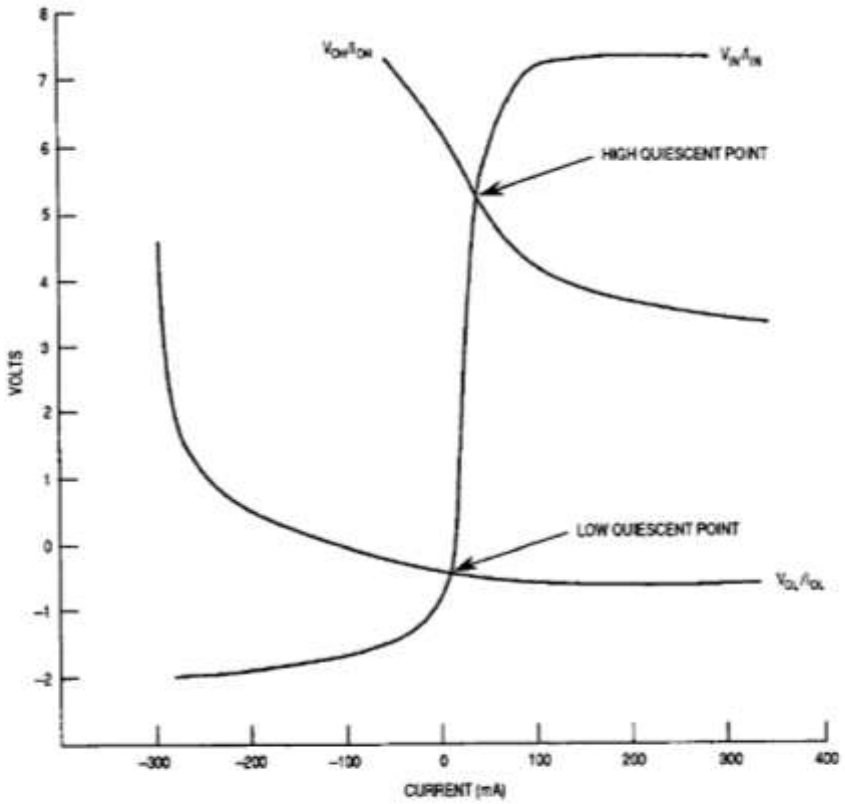
Voltage Plot from Lattice Diagram



(b) Voltage Versus Time Plot

Figure 5. Lattice Diagram Representations (Sheet 2 of 2)

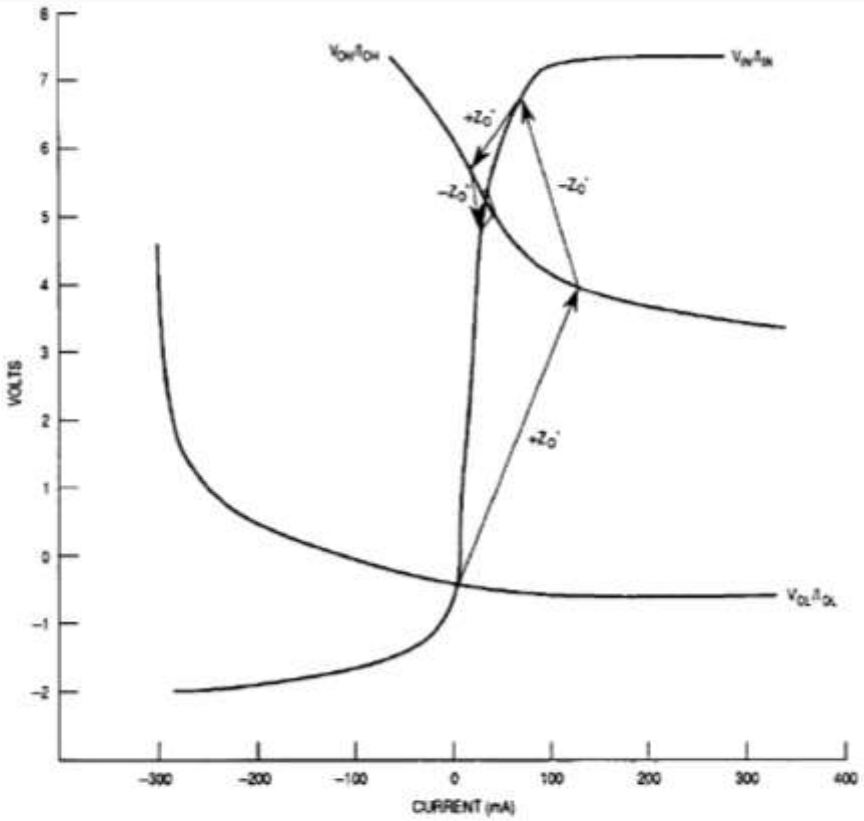
Bergeron Plot – overlay device IV curves



NOTE: V_{OL}/I_{OL} and V_{OH}/I_{OH} are output curves for the driving device; V_{IN}/I_{IN} is the input curve for the receiving device.

Figure 6. Bergeron Plot

Bergeron Plot with Interconnect Impedance



NOTE: V_{OL}/I_{OL} and V_{OH}/I_{OH} are output curves for the driving device; V_{IN}/I_{IN} is the input curve for the receiving device, and Z_0 is the loaded characteristic impedance of the trace.

Figure 7. Bergeron Plot with Transitions

Bergeron Graphical Method for Water Hammer

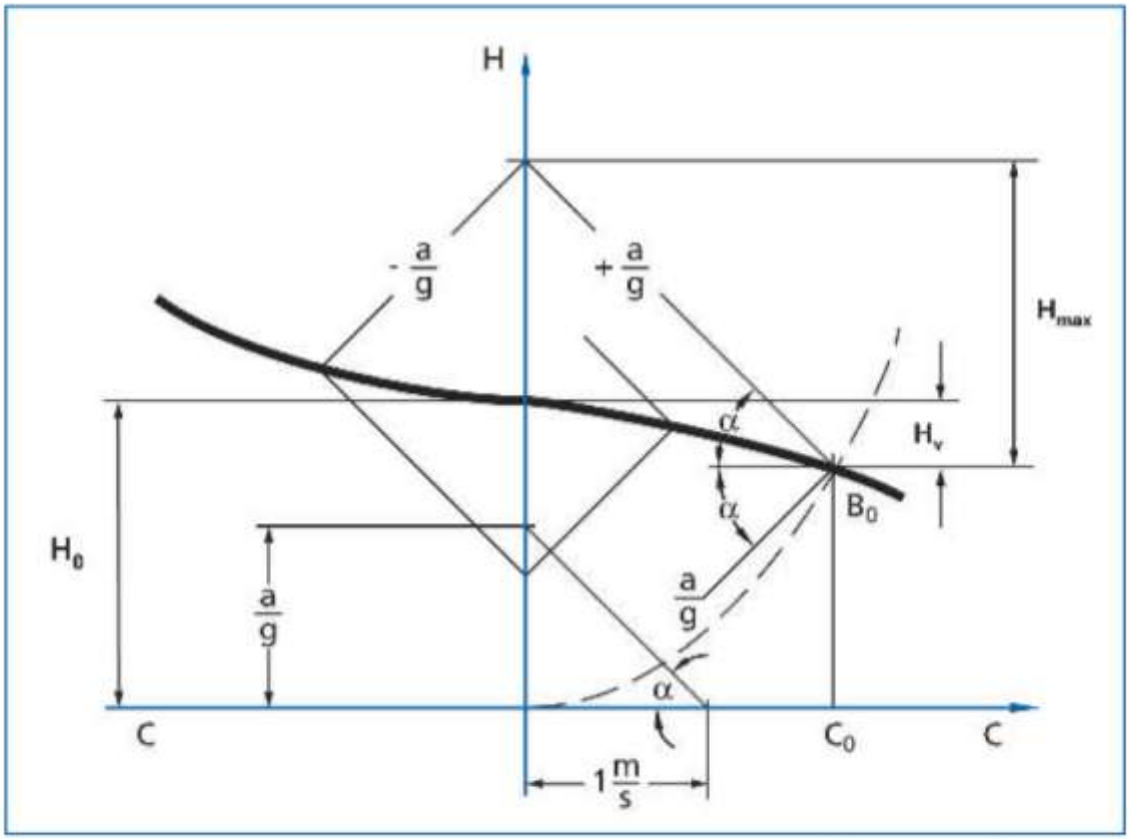
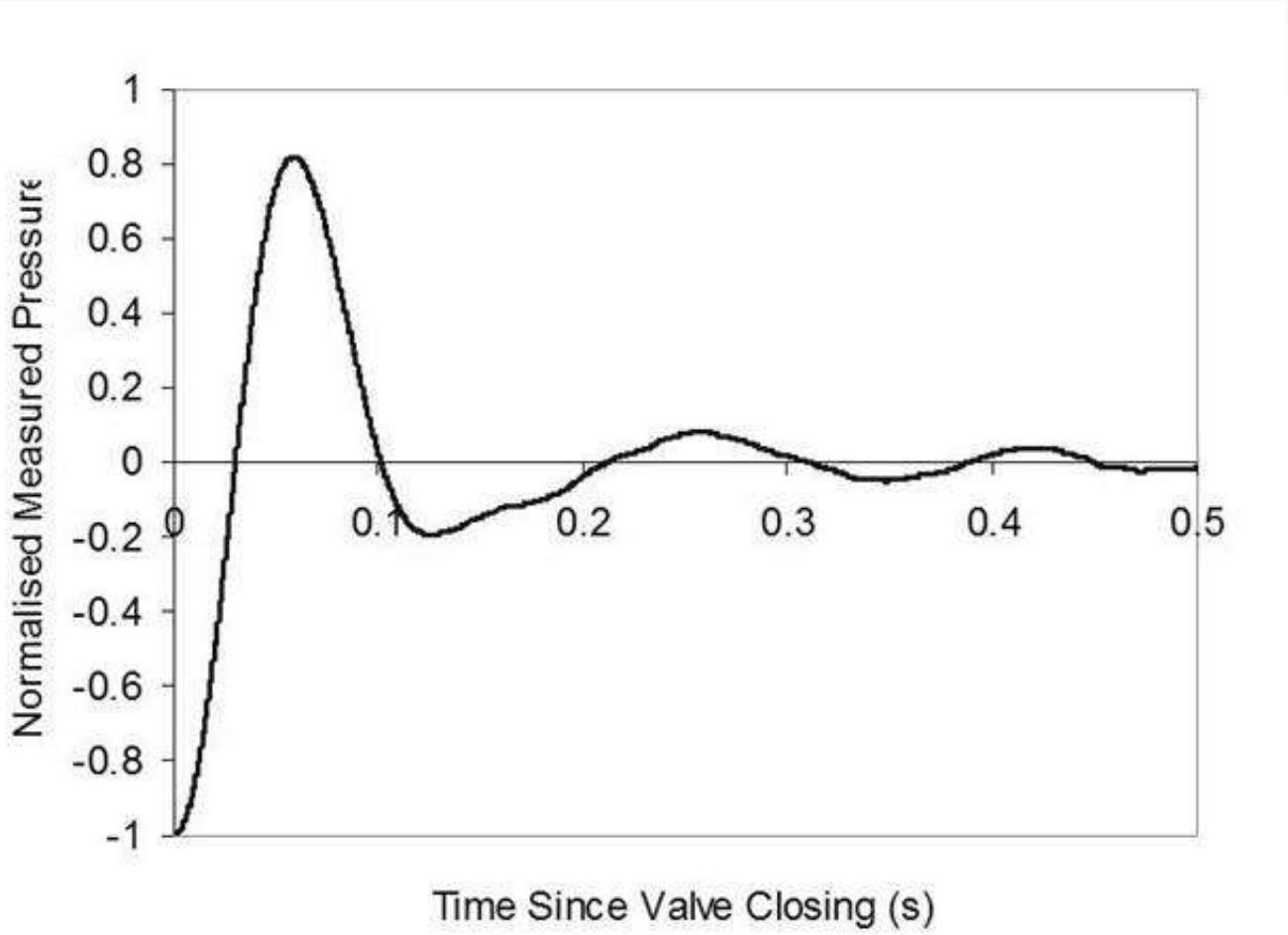


Fig. 7-1: Graphical method developed by Schnyder-Bergeron

Water Hammer Pressure



Detailed IO Buffer Modeling Solution: SPICE and IBIS

- Better means that linear models:
  - SPICE
  - Behavioral
- SPICE solutions used for circuit design
  - Based on IO buffer's physical dimensions
- SPICE has long runtime for layout-based (most accurate) IOs
- SPICE could have proprietary buffer design and process information
- SPICE models may not easily work together if global parameters are used in IO models.
- IBIS fast runtime and data descriptive of IO buffer

Details of IBIS: What are the pieces?

Elements of IBIS

Data needed for electrical modeling of the IO:

- Electrical Data
- Hardware Specification Data
- Pin Listing
- Package Data

Details of IBIS: How to derive the electrical model data?

Elements of IBIS: Electrical Data

DC IV Data
- Pulldown
- Pullup
- Ground Clamp
- Power Clamp

Transient (Voltage vs. Time) Data
- Ramp or dv/dt ratio
- VT: rising, pulled low
- VT: rising, pulled high
- VT: falling, pulled low
- VT: falling, pulled high

Data is simulated or measured across process, voltage, temperature
- IBIS min: worst-case drive (slow process, low voltage, high temperature)
- IBIS typ: typical-case drive (typ process, typ voltage, typ temperature)
- IBIS max: best-case drive (fast process, high voltage, low temperature)

From IBIS Cookbook

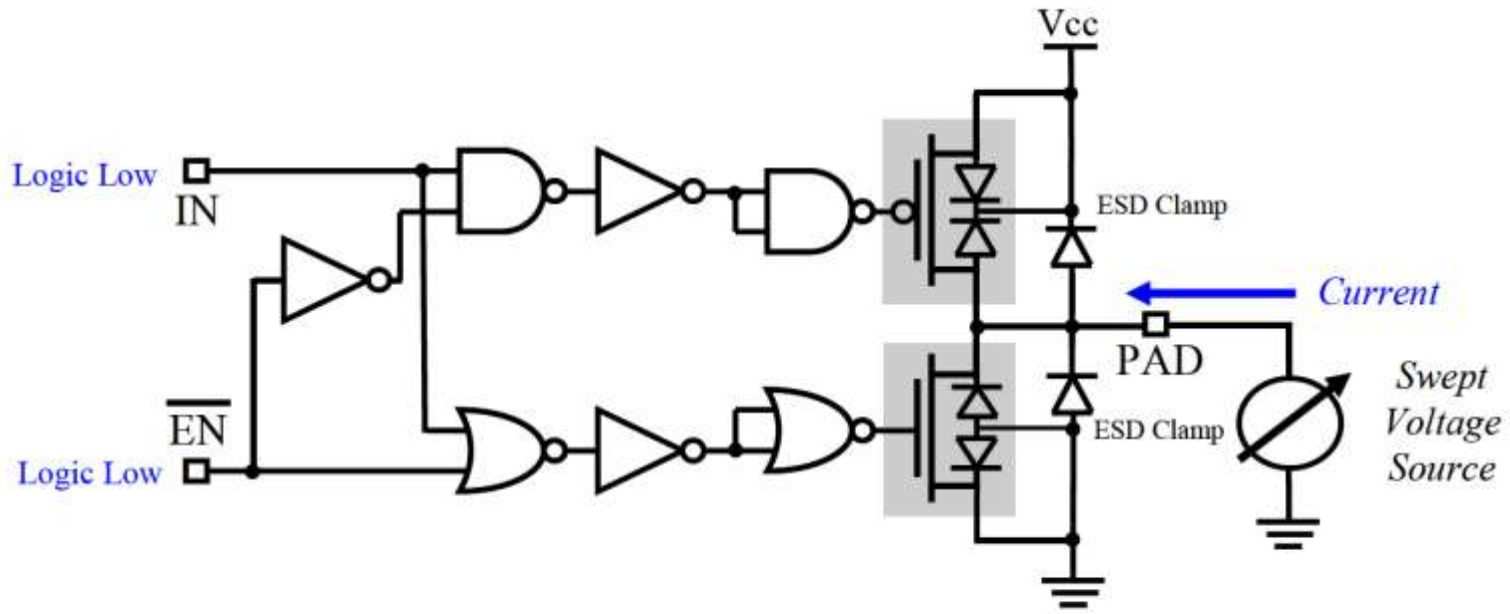
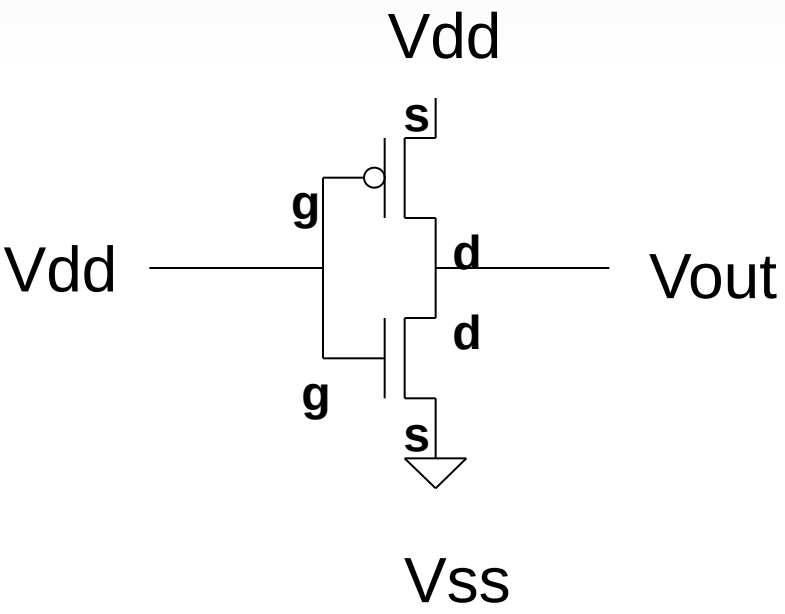


Figure 3.1 – Standard 3-state Buffer (Pulldown I-V Table Extraction Shown)

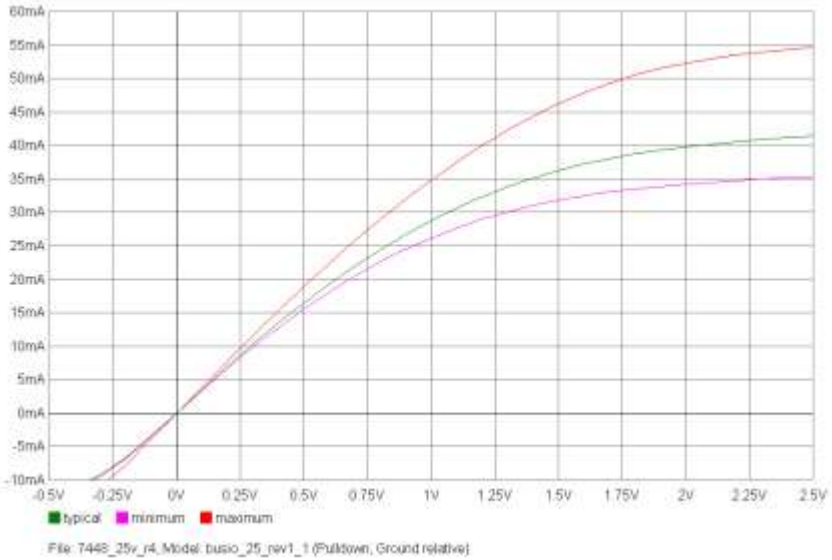
DC IV Data: Pulldown



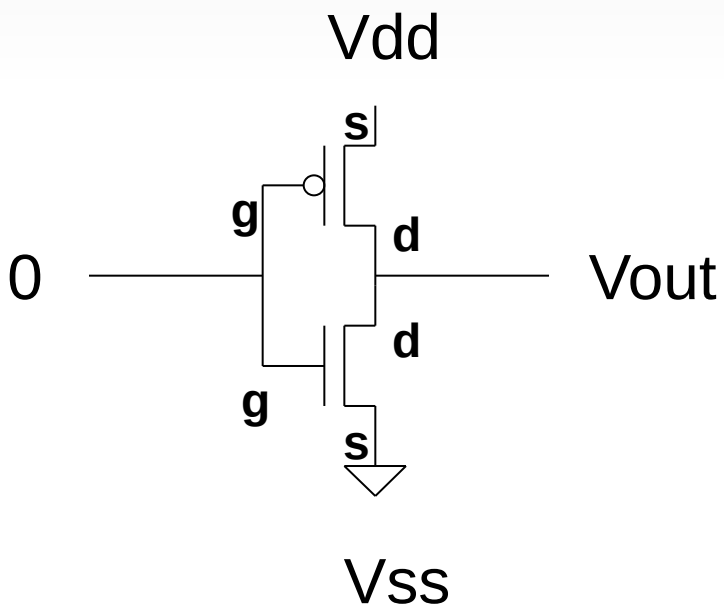
Pulldown Extraction:

Excite Pulldown (e.g. NMOS)

Sweep I vs. –Vdd to 2Vdd



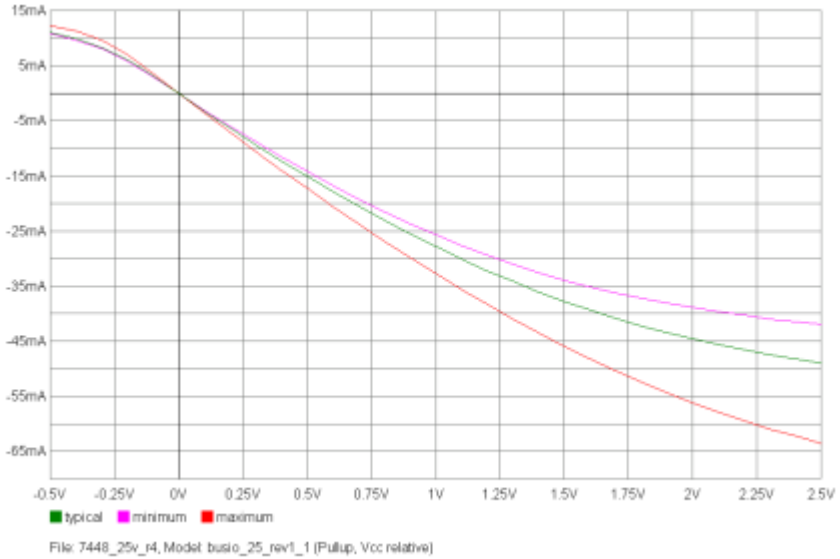
DC IV Data: Pullup



Pullup Extraction:

Excite Pullup (e.g. PMOS)

Sweep I vs. –Vdd to 2Vdd



From IBIS Cookbook

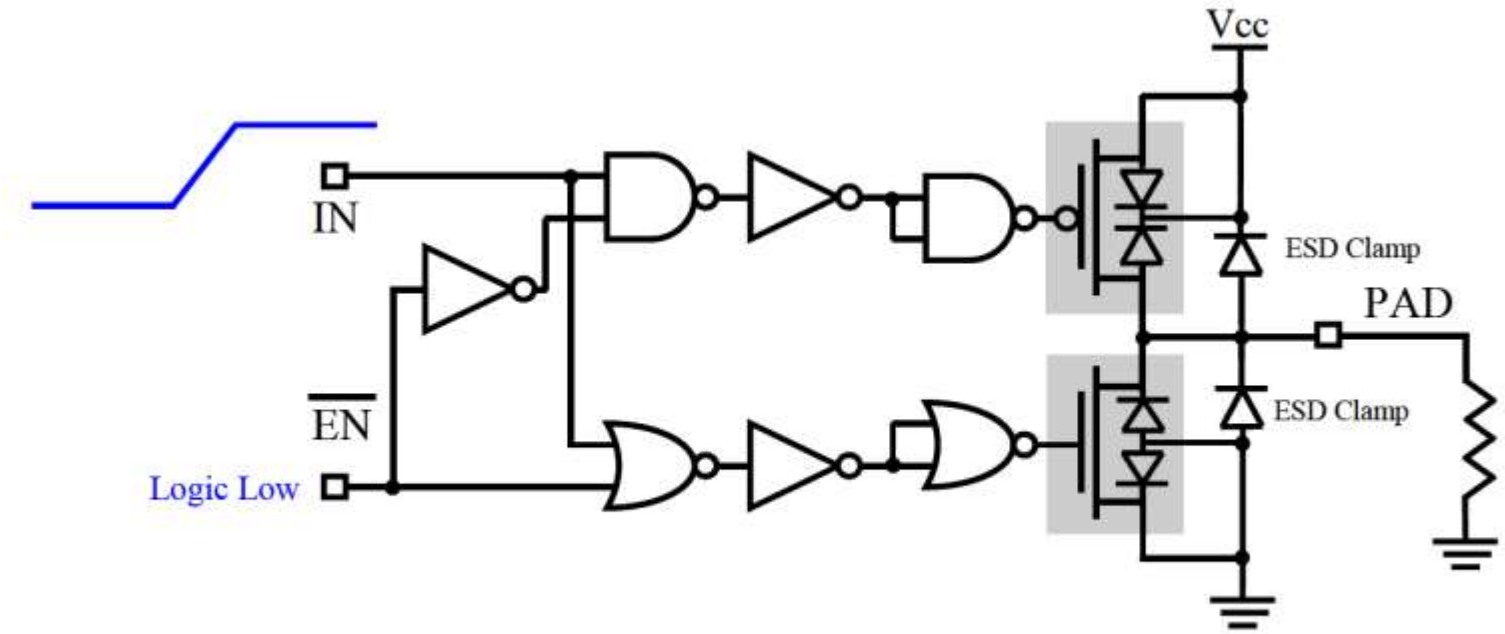
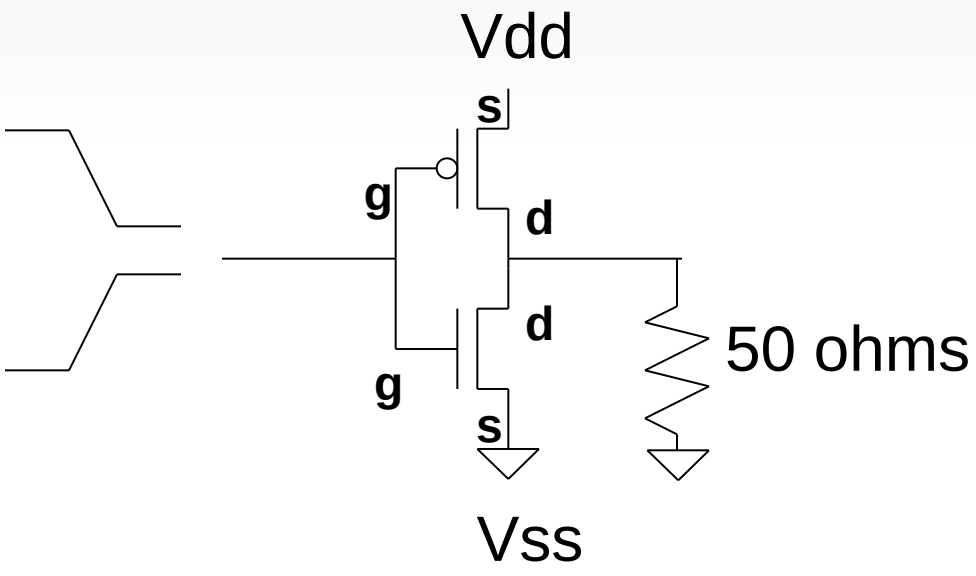
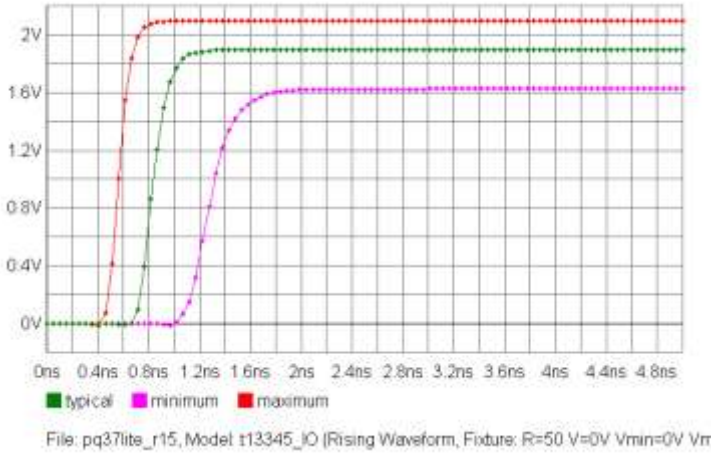


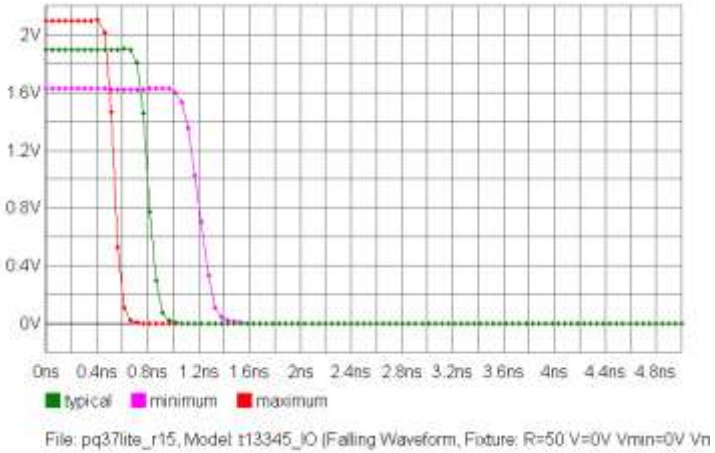
Figure 3.2 – Simulation Setup for Extracting Ramp Rate Information (Rising Edge Shown)

Transient Data: 50 ohm resistor tied to Ground

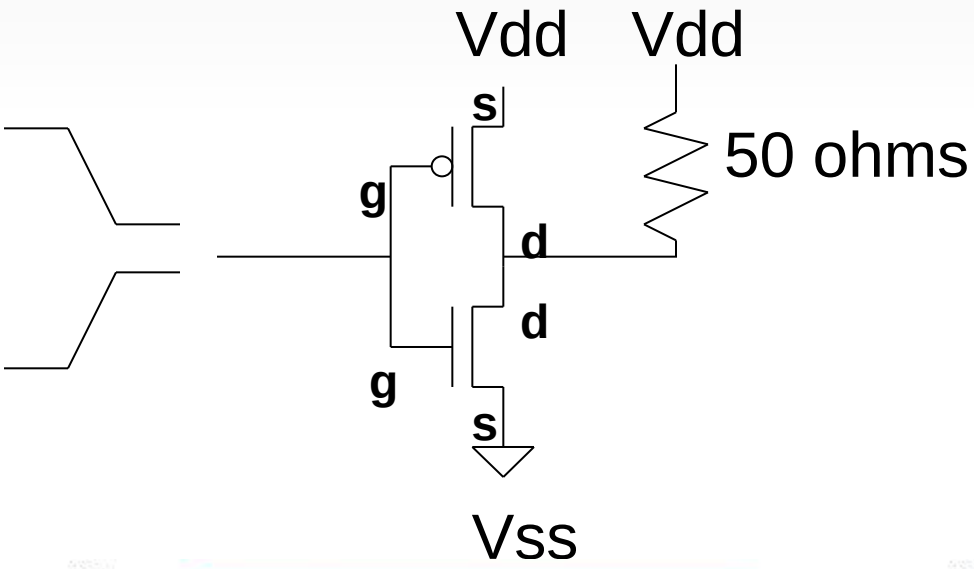


Rising and Falling Voltage vs. Time table with 50 ohm resistive load tied low

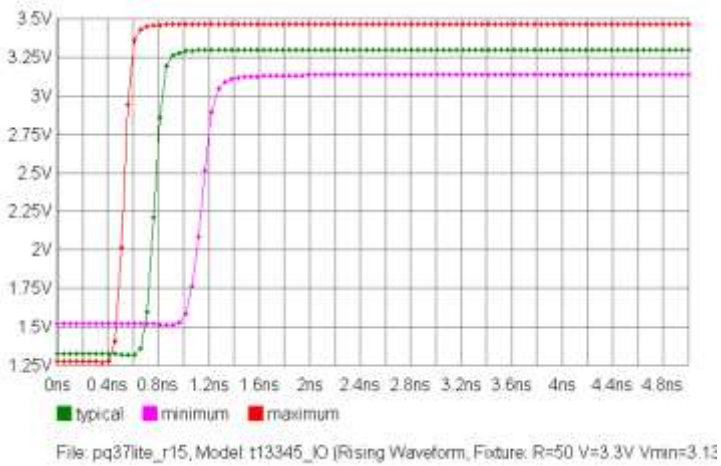


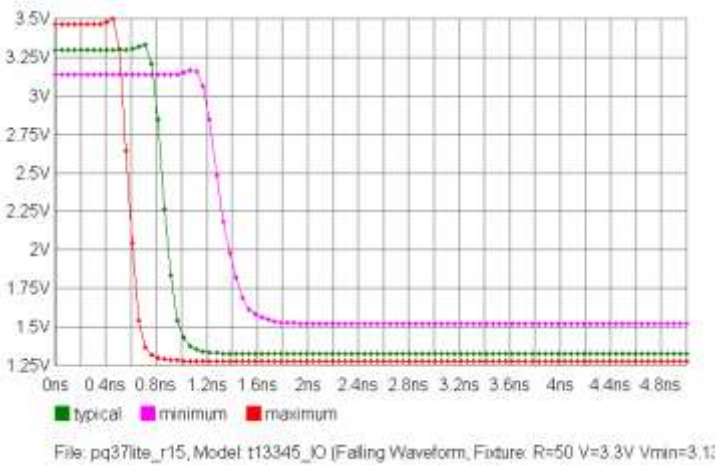


Transient Data: 50 ohm resistor tied to VDD



Rising and Falling Voltage vs. Time table with 50 ohm resistive load tied high





Elements of IBIS: Hardware Spec Related Data

Signal name and buffer description items:

- Pin List
- Signal to IO buffer model map
- Programmable/selectable drive strength IOs
- Differential pair map

Operating conditions and Hardware Spec value items:

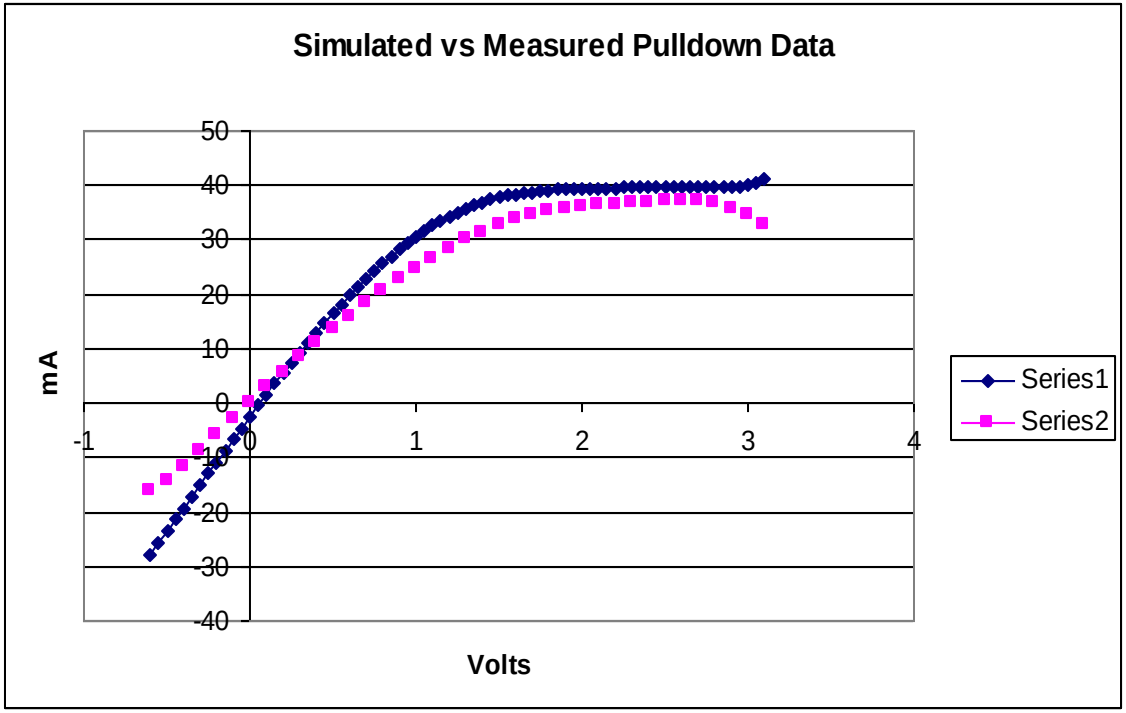
- OVdd: min, typ, max
- Temperature: min, typ, max
- Test Load: Vmeas, Vref, Cref, Rref
- Input voltage levels: Vinl, Vinh
- Overshoot and undershoot levels

IBIS Correlation

IBIS Development and Checking Procedure

- IBIS Checker Status
  - IBIS checked using 3.2, 4.1, 5.0 checkers
  - Visual IBIS inspection
  - Warnings reviewed
- Simulation Comparison
  - IBIS-based simulations vs. internal SPICE
- Measured IBIS
  - Tester-based IBIS data
  - Allows IBIS to track actual silicon and process updates

Measured vs. Simulated Pulldown Data



Blue is measured; purple is simulated

Example IBIS-based Simulations

IBIS-based simulation examples

- Examples of problems IBIS can help evaluate:

  1) Slow Bus Daisy Chain Route
     - Vary Edge Rate and Terminations

  2) Input Signal Edge Rate
     - Clock Signal Edge Rate → need to meet FSL clock input timing specs

  3) Input (Read) Signal Quality
     - Look at Die vs Pin

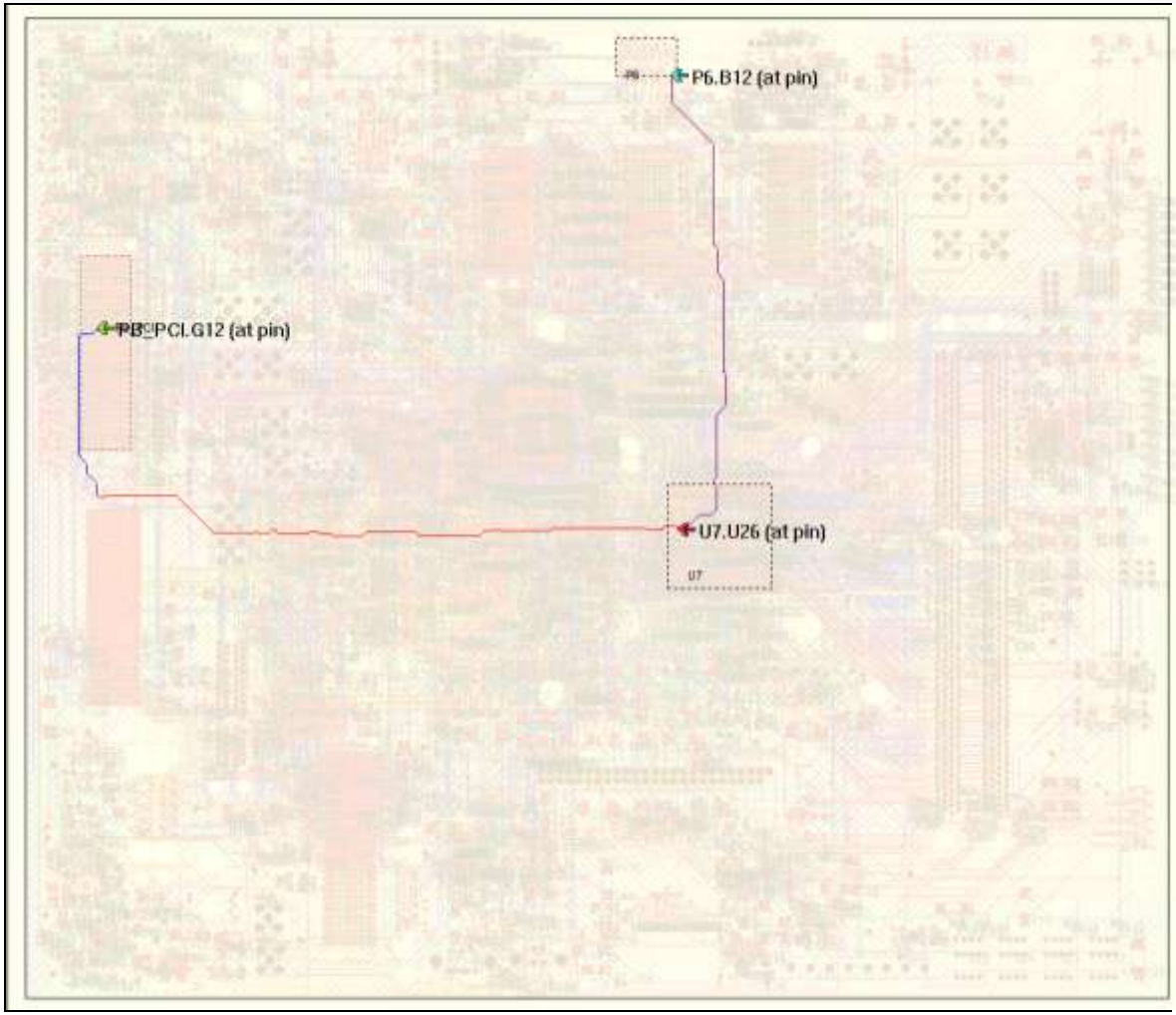
  4) DDR Read Signal

  5) DDR write timing
     - DDR3-1866 with two DIMM slots
       - Simulate to measure which DIMM slot has best signal quality and timing

1) Daisy Chain Load

Vary Edge Rate, Termination

Board Layout Example: Slower Speed Bus



Slow Clock

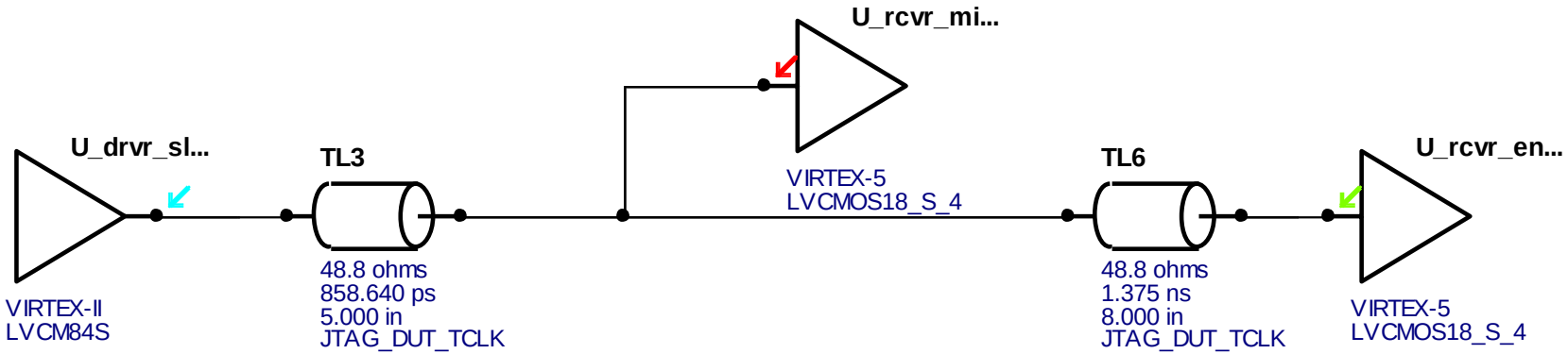
What if Routing to Clock Load is not at end of net?

How do edge rates affect solution?

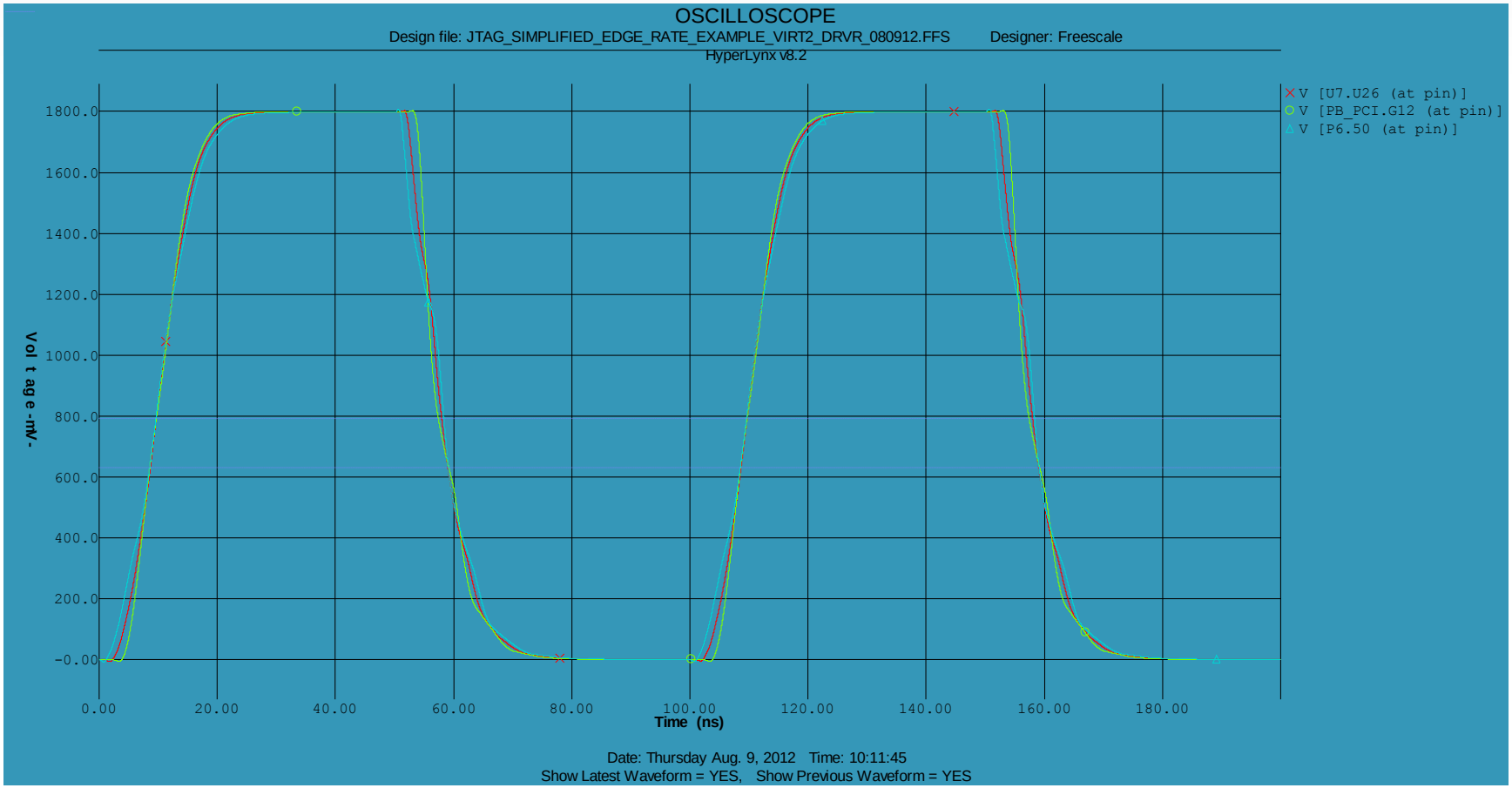
What simulation options are available?

Slow Edge Rate Daisy Chain

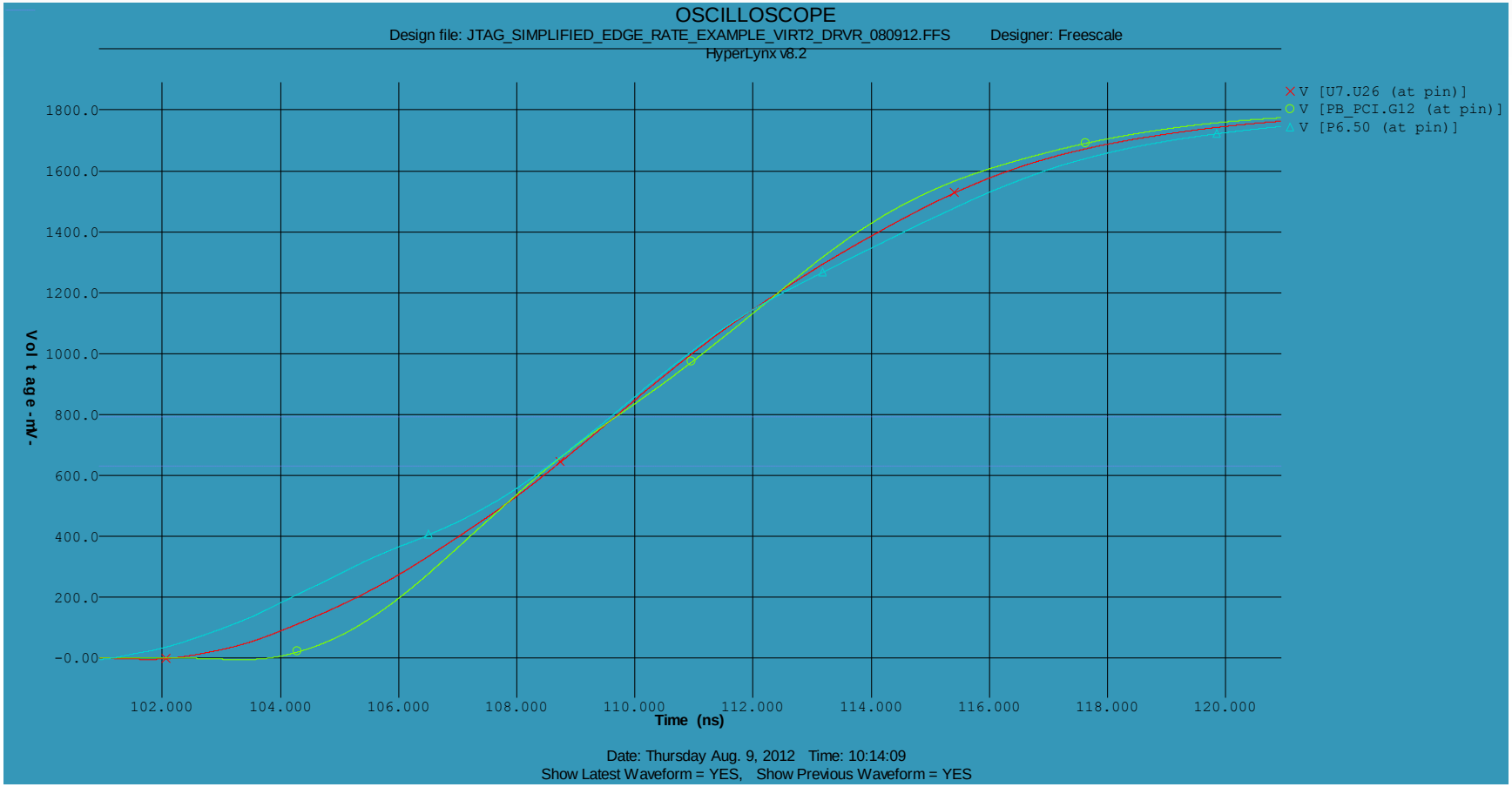
Design File: JTAG_simplified_edge_rate_example_virt2_dvr_080912.ffs
HyperLynx LineSim v8.2



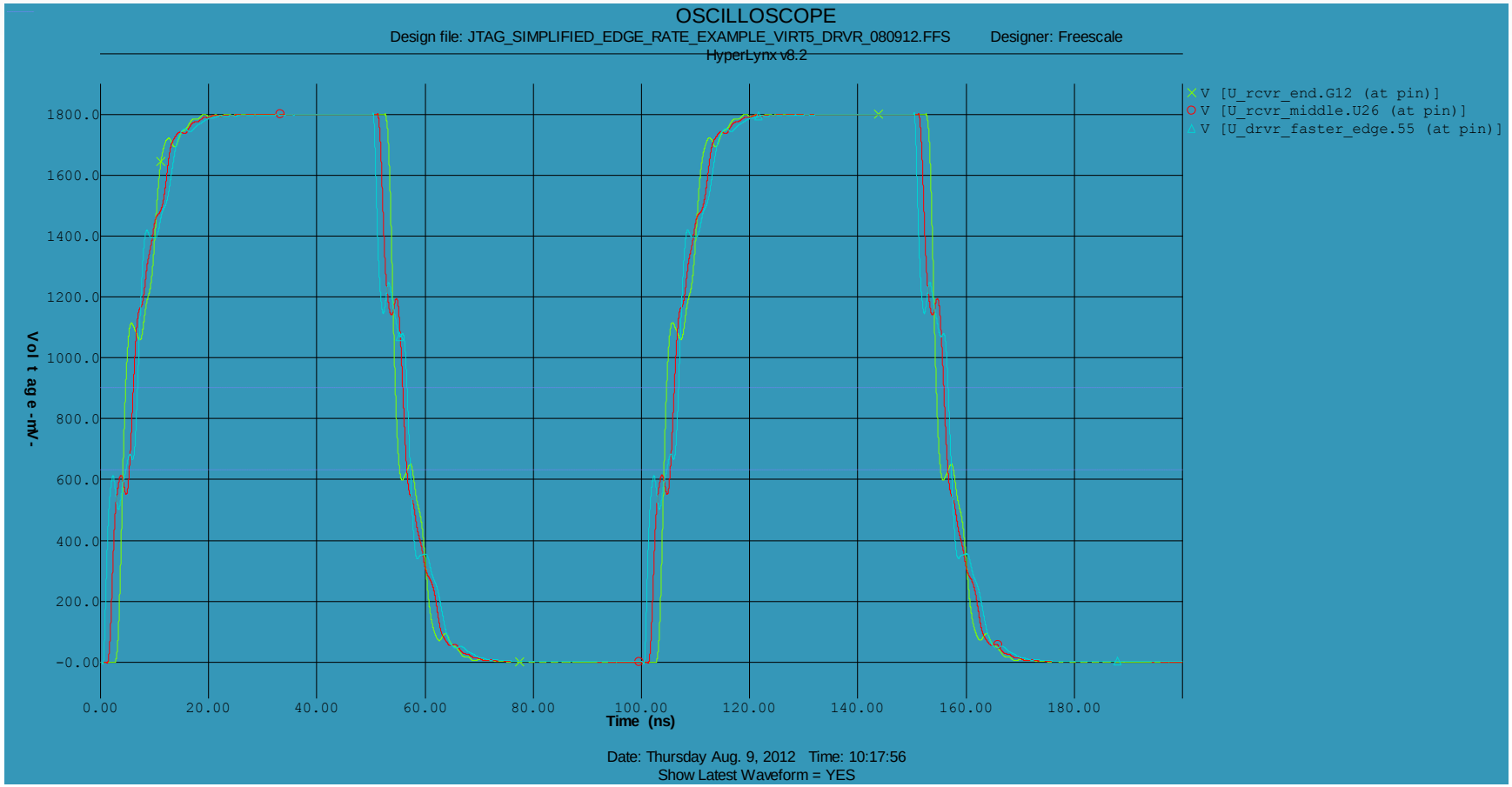
Slow Edge Rate Daisy Chain



Slow Edge Rate Daisy Chain



Faster Slow Edge Rate Daisy Chain



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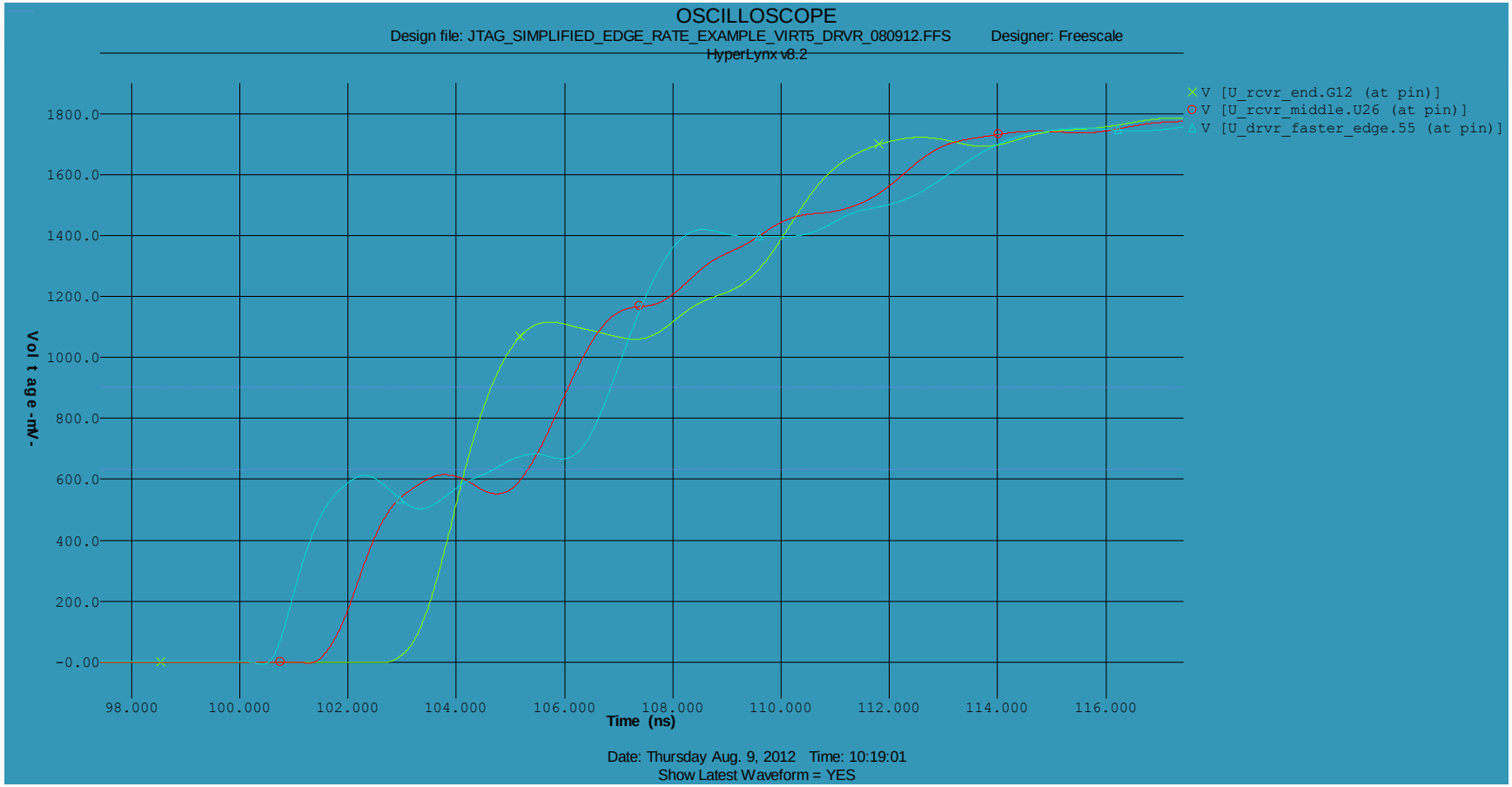

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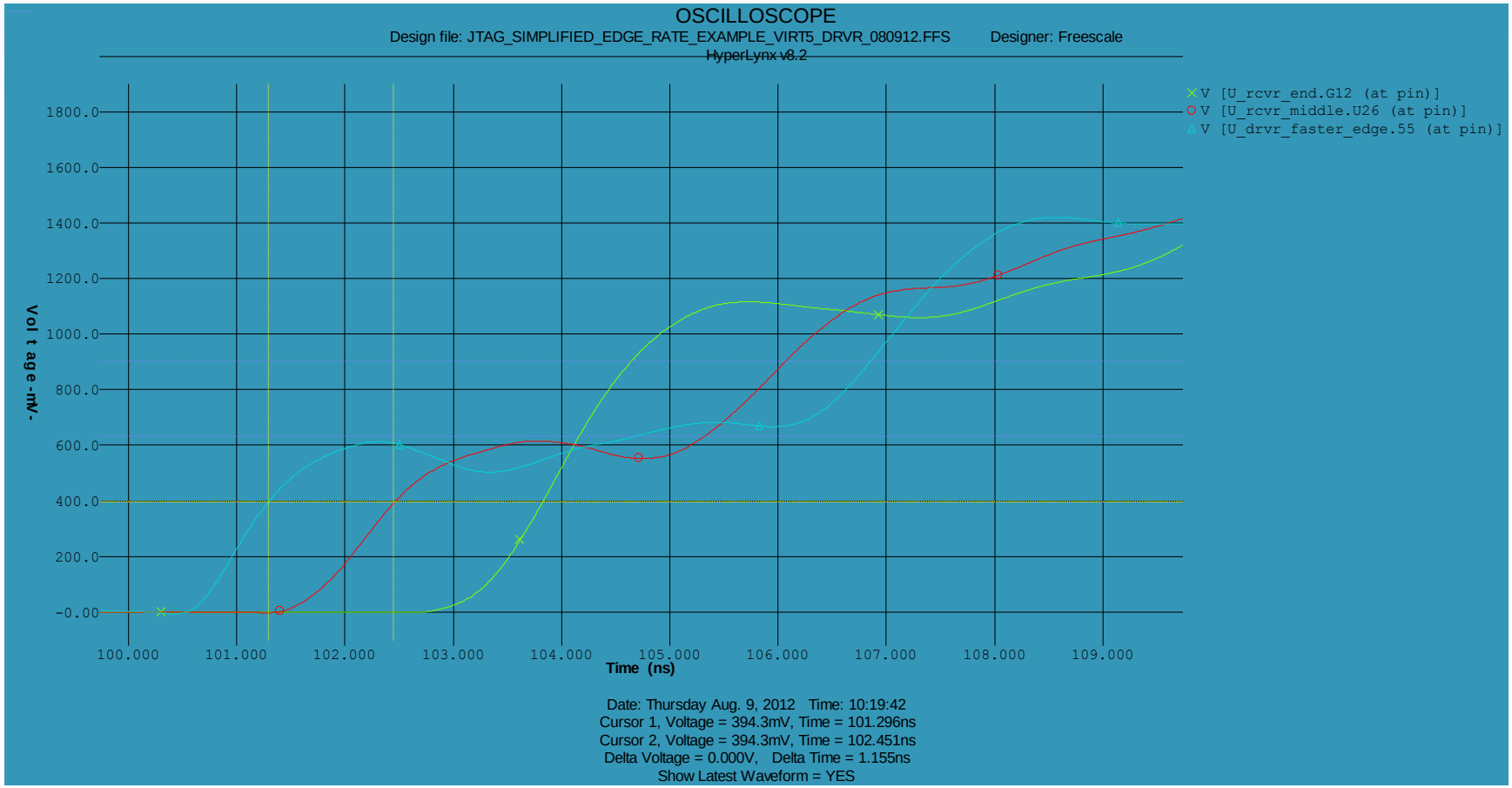
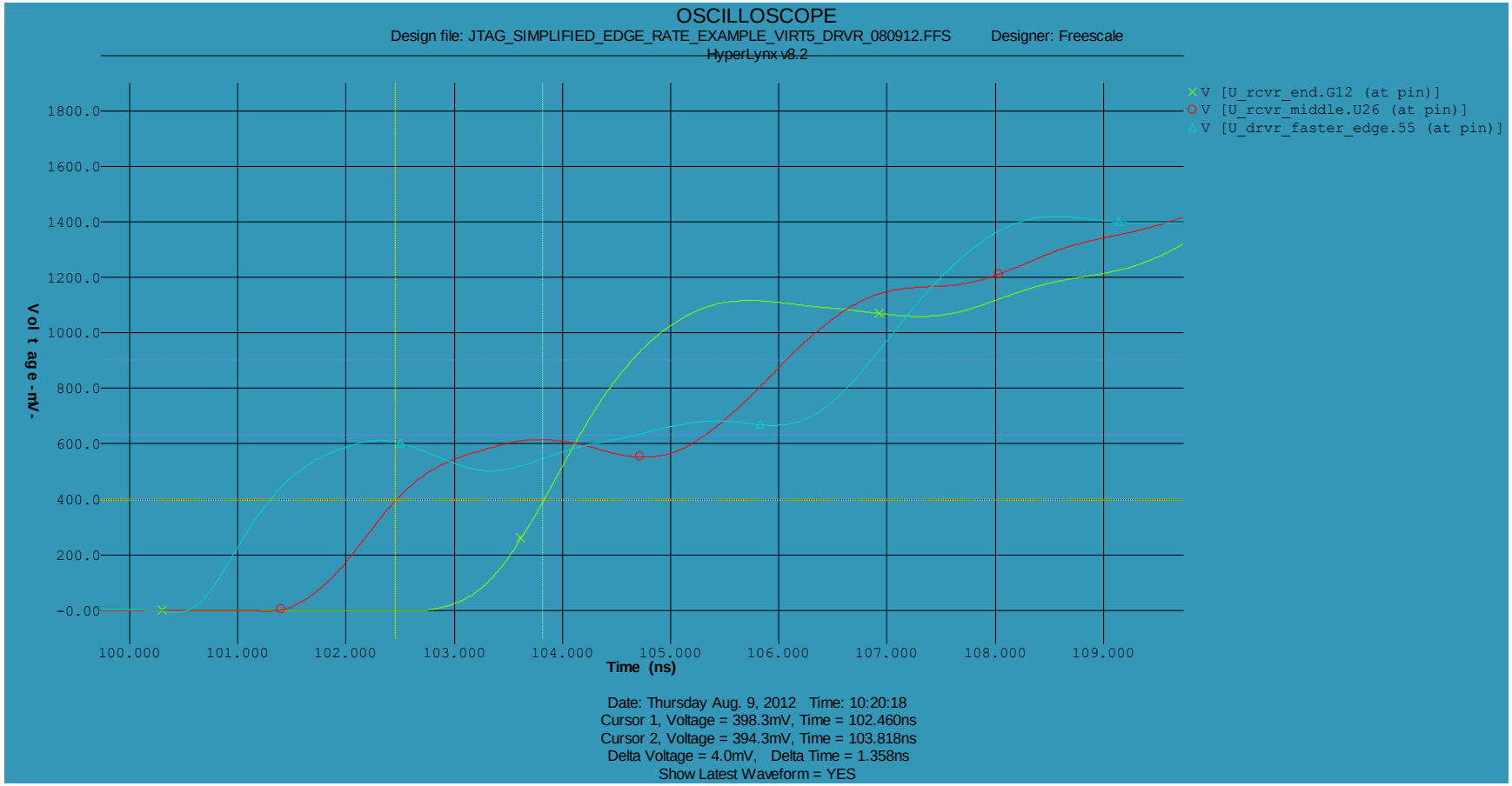
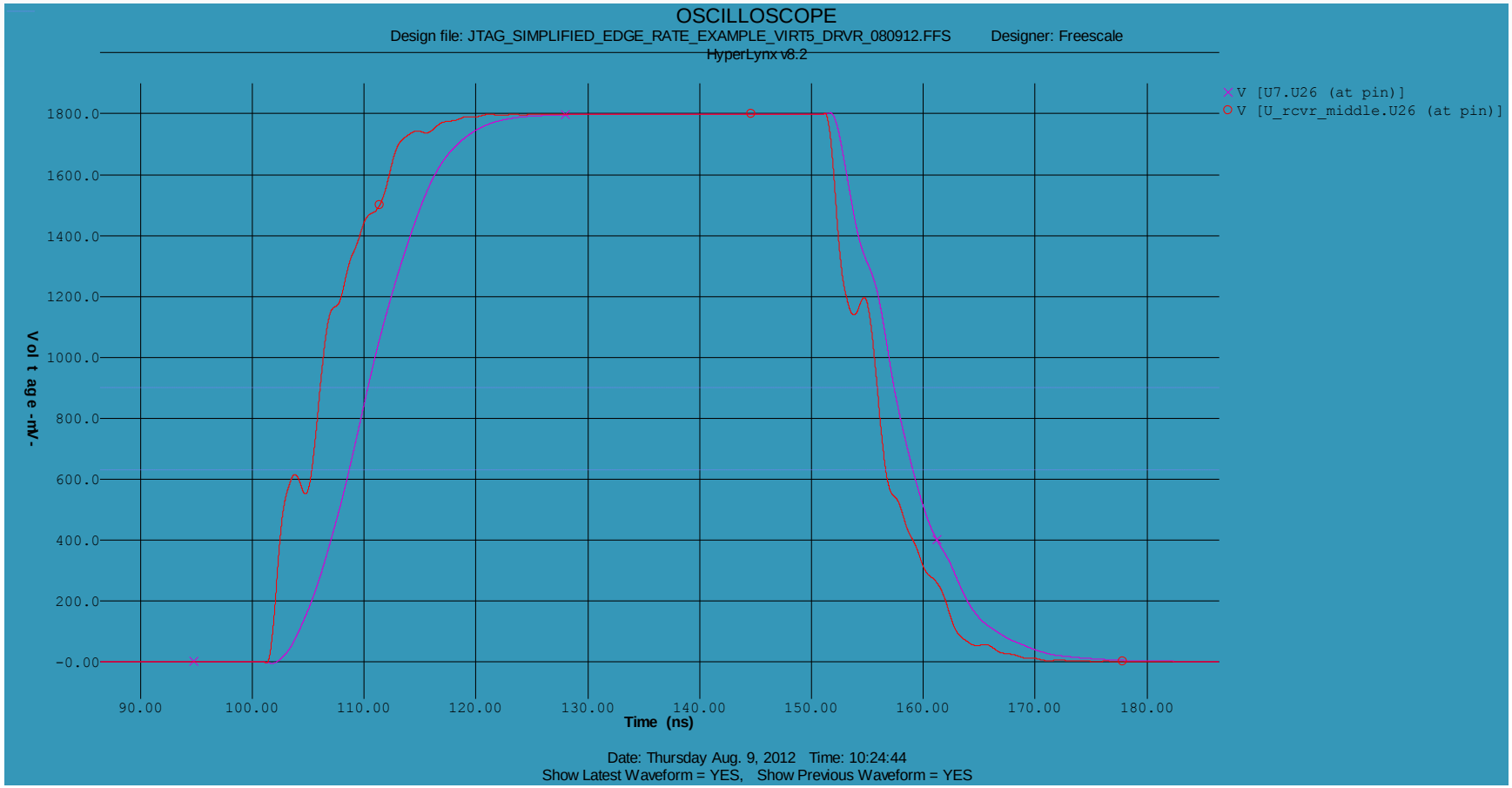


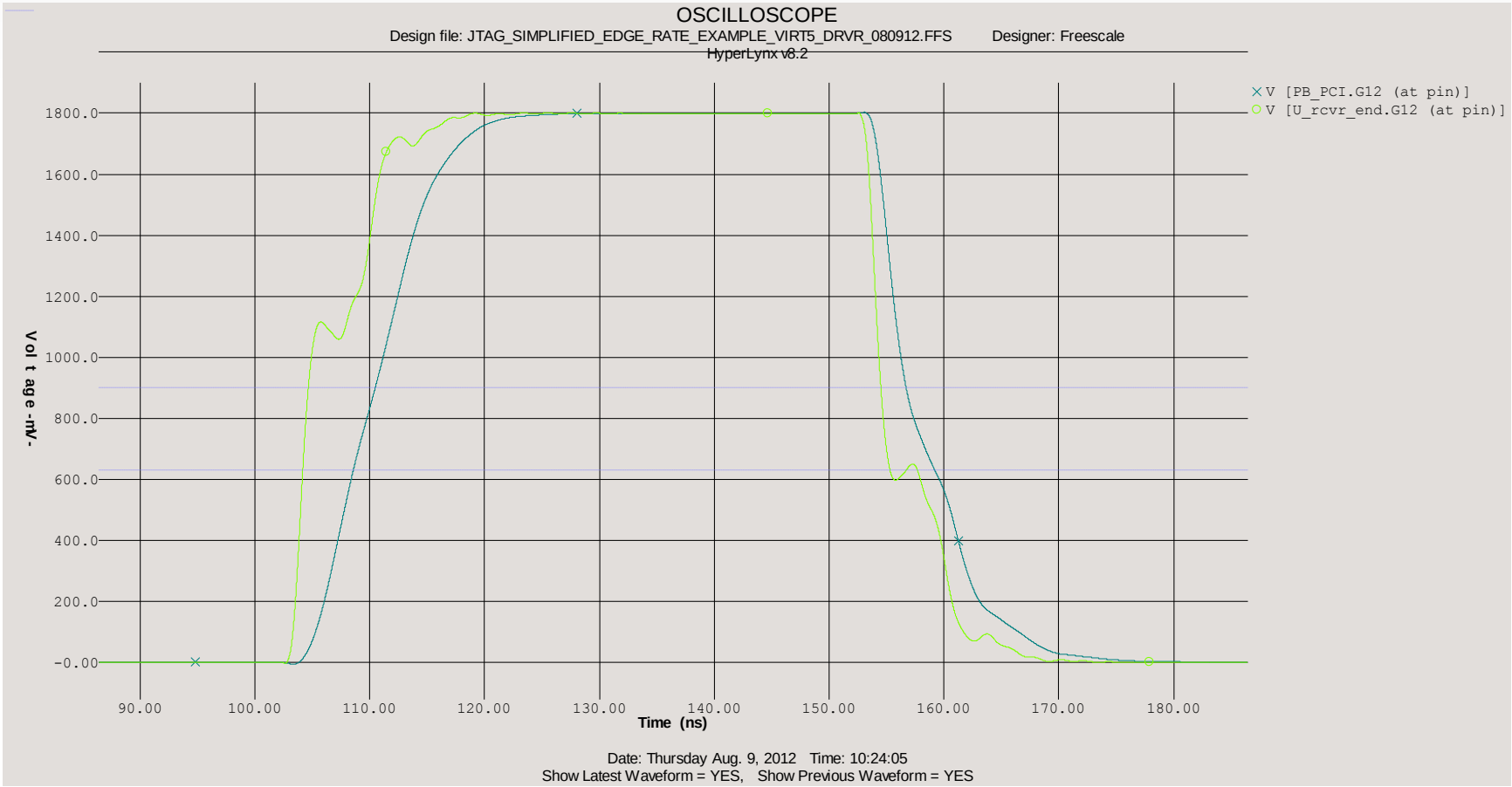
Faster Slow Edge Rate Daisy Chain



Compare Edge Rate Waveforms

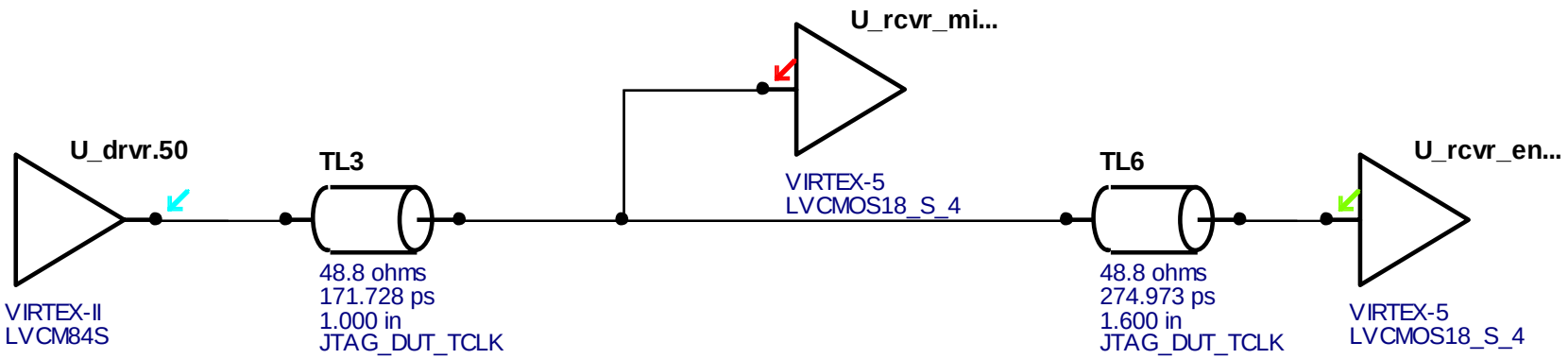


Compare Edge Rate Waveforms

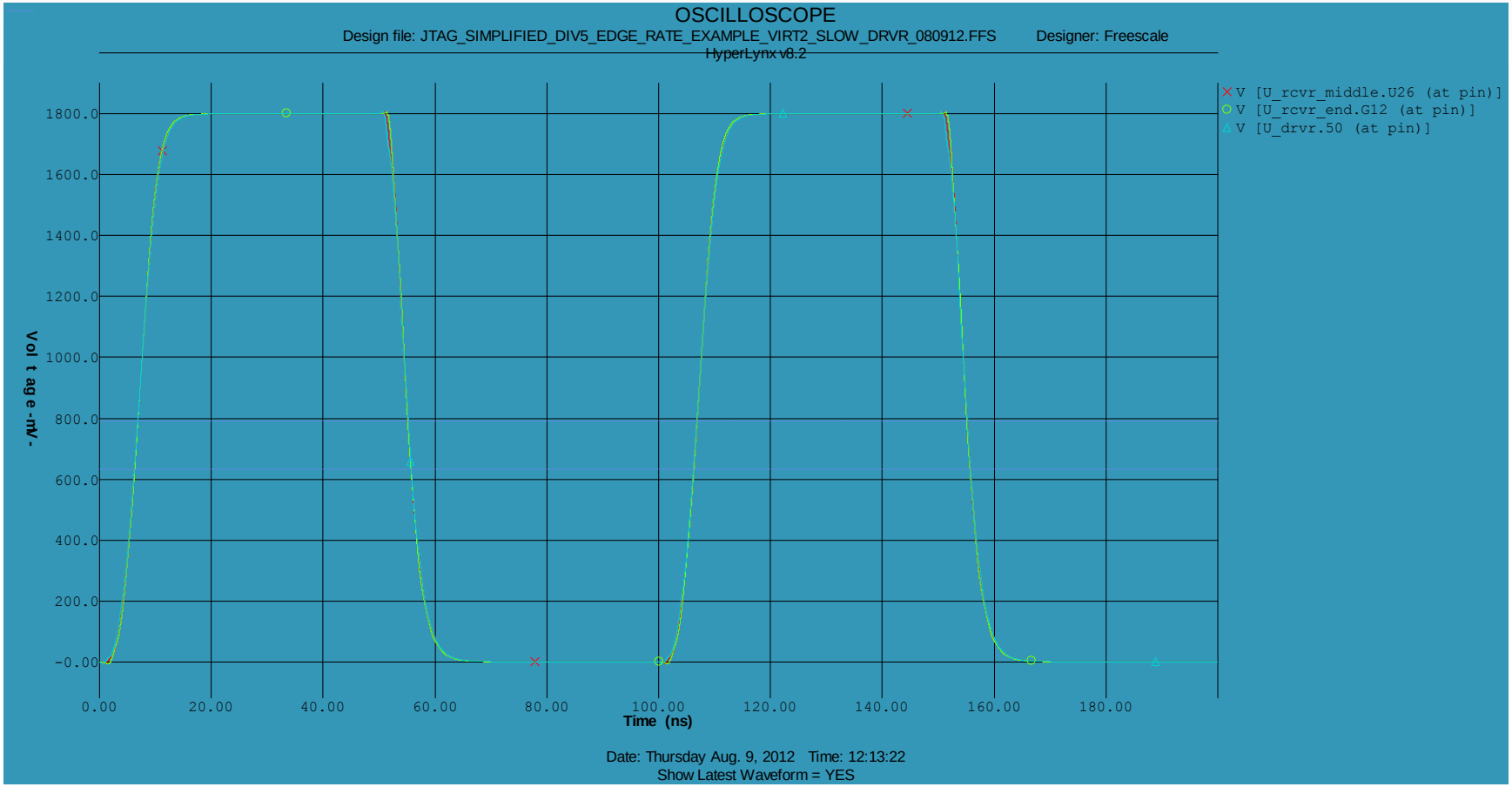


Shorten lengths: Slow Driver

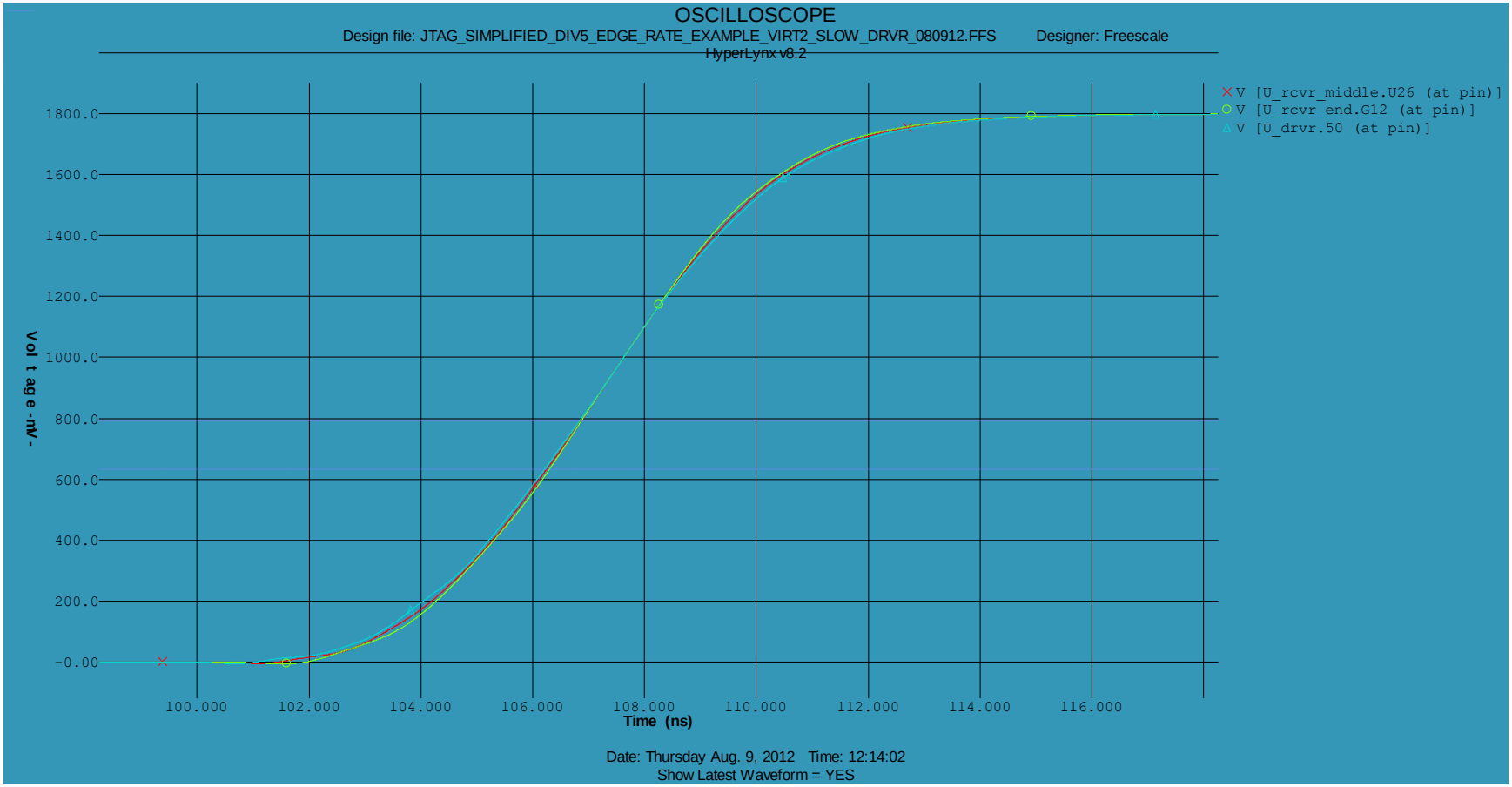
Design File: JTAG_simplified_clv5_edge_rate_example_virt2_slow_drvr_080912.ffs
HyperLynx LineSim v8.2



Shorten lengths: Slow Driver

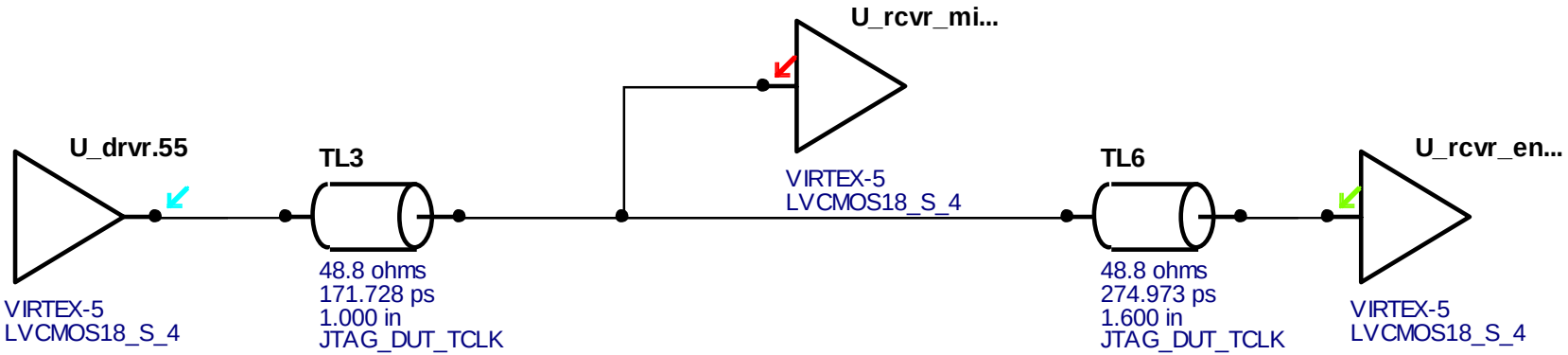


Shorten lengths: Slow Driver

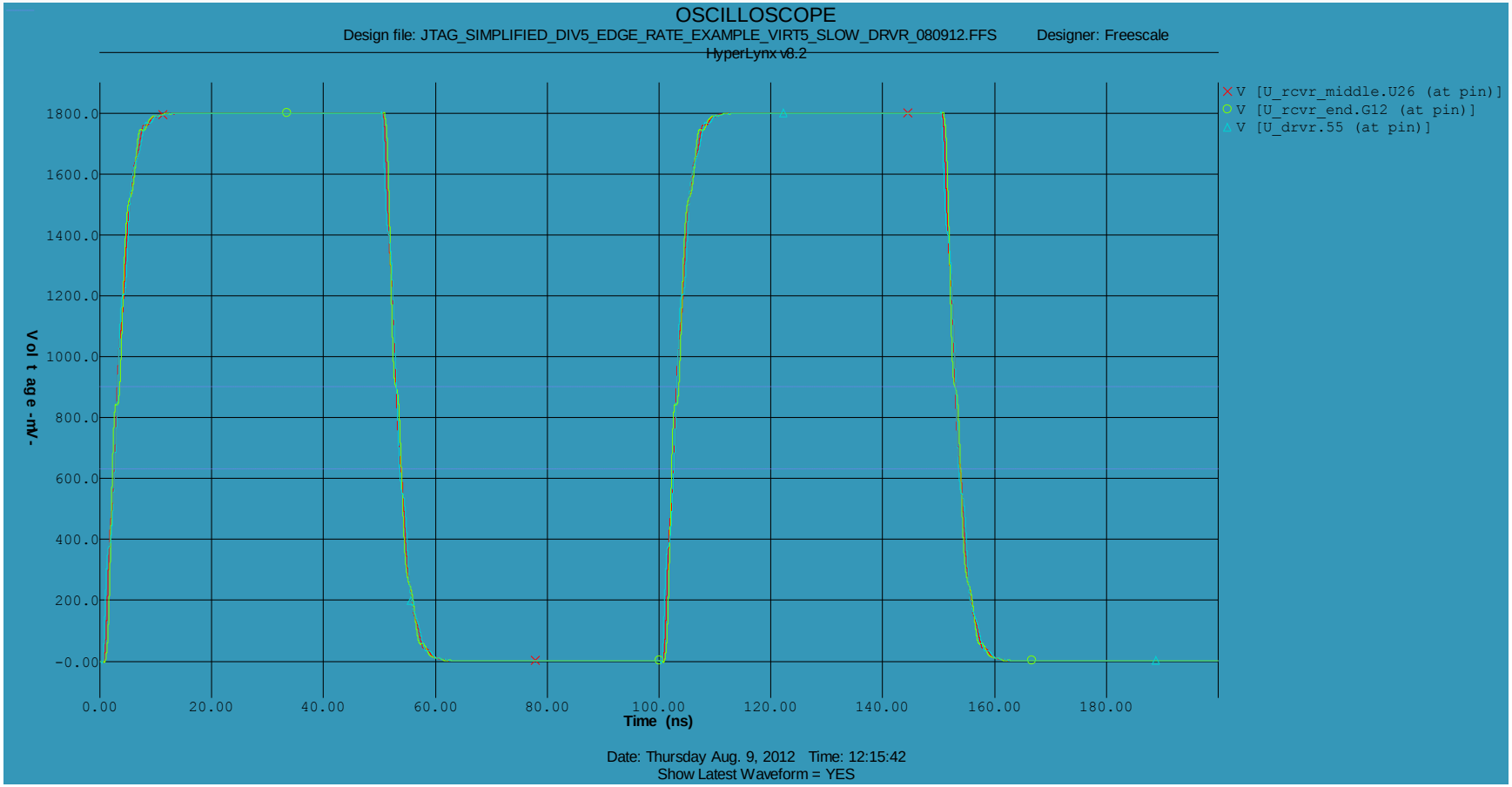


Shorten lengths: Faster Slow Driver

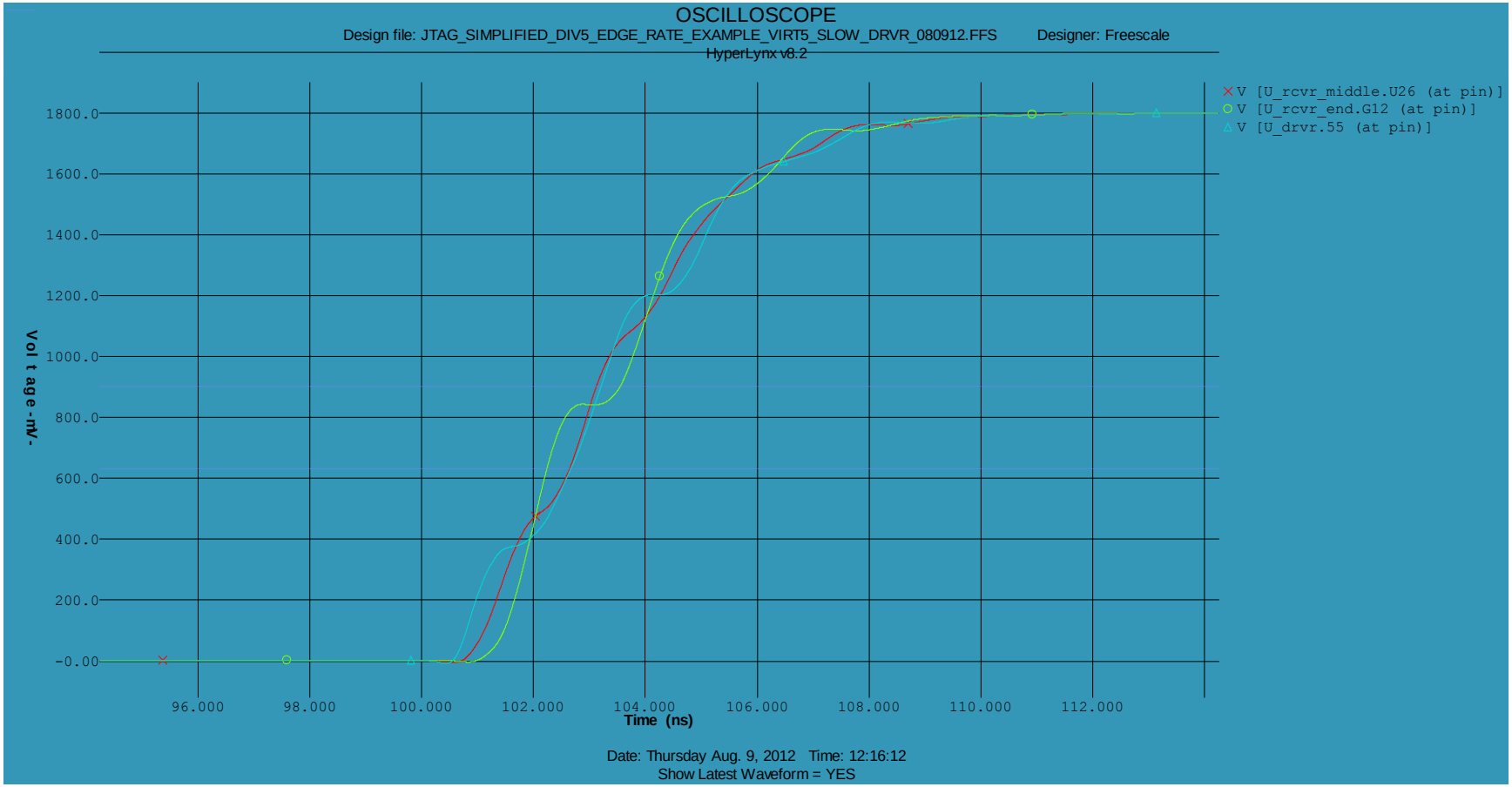
Design File: JTAG_simplified_dv5_edge_rate_example_virt5_slow_drvr_080912.ffs
HyperLynx LineSim v8.2



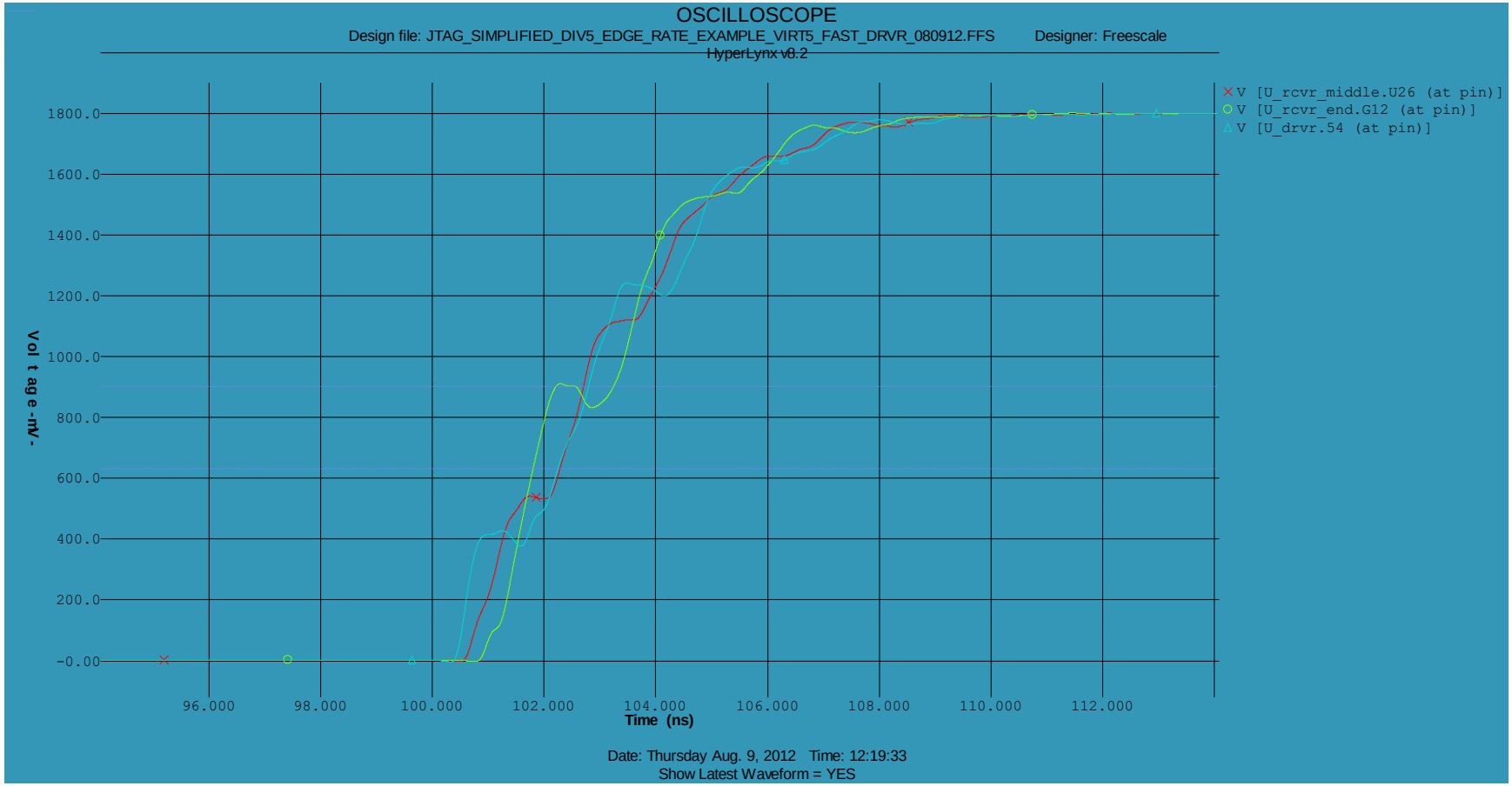
Shorten lengths: Faster Slow Driver



Shorten lengths: Faster Slow Driver

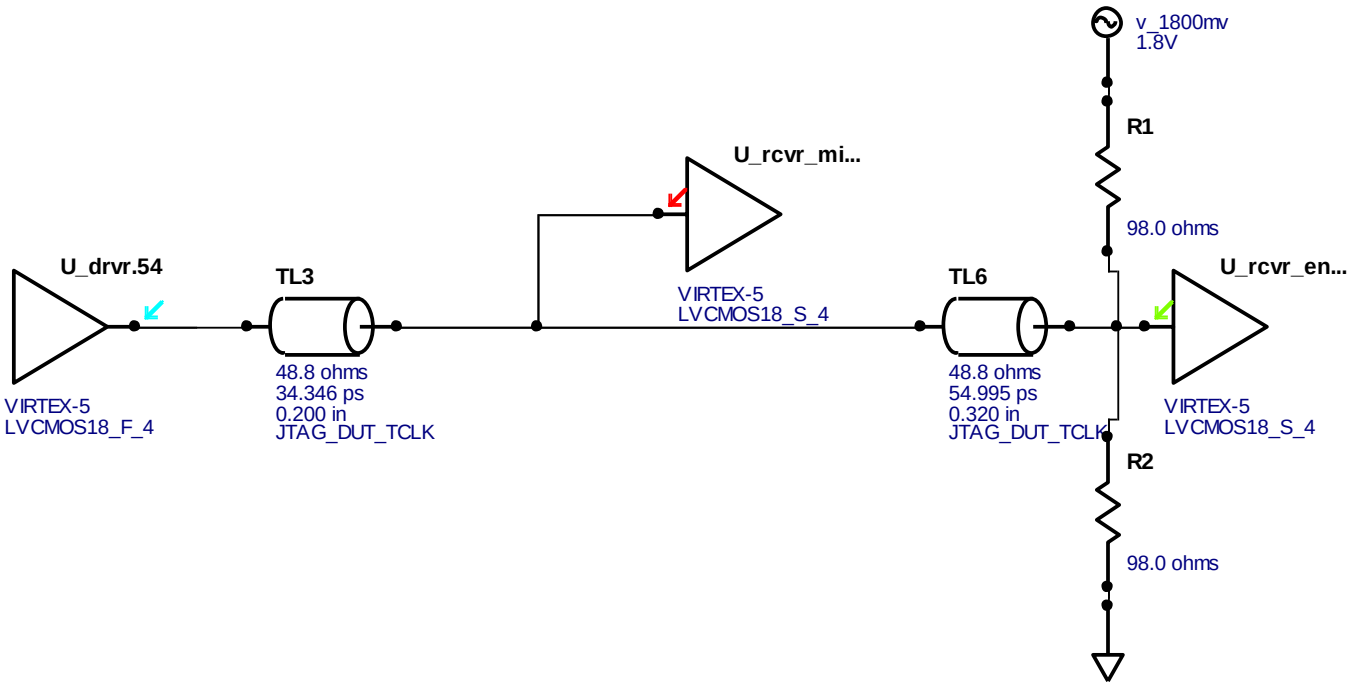


Shorten lengths: Fast Driver

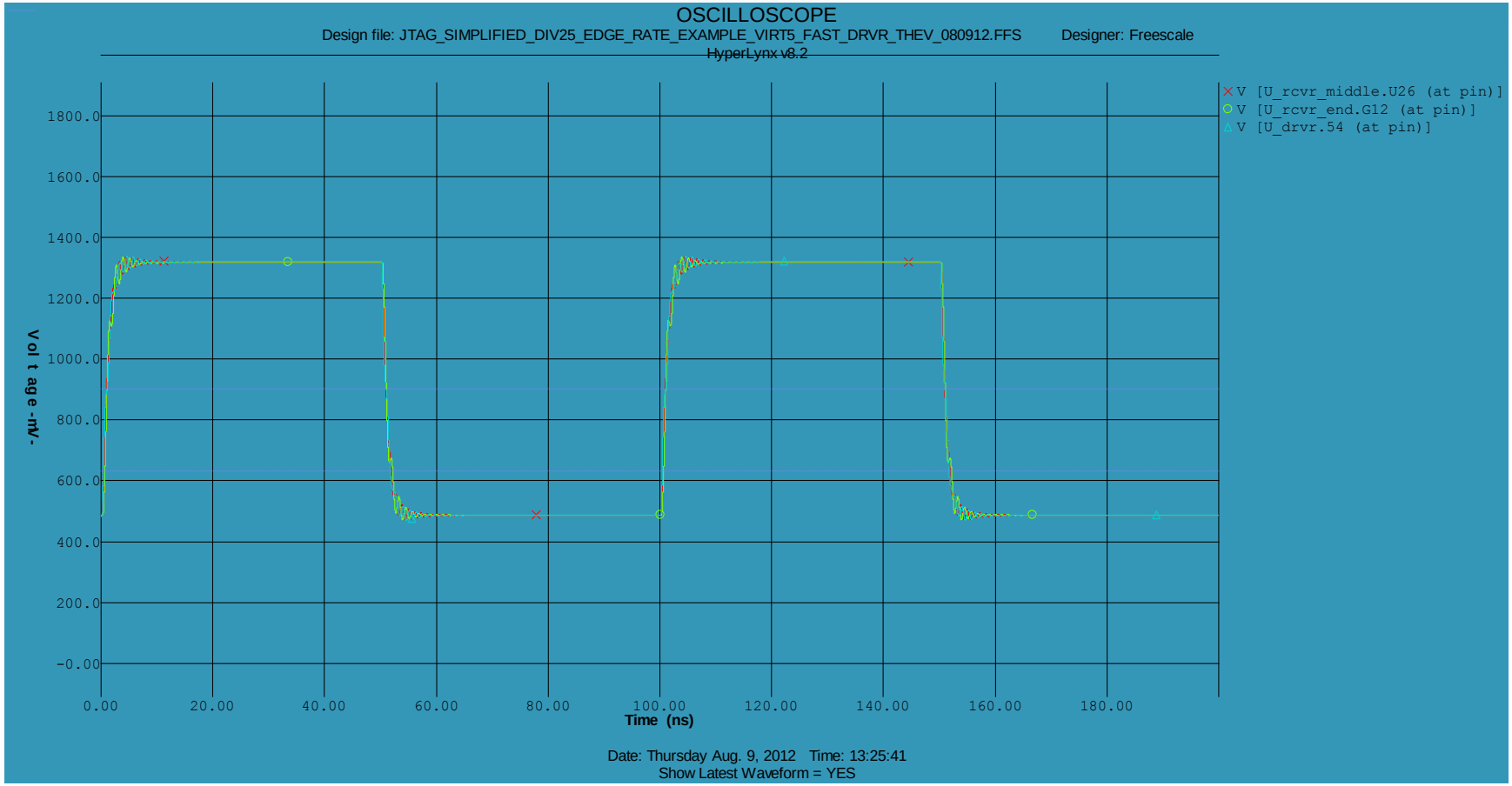


Shorten lengths & Use Thevenin Termination: Fast Driver

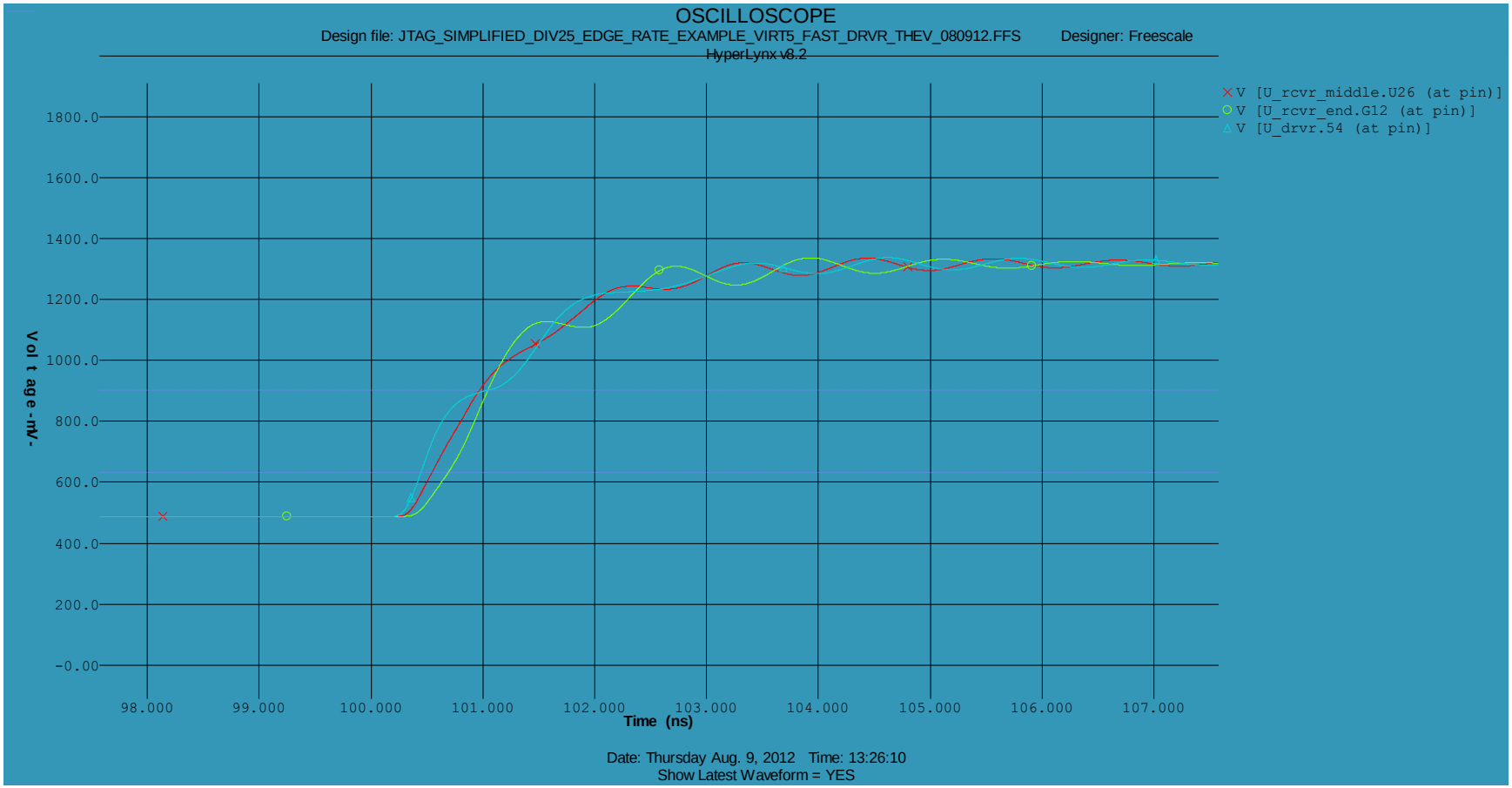
Design File: JTAG simplified_dv25_edge_rate_example_virt5_fast_dvr_thev_080912.ffs
HyperLynx LineSim v8.2



Shorten lengths & Use Thevenin Termination: Fast Driver

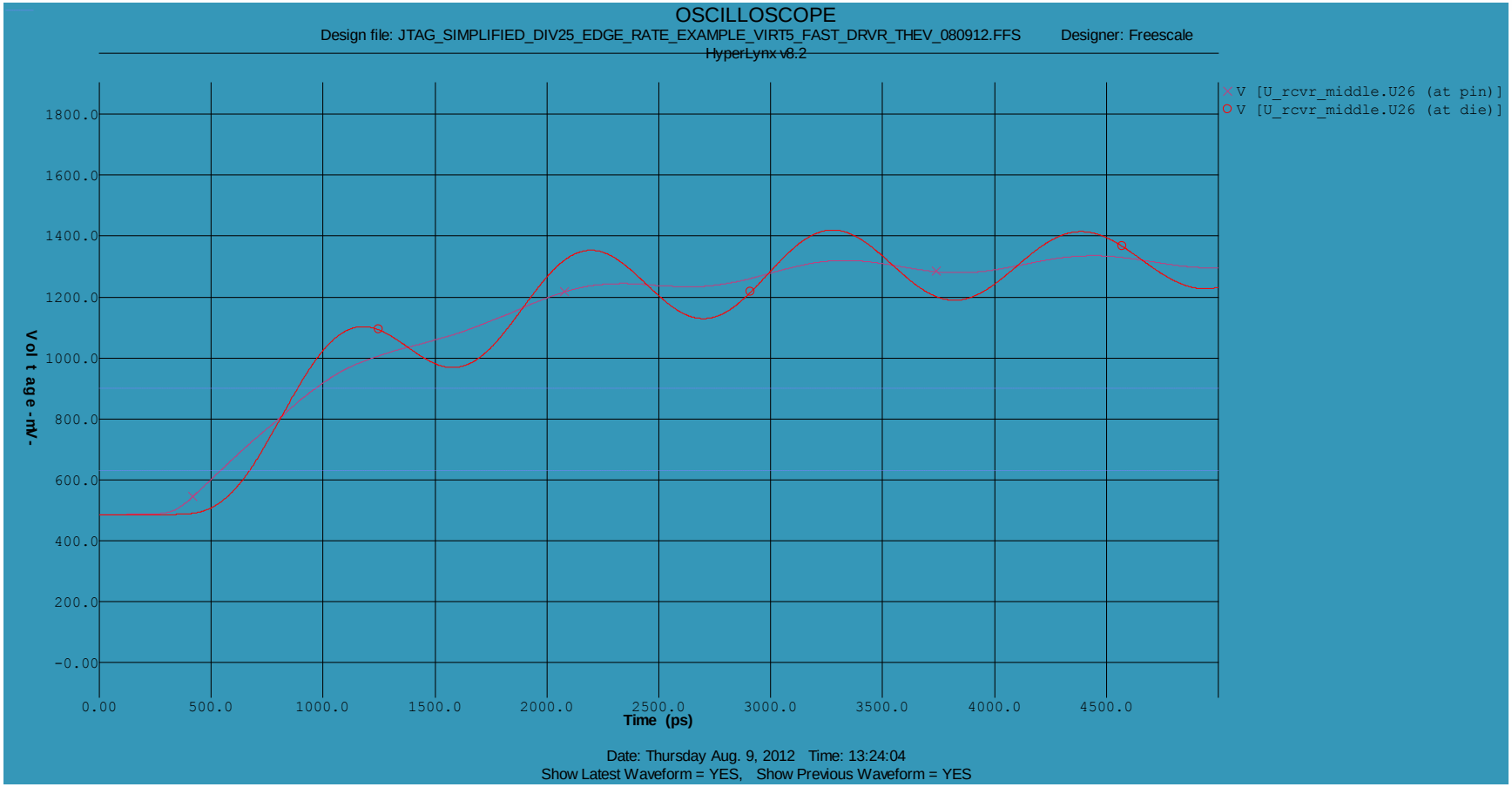


Shorten lengths & Use Thevenin Termination: Fast Driver



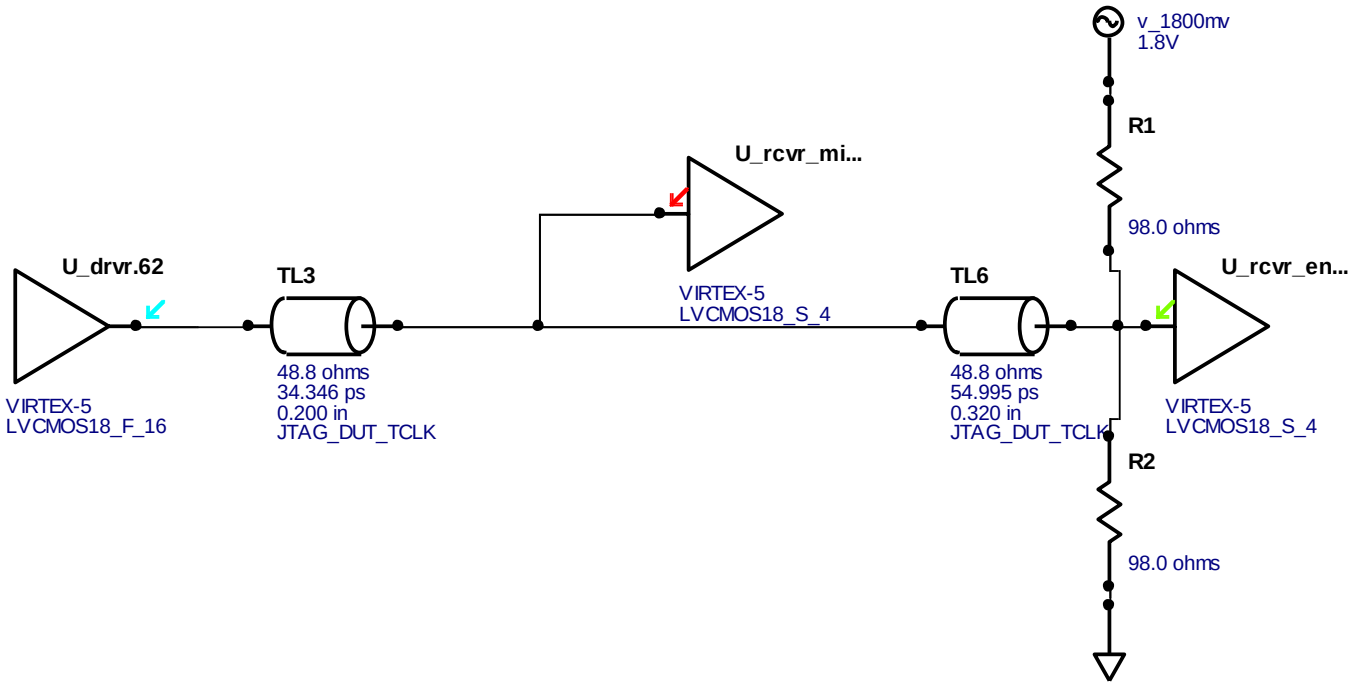
horten lengths & Use Thevenin Termination: Fast Driver

→ Edge is better but swing is too narrow with sampling point at ~ Ovdd/2

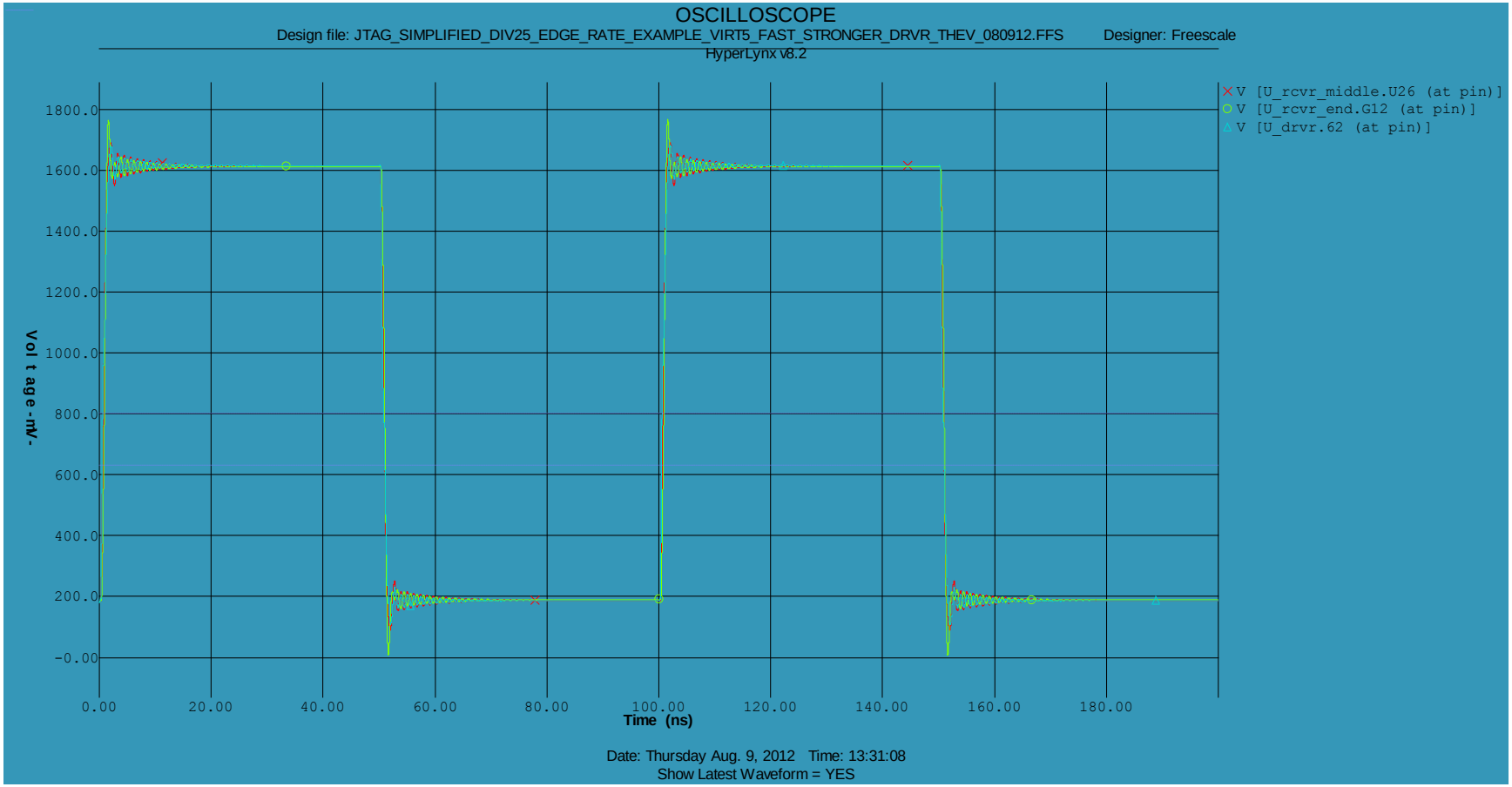


Shorten lengths & use Thevenin Termination: Stronger Fast Driver

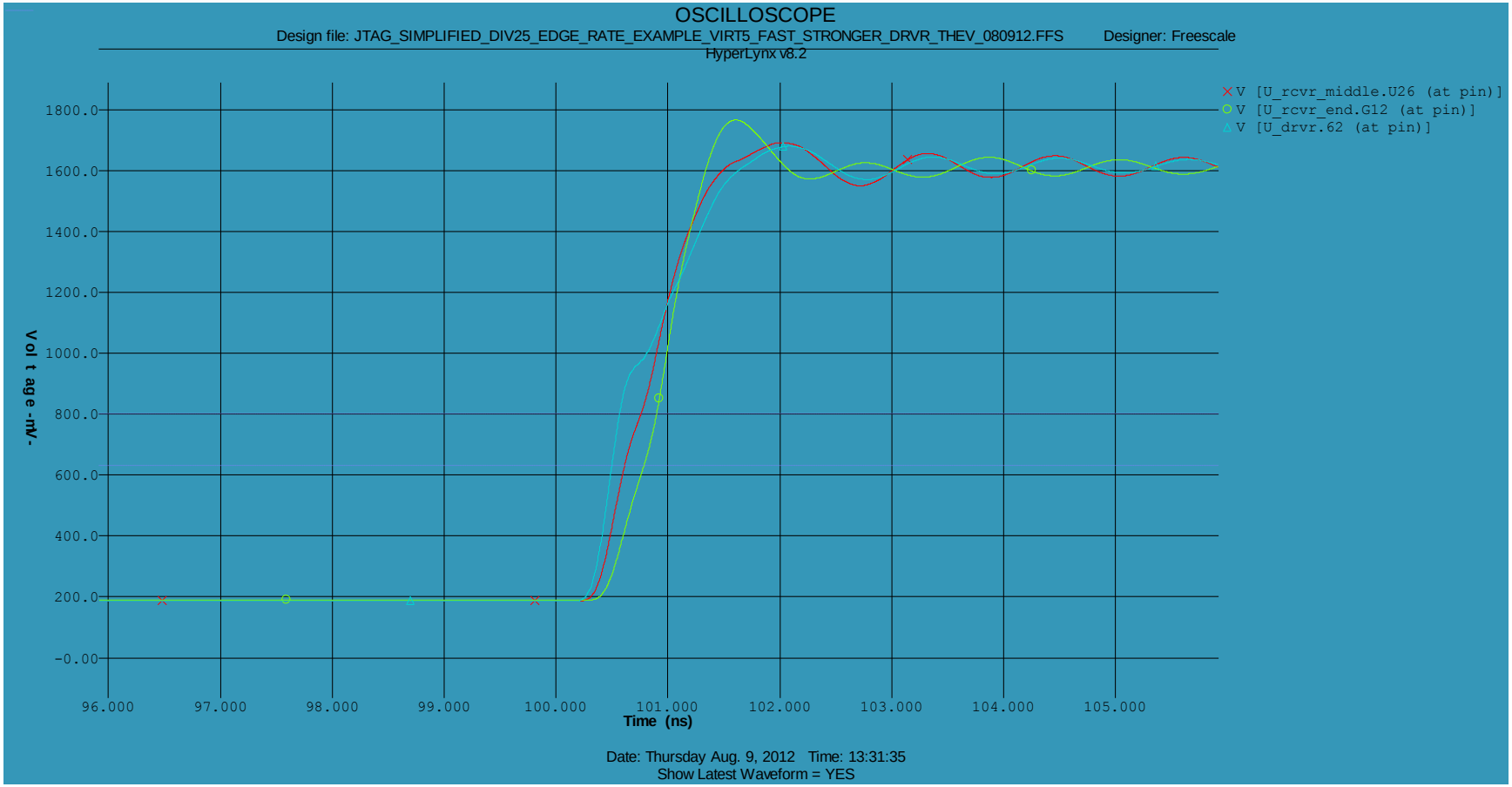
Design File: JTAG simplified_dlv25_edge_rate_example_virt5_fast_stronger_drvr_thev_080912.ffs
HyperLynx LineSim v8.2



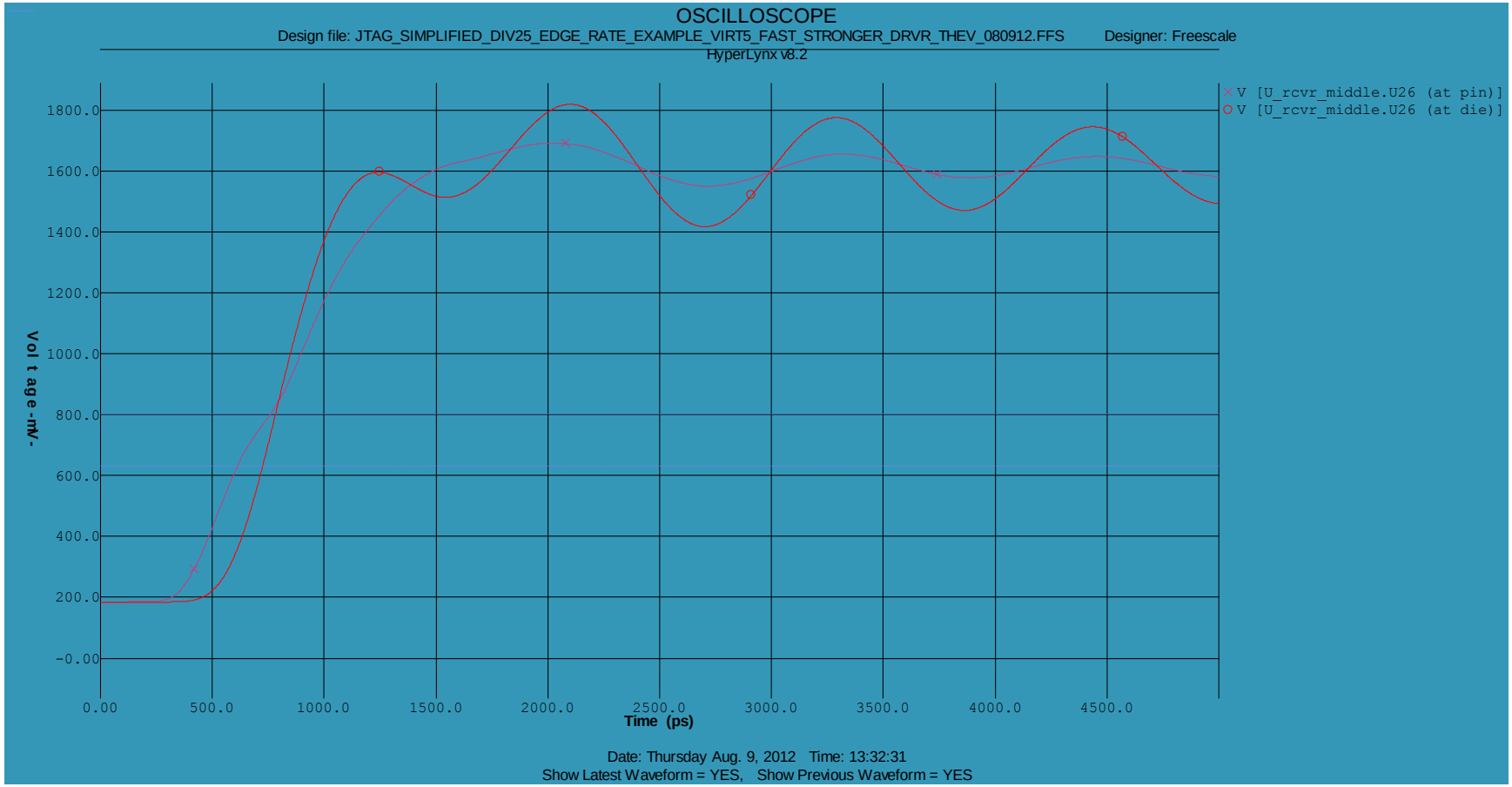
Shorten lengths & use Thevenin Termination: Stronger Fast Driver



Shorten lengths & use Thevenin Termination: Stronger Fast Driver

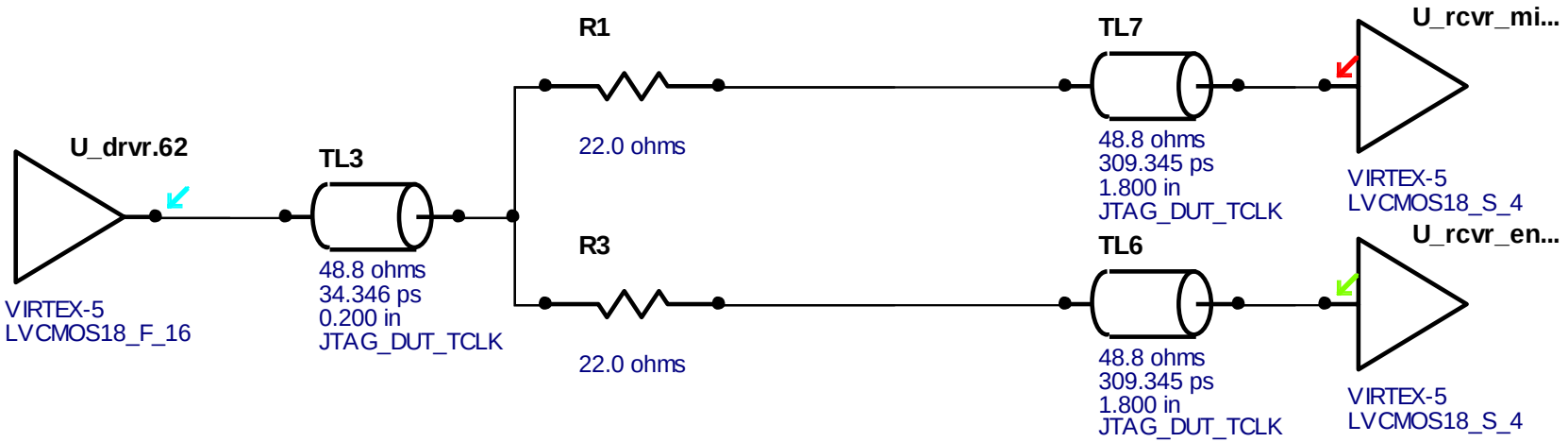


Shorten lengths & use Thevenin Termination: Stronger Fast Driver → Edge is good & Swing is good now

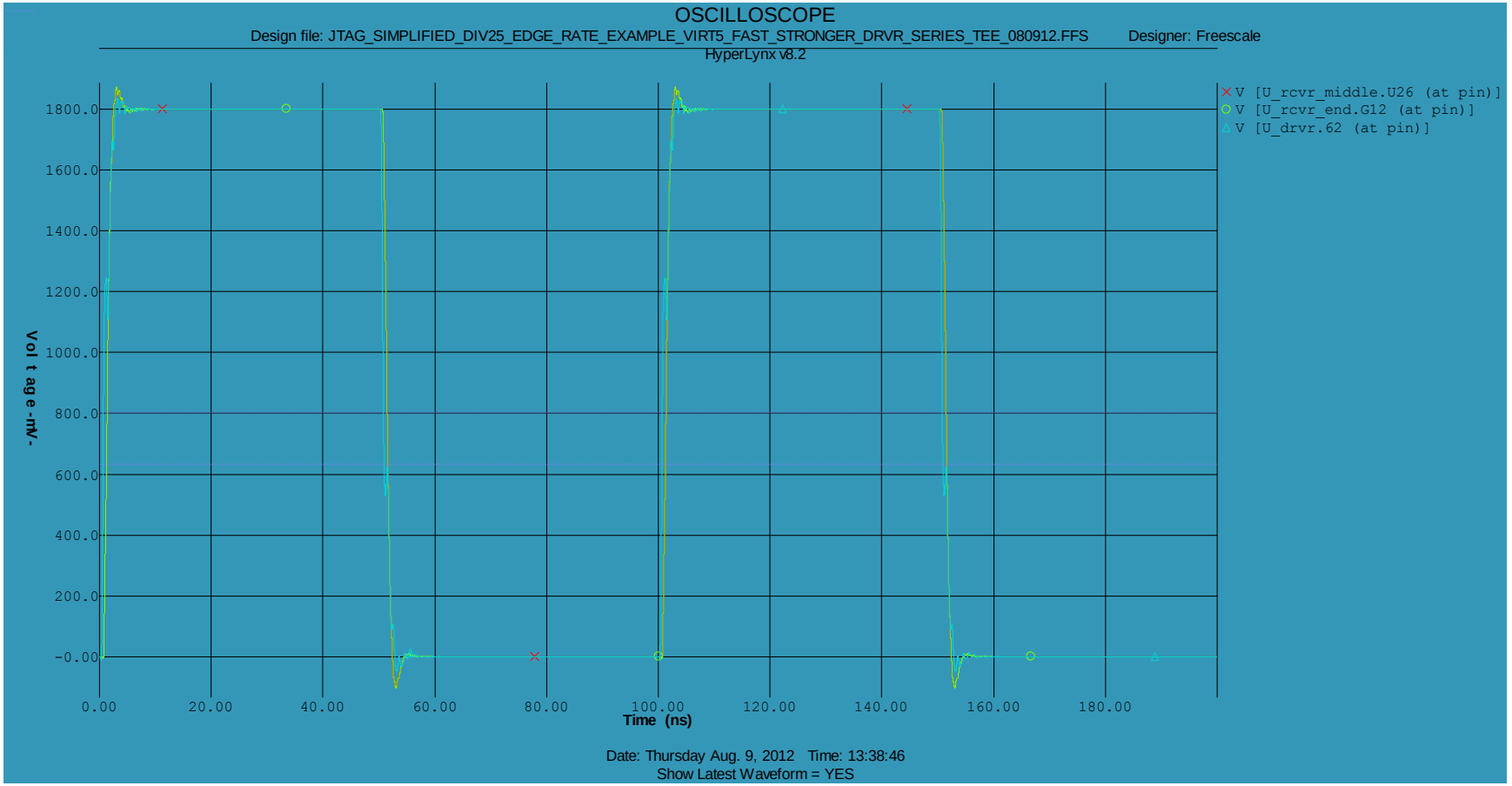


Shorten lengths & use Series Termination and Tee Route

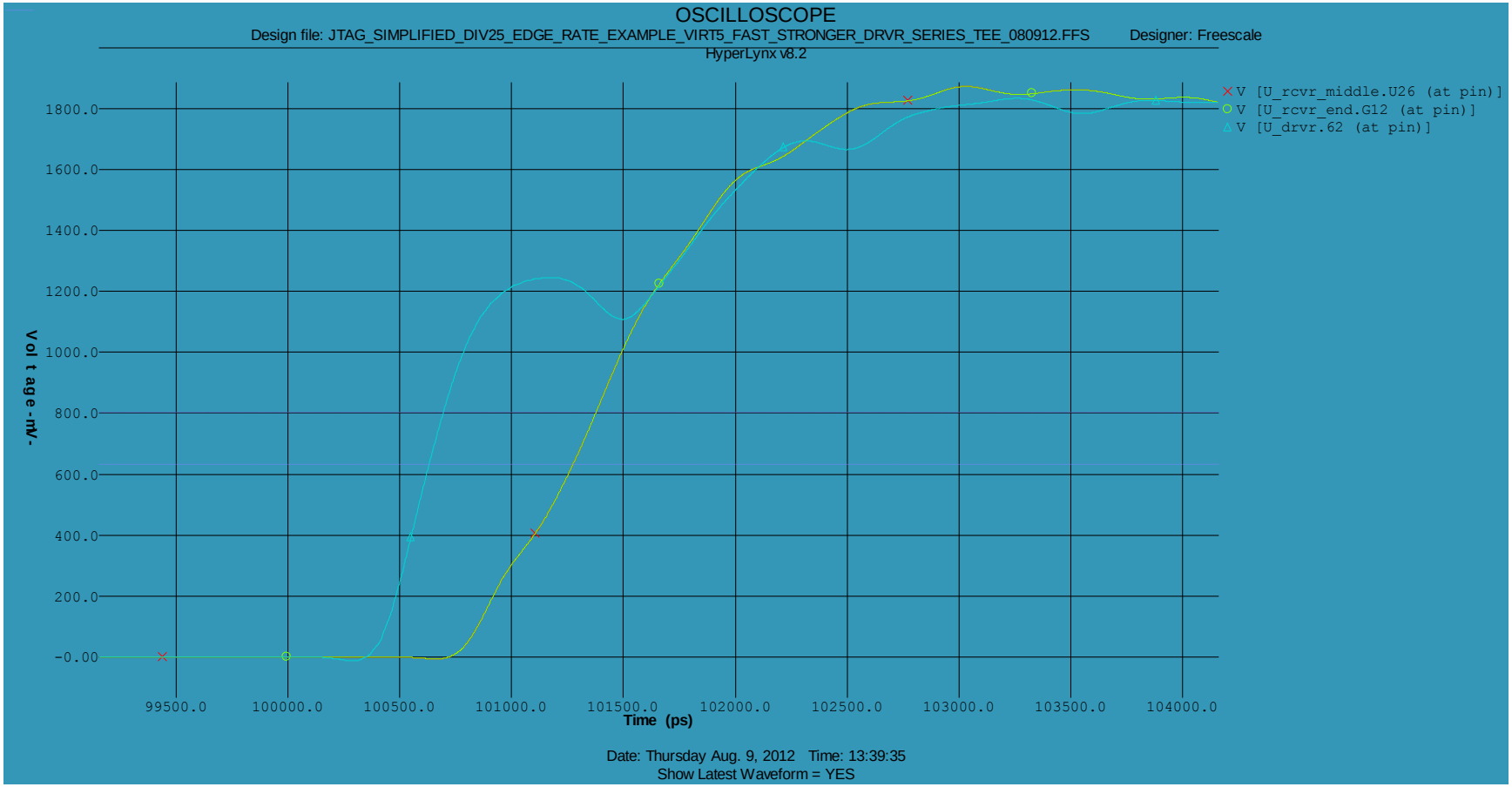
Design File: JTAG_simplified_dlv25_edge_rate_example_virt5_fast_stronger_dlvr_series_tee_080912.ffs
HyperLynx LineSim v8.2



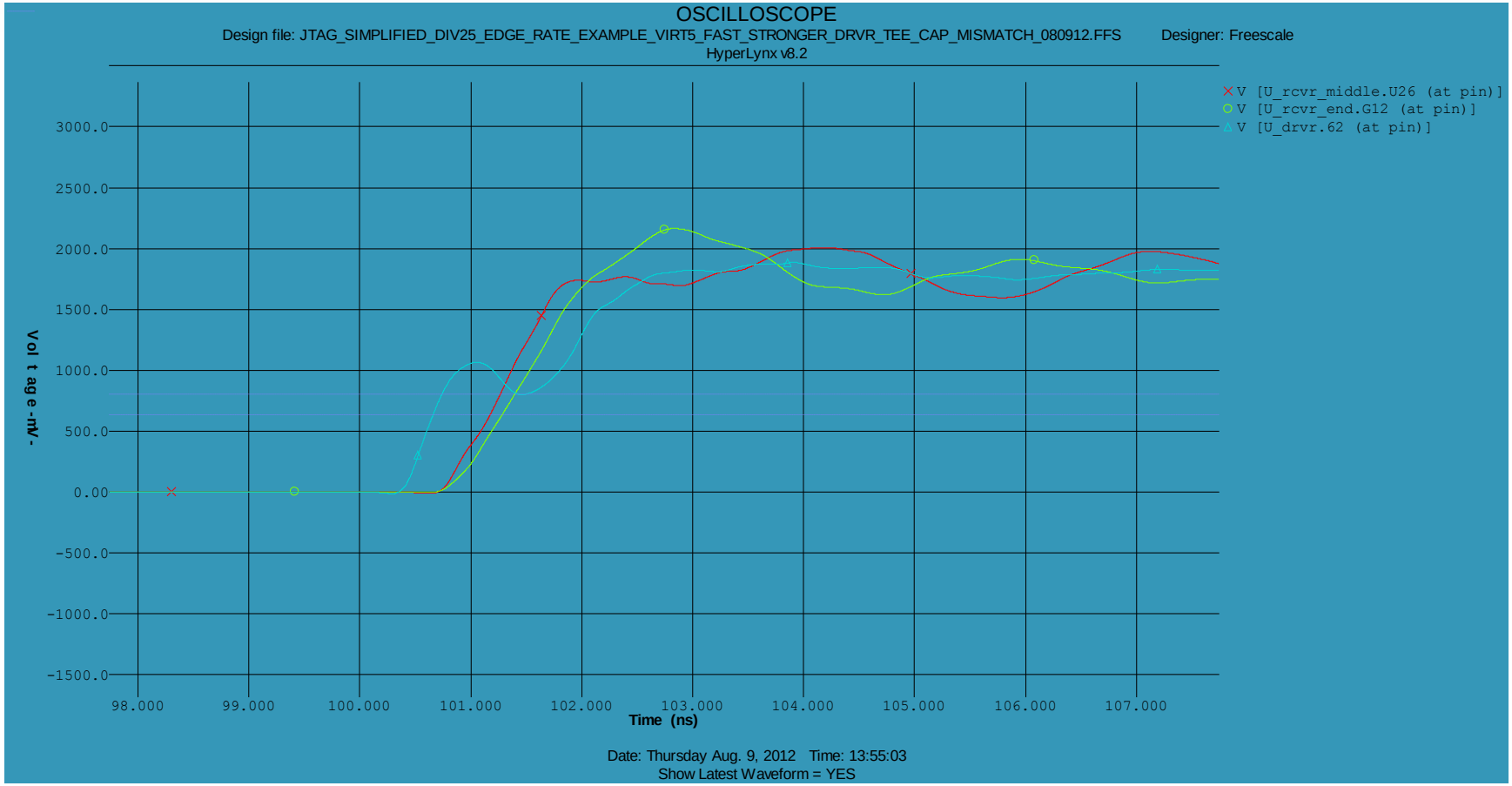
Shorten lengths & use Series Termination and Tee Route



Shorten lengths & use Series Termination and Tee Route



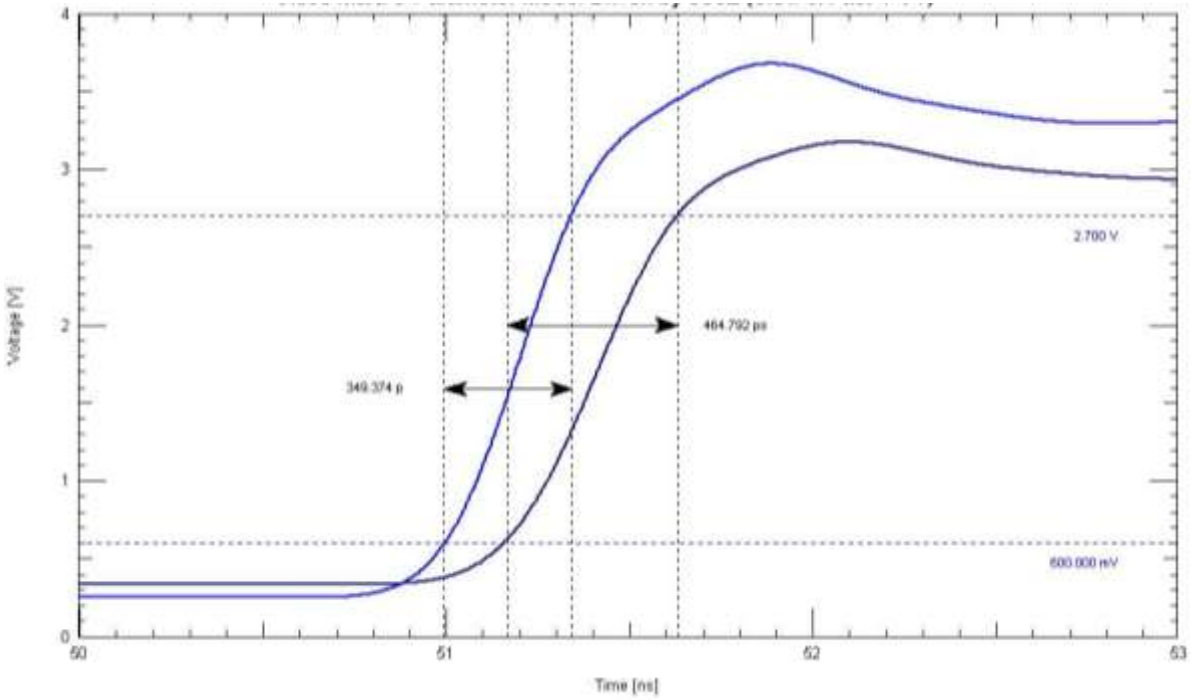
Shorten lengths & use Series Termination and Tee Route: → Unequal Loads cause skew; be careful for timing



2) SYSCLK Input Edge Rate

SYSCLK Simulation

- Simulate Various Clock Drivers
  - Do the Clock Drivers meet the HW spec values for the SYSCLK spec?
  - Look at Edge Rate at CPU.
  - Look at Fast and Slow Corners for Clock Driver and CPU SYSCLK input from IBIS models.



3) Die vs Pin Probing for Read (incoming/receive) Waveforms

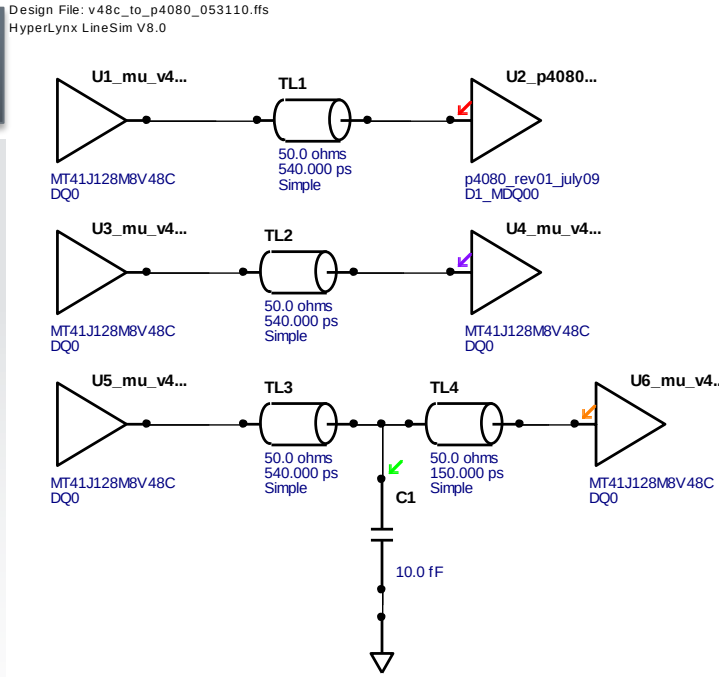
Signal Integrity FAQ: Die vs Pin Probing

- Especially an issue for signals into CPUs
- Large package sizes create longer transmission lines/delays
- Reflection from end of transmission line will distort signal not at end of transmission line

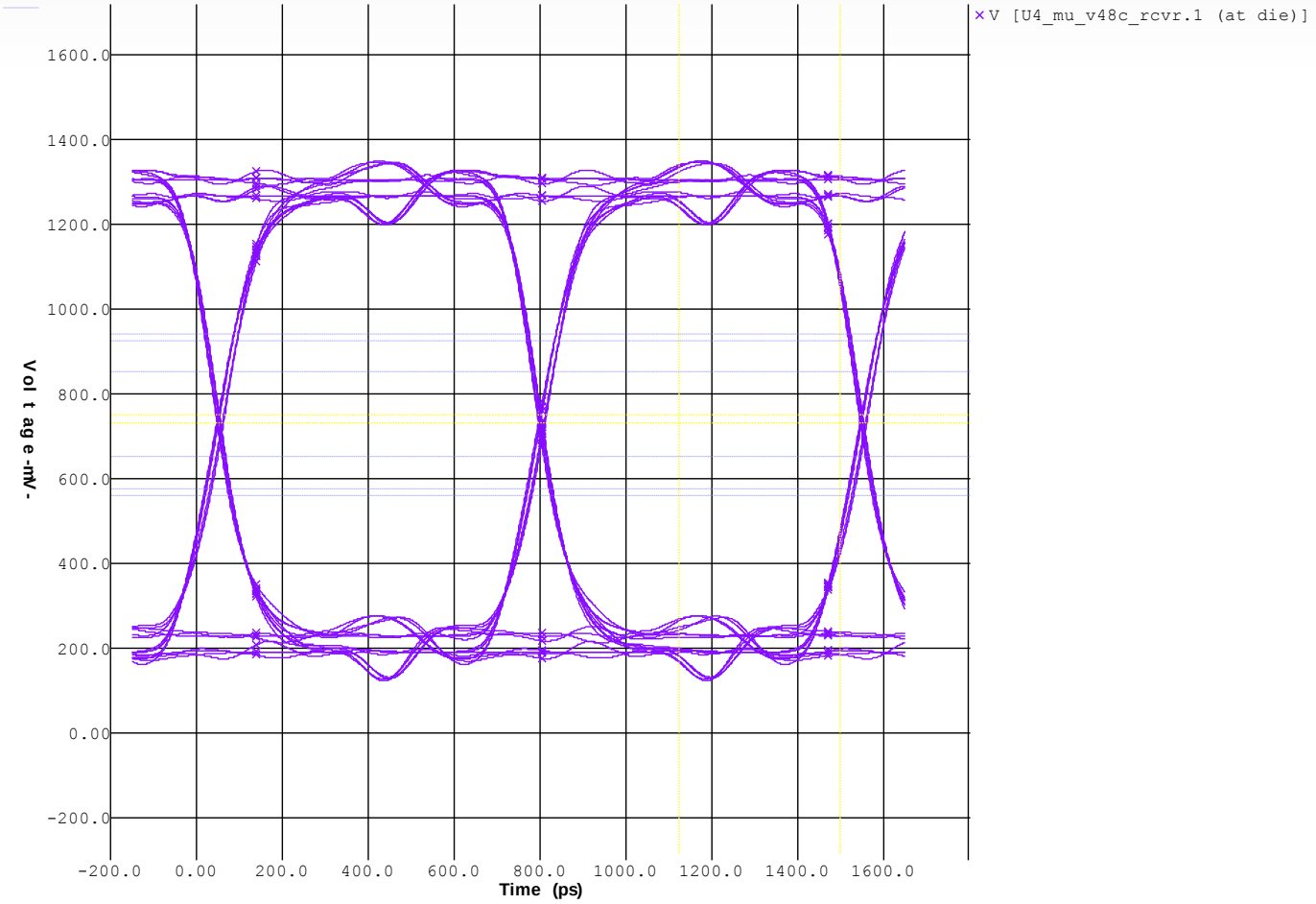
Die vs Pin Simulation Example

Die vs Pin

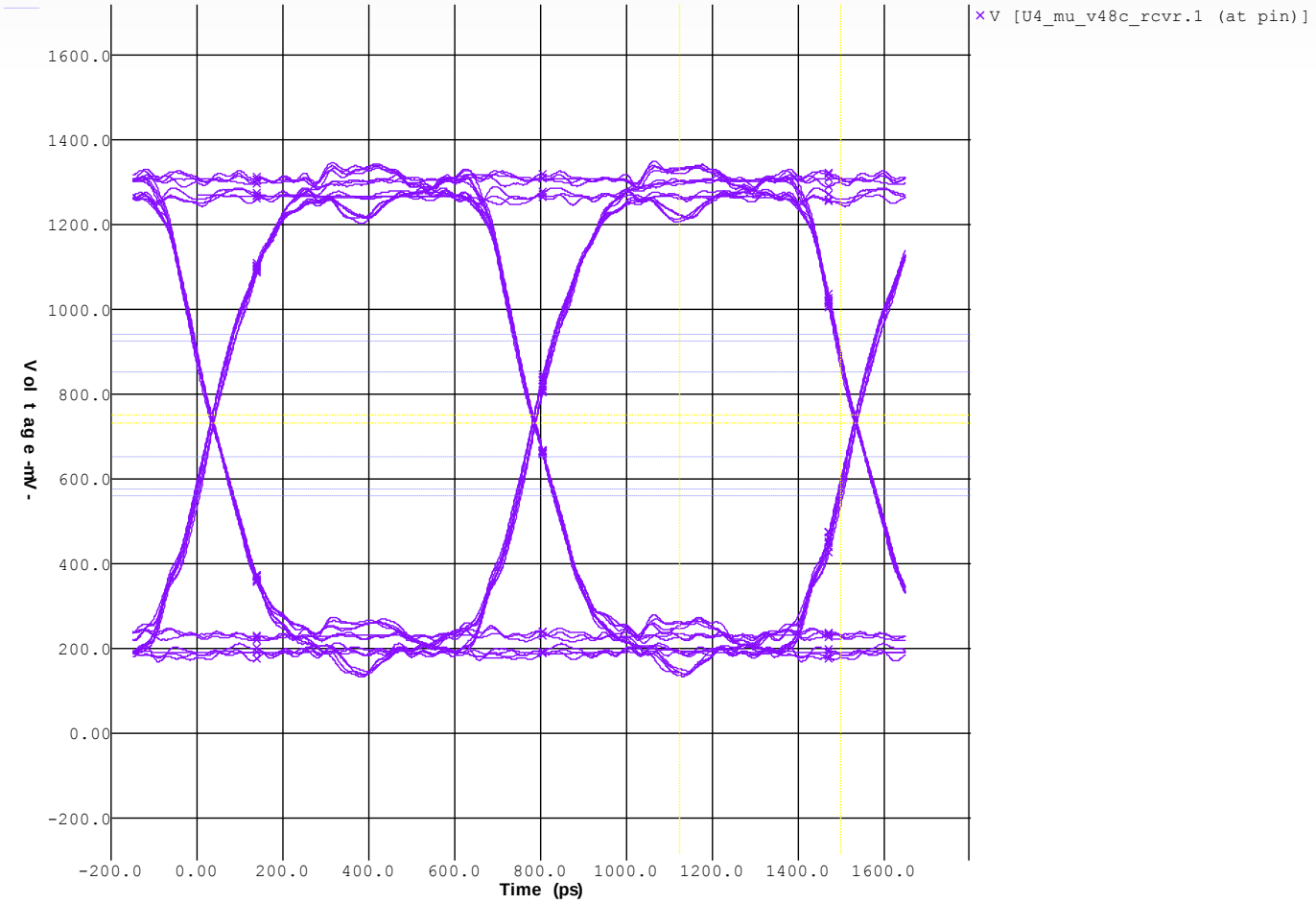
- Top is Memory to P4080
- Middle is Memory to Memory
- Bottom is Memory to Memory with probe point 150ps from end of net
- Purpose is to test effect of P4080 package probe point at pin vs die
  - P4080 package electrical length is approx 150 ps



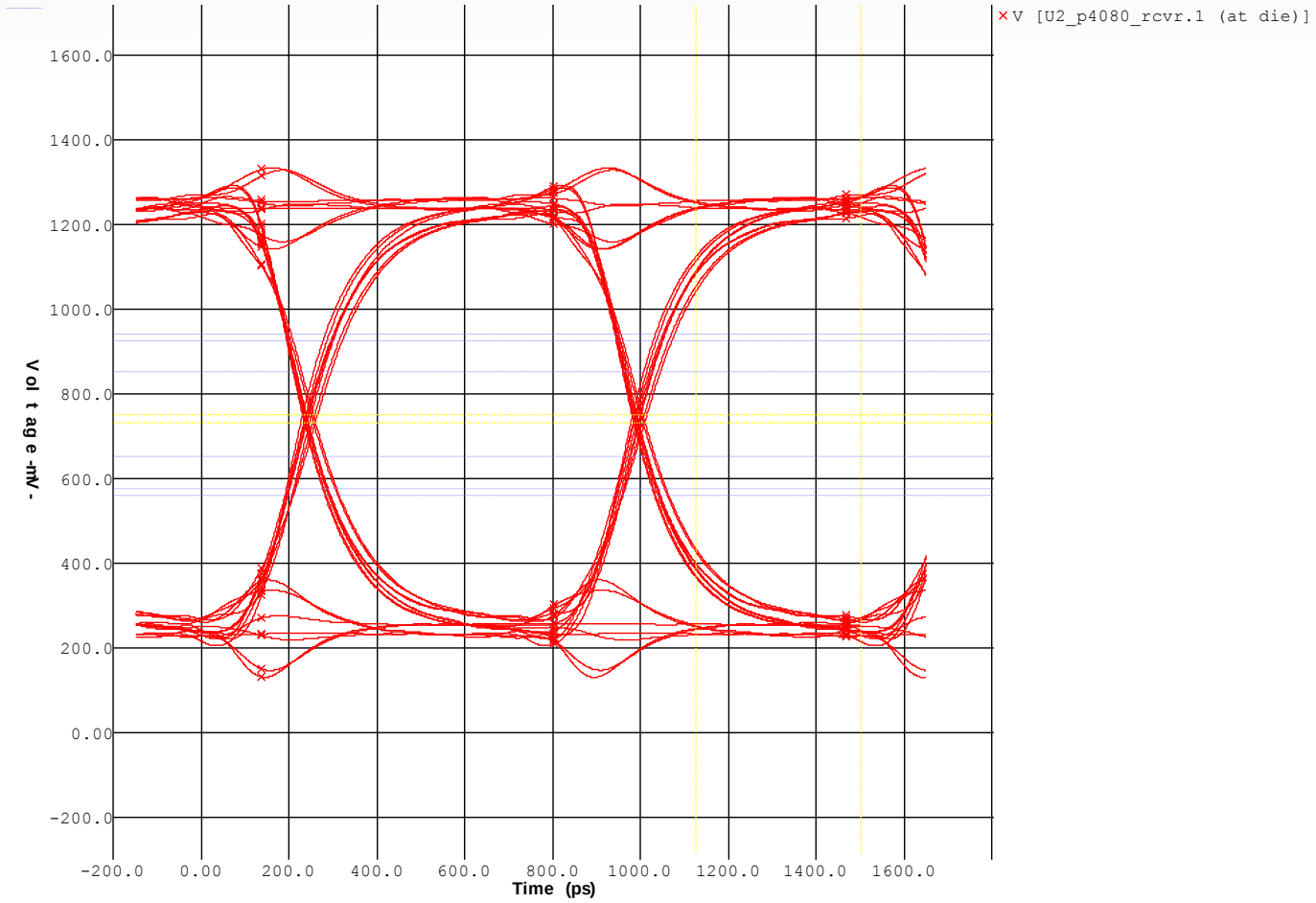
Read Waveform Measured at Memory Die



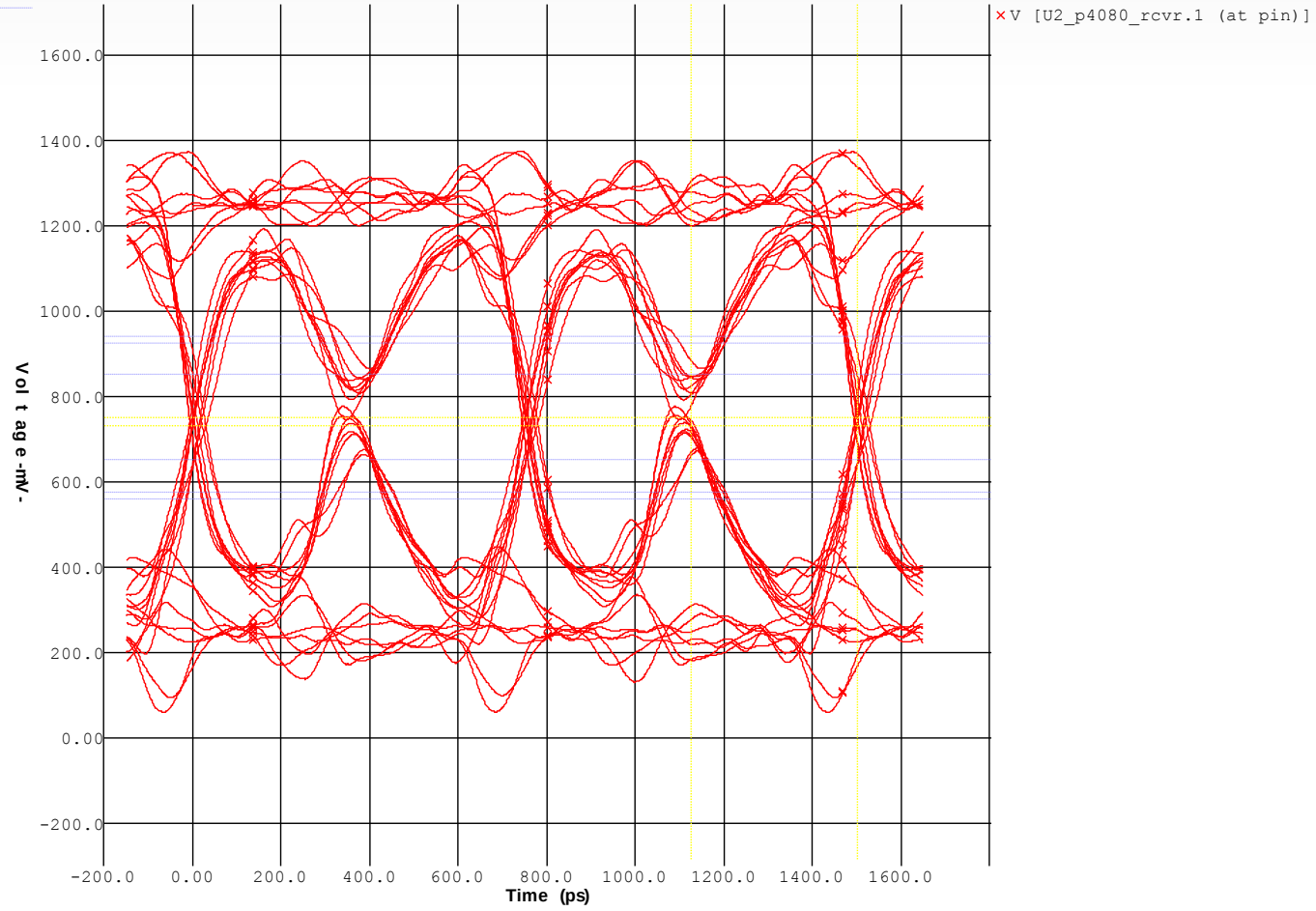
Read Waveform Measured at Memory Pin



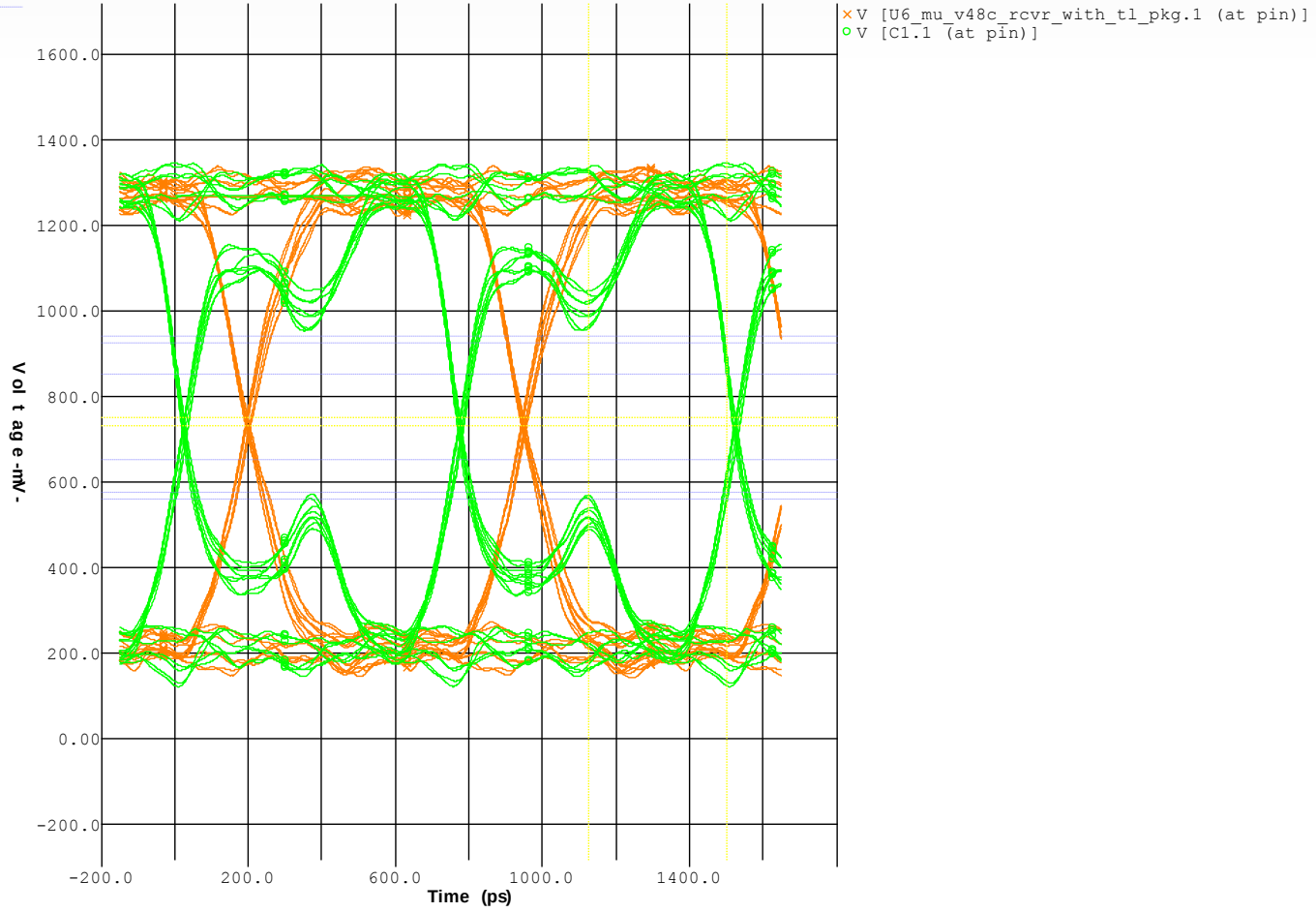
Read Waveform Measured at P4080 Die



Read Waveform Measured at P4080 Pin

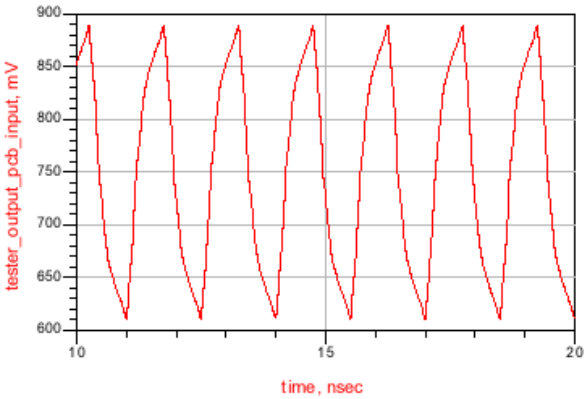


Read Waveform Measured at Memory Pin and 150 ps back from Memory Pin

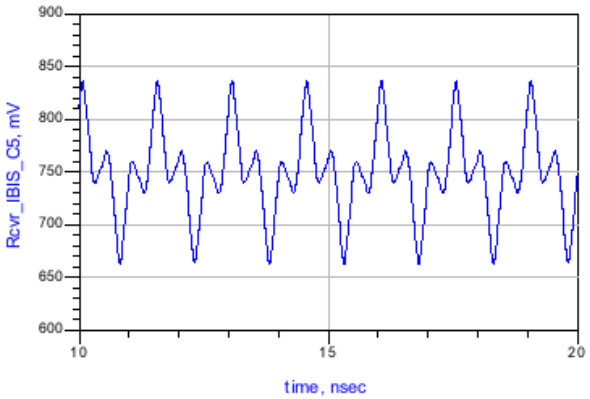


4) DDR Read Measurement

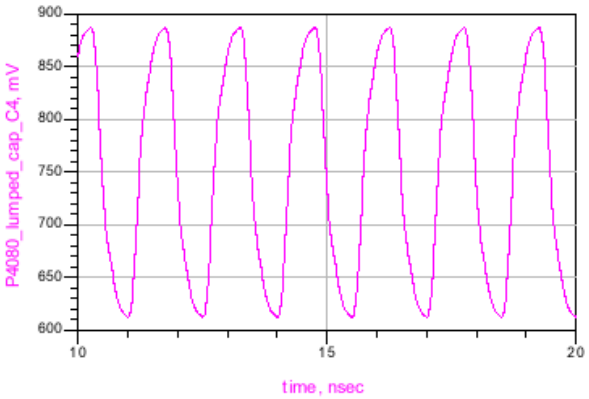
First Pass, Pre-Tuned Simulation Results For P4080 Receiver (No ODT) Inserted



Tester Output

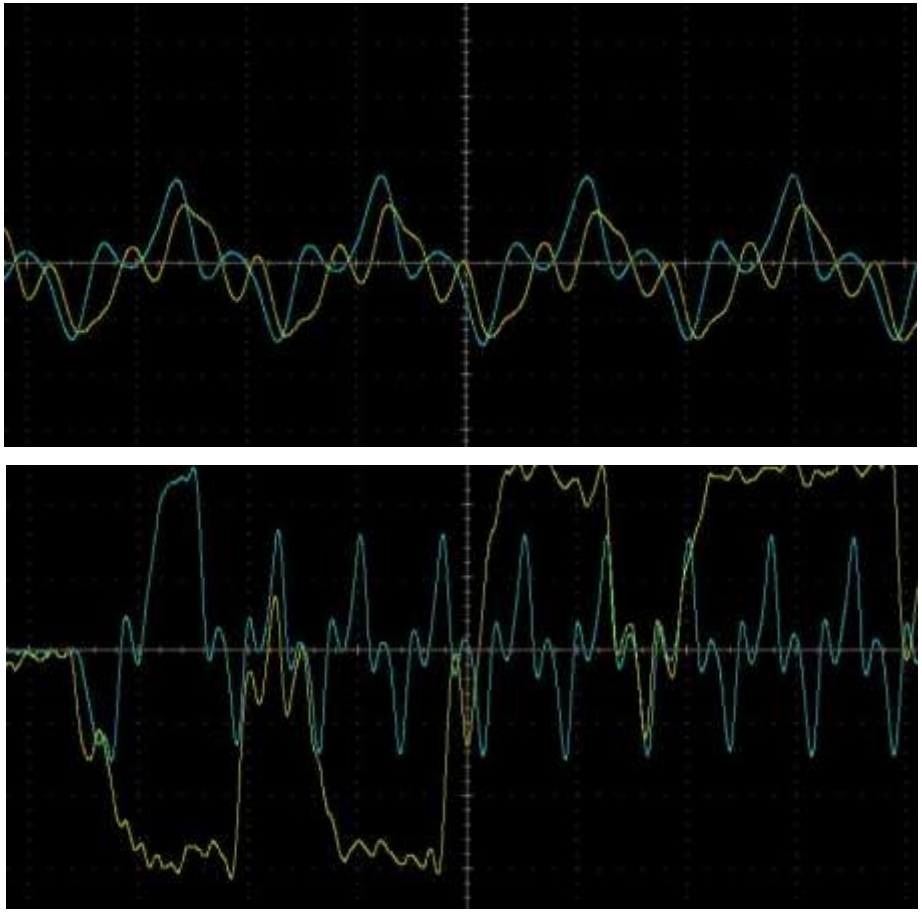


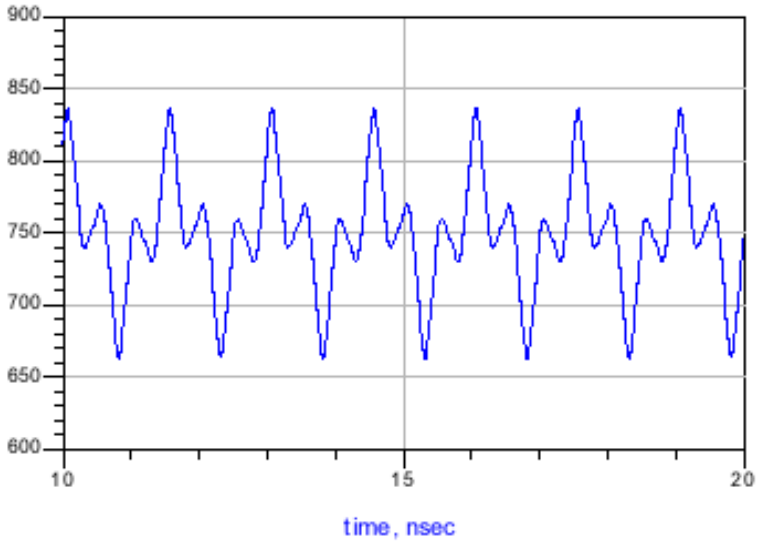
Receiver at Pin/C5



Receiver at Die/C4

Compare No ODT Measurement vs Simulated (Pre-Tuned)





5) DDR3-1866 Write Timing for Two DIMM System

DDR3-1866 Dual and Quad Ranked DIMM Plots

- Goal is to look at DDR3 write waveforms for DDR3-1866 to see if first or second DIMM slot shows better signal integrity behavior
  - Look at one dual-ranked, two dual-ranked, one quad-ranked DIMM options
- PCB is based on T4 QDS preliminary layout
  - 50 ohm PCB
  - 6 inch trace from CPU to first DIMM
- IO buffer models for CPU are P4080 and are not T4-based
- Comments:
  - A single dual-ranked DIMM shows improvement for using the second slot of two slots (farthest from CPU).
  - Two Dual Ranked or one Quad Ranked DIMM does not show as strong of a preference for first or second DIMM location from this set of simulations (with non-T4 models).

Data Eye Width vs Number and Type of DIMMs (Typ PVT) – Greater Numbers are better

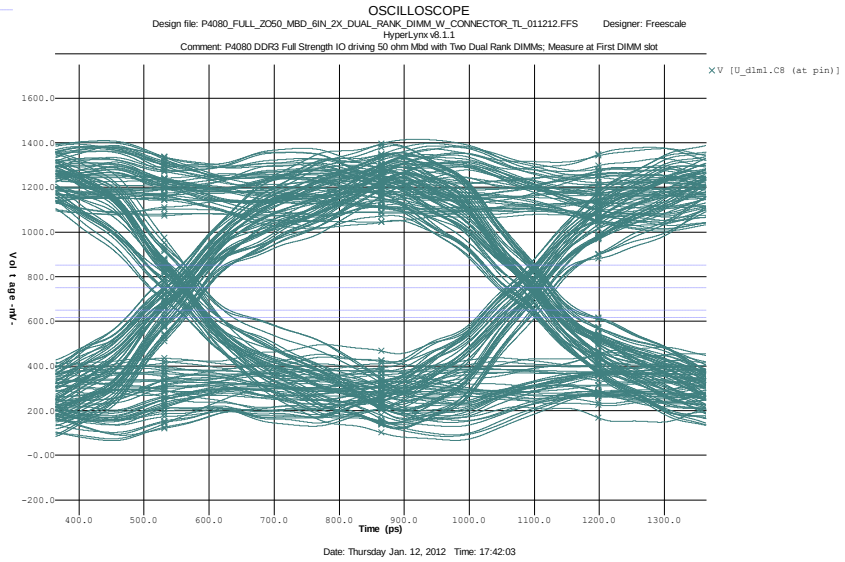
Read/Write	DIMM	#_DIMMs	Slot	Data Eye Width at AC-DC Vin Levels (Ave High & Low Vin - ps)
Write	Dual Rank	1	2	426
Read	Dual Rank	1	2	399.5
Read	Dual Rank	2	2	354.5
Read	Dual Rank	2	1	351
Write	Dual Rank	2	2	350.5
Write	Dual Rank	2	1	346.5
Write	Quad Rank	1	2	334
Write	Dual Rank	1	1	332
Read	Dual Rank	1	1	305.5
Write	Quad Rank	1	1	285.5
Read	Quad Rank	1	2	234.5
Read	Quad Rank	1	1	234

Data Eye Width vs Number and Type of DIMMs
(Slow PVT) – Greater Numbers are better

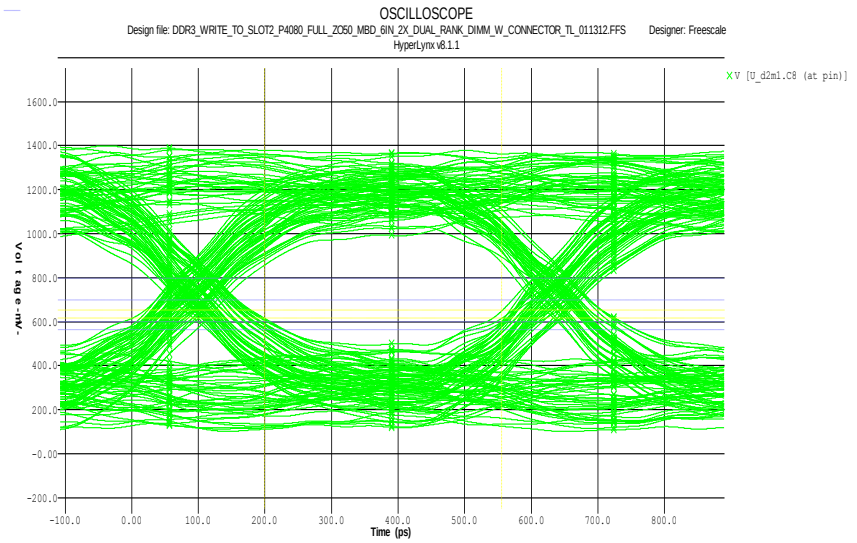
Read/Write	DIMM	#_DIMMs	Slot	Data Eye Width at AC-DC Vin Levels (Ave High & Low Vin - ps)
Write	Dual Rank	1	2	406.5
Read	Dual Rank	1	2	359
Write	Dual Rank	2	2	321
Write	Dual Rank	1	1	309.5
Write	Dual Rank	2	1	307.5
Write	Quad Rank	1	2	299
Read	Dual Rank	1	1	295.5
Read	Dual Rank	2	2	283
Write	Quad Rank	1	1	250
Read	Dual Rank	2	1	247
Read	Quad Rank	1	1	196.5
Read	Quad Rank	1	2	177

DDR3-1866 Write with Two Dual Ranked DIMMs

- **Write to Slot 1**

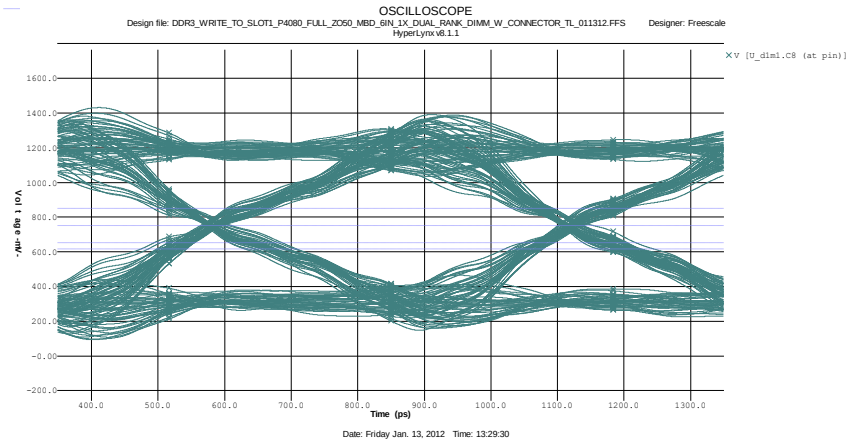


- **Write to Slot 2**

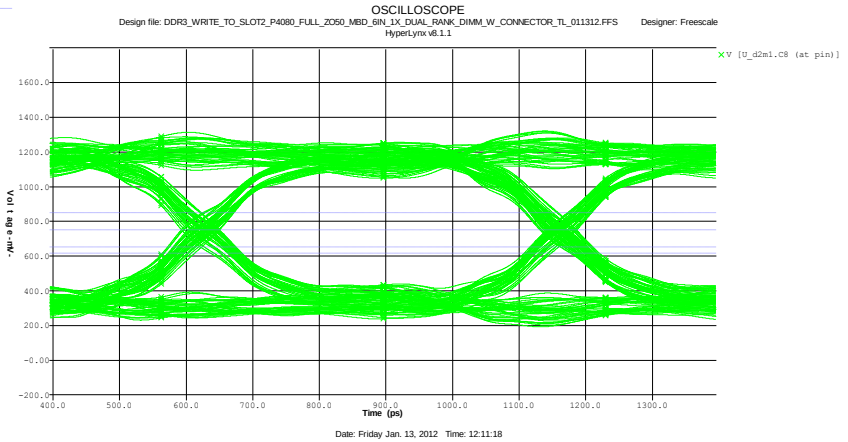


DDR3-1866 Write with One Dual Ranked DIMM:
Improvement in Data Eye is More Pronounced

- **Write to Slot 1**

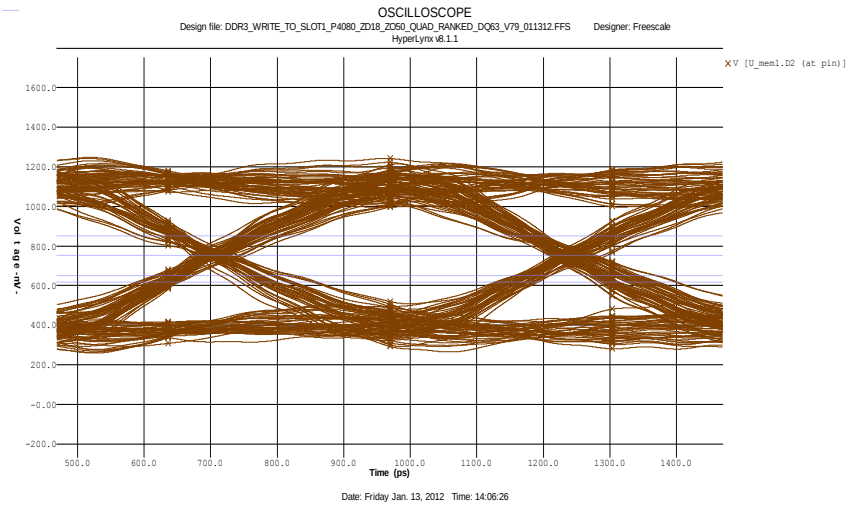


- **Write to Slot 2**

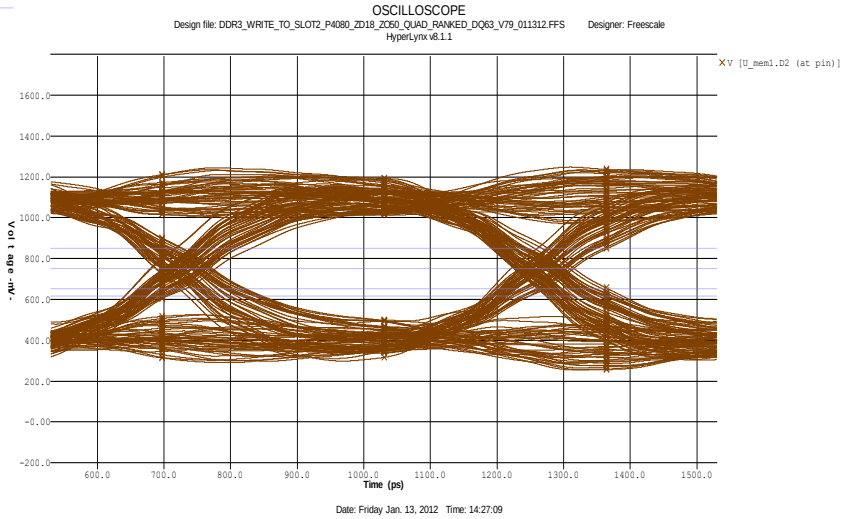


DDR3-1866 Write with One Quad Ranked DIMM

- **Write to Slot 1**

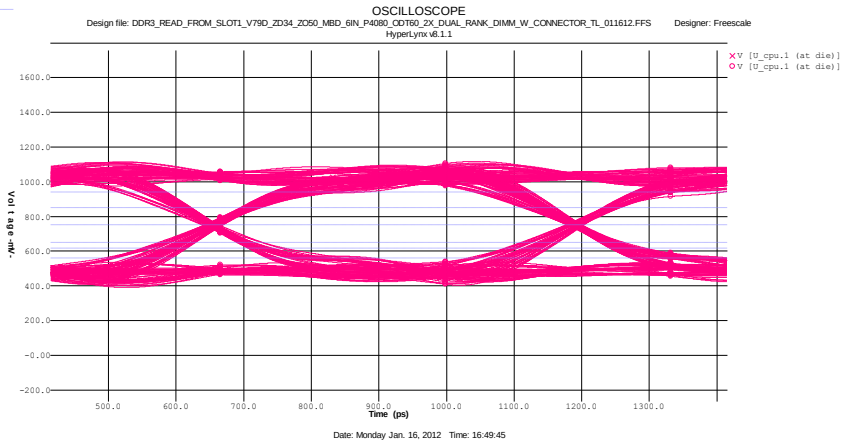


- **Write to Slot 2**

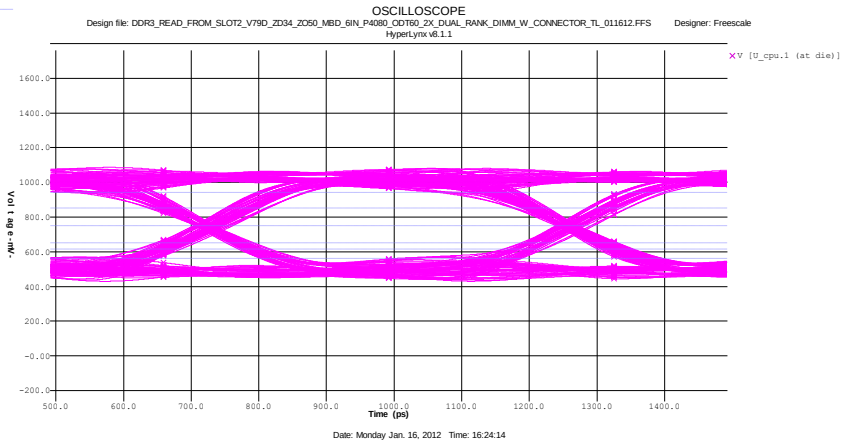


DDR3-1866 Read with Two Dual Ranked DIMMs

- **Read from Slot 1**

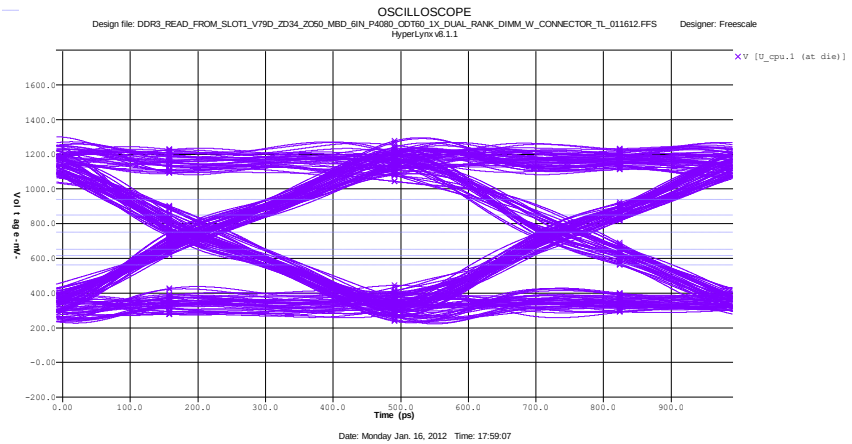


- **Read from Slot 2**

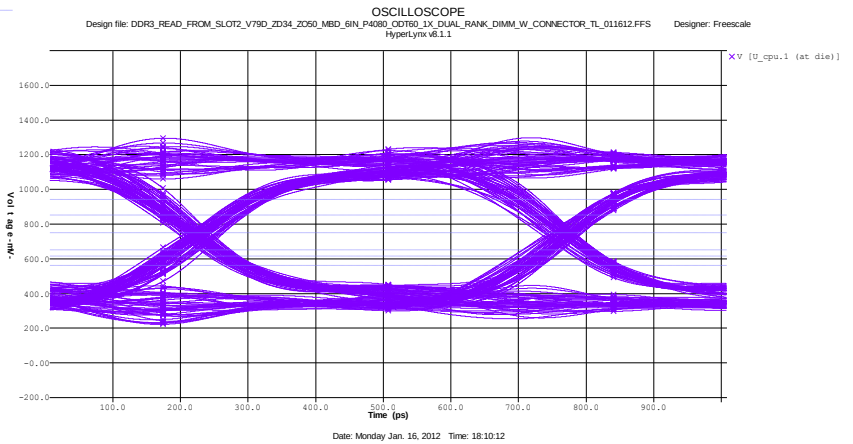


DDR3-1866 Read with One Dual Ranked DIMM

- **Read from Slot 1**

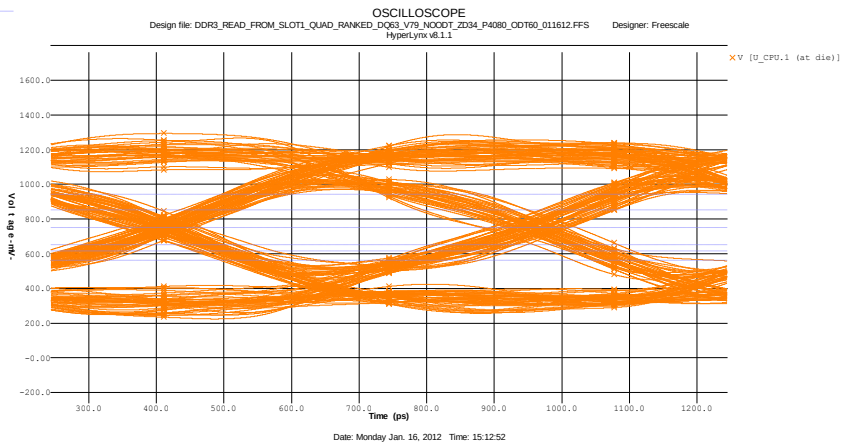


- **Read from Slot 2**

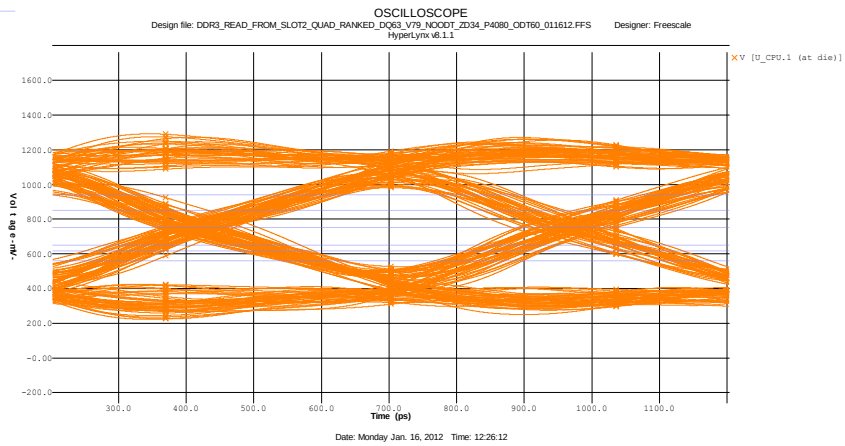


DDR3-1866 Read with One Quad Ranked DIMM

- **Read from Slot 1**



- **Read from Slot 2**

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