AH1301

TJA1052i Galvanic Isolated High Speed CAN Transceiver

Rev. 1.2 — 19 August 2014 **Technical Report**

Document information

Info	Content
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1.0	2013-03-01	Initial Version
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1.2	2014-08-19	State diagram corrected (Fig.11)

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1. Introduction

1.1 Portfolio

Fig 1 shows the current high speed CAN (HSCAN) standalone transceiver portfolio of NXP.

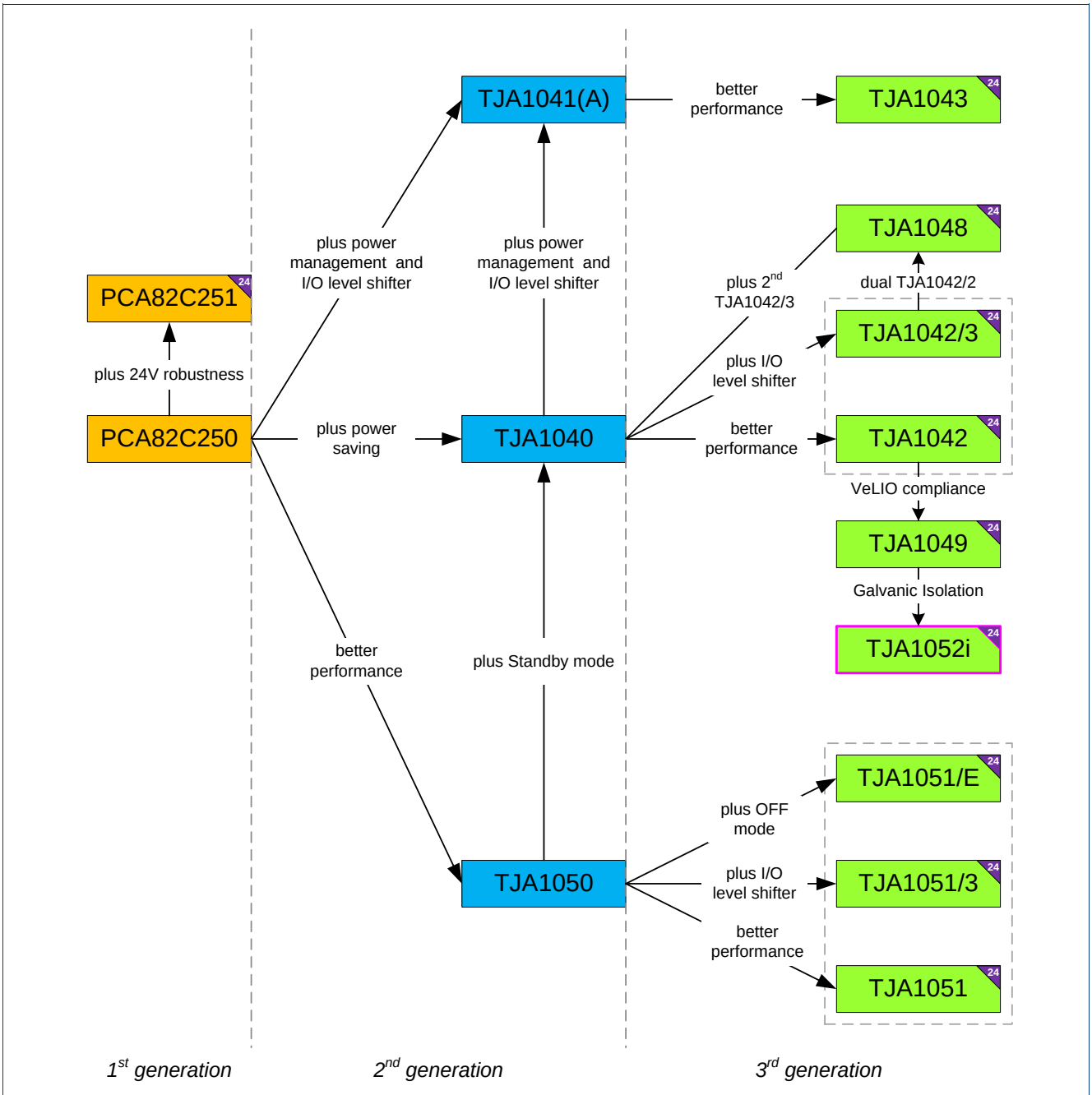


Fig 1. Overview of current NXP's standalone high speed CAN transceiver portfolio

1.2 Galvanic Isolation

Isolated CAN applications are becoming increasingly common in electric and hybrid electric vehicles. The TJA1052i is the ideal solution in applications that require an isolated CAN node, such as Li-ion battery management, regenerative braking and 48 V-to-12 V level shifting. The device can also be used to isolate high-voltage on-demand pumps and motors in belt elimination projects (see Fig 2).

Since subsystems in the vehicle are sometimes distributed over a greater distance in the vehicle, isolation that avoids ground loops and protects the systems against high voltage pulses is advised. Galvanic isolation also reduces signal distortion. In addition to protecting against high voltages, corresponding transceivers thus contribute towards increasing the robustness of the bus system by ensuring the signal integrity. An interrupted signal transmission means that bus system performance is decreased, messages are sent multiple times, or system responses are delayed. This effect increases with the number of nodes in the network.

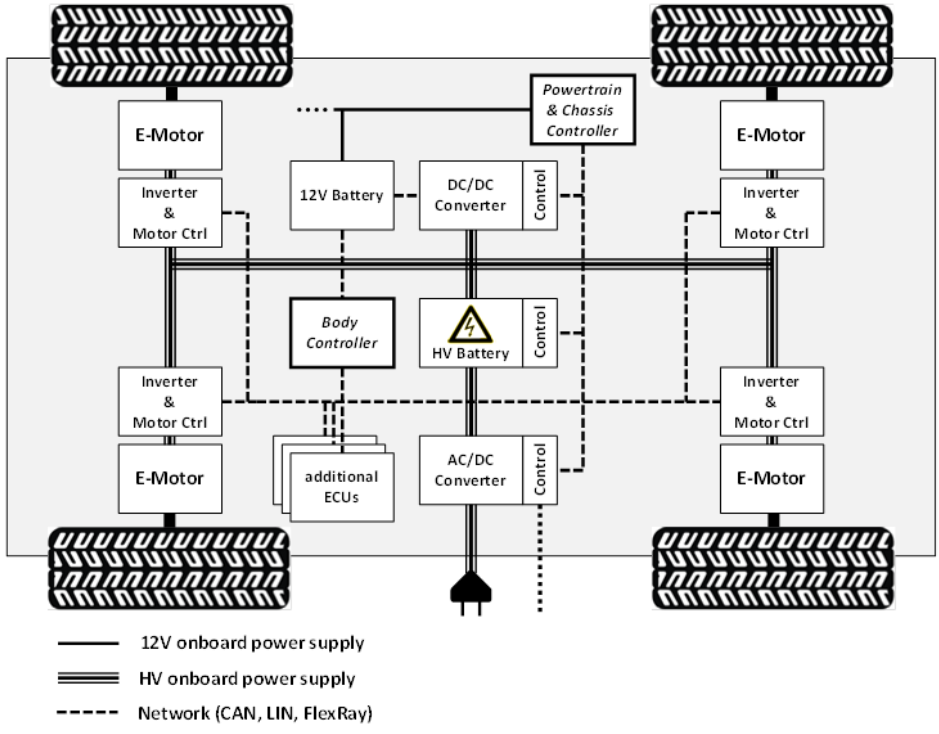


Fig 2. Networking of components in various voltage domains

The TJA1052i combines the advantages of optimized transceivers and those of the galvanic isolation without having to compromise functionality, safety, or EMC.

2. TJA1052i – Galvanic Isolated HSCAN Transceiver

2.1 General

The TJA1052i has implemented capacitive isolation in a CAN transceiver. This solution incorporates the advantages of low current consumption, short processing times, and stable pulse widths. Through appropriate implementation, the sensitivity to HF fields present at capacitive isolators was able to be limited to a non-application relevant degree.

The TJA1052i belongs to the third-generation of NXP`s high-speed [HS] CAN transceivers. It combines the advantages of a galvanic isolation of up to 5000 VRMS with the excellent EMC characteristics of non-isolated CAN transceivers from NXP Semiconductors. The TJA1052i [1] is in compliance with ISO 11898-2 and has a loop delay of 220 ns including isolation, which enables a maximum baud rate of 1 MBaud in automotive networks.

2.2 Main features

- Electrical transient immunity of 45 kV/µs (typ.)
- ISO 11898-2 compliant; Loop delay < 220ns
- Suitable for use in 12 V and 24 V systems
- Compatible with 3 V to 5 V microcontrollers
- Bus common mode voltage (Vcm) = ±25V
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)

2.3 Block Schematic

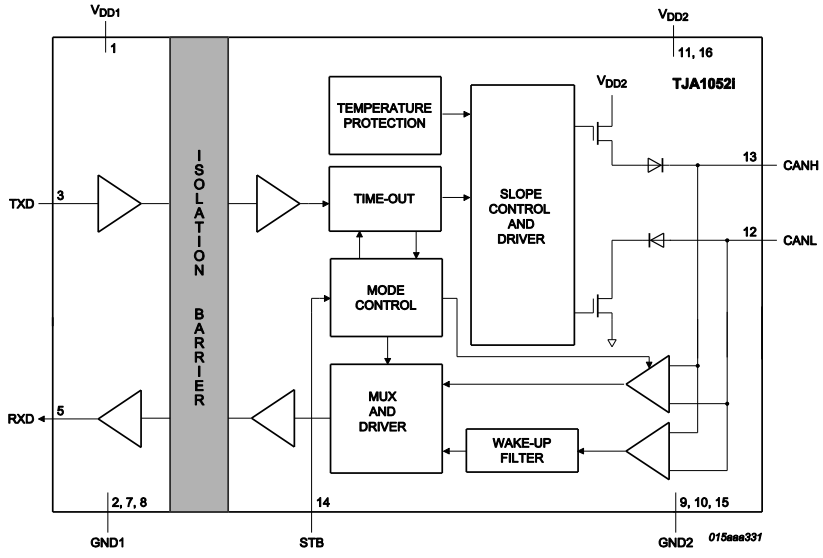


Fig 3. Block schematic of TJA1052i

2.4 Pinning

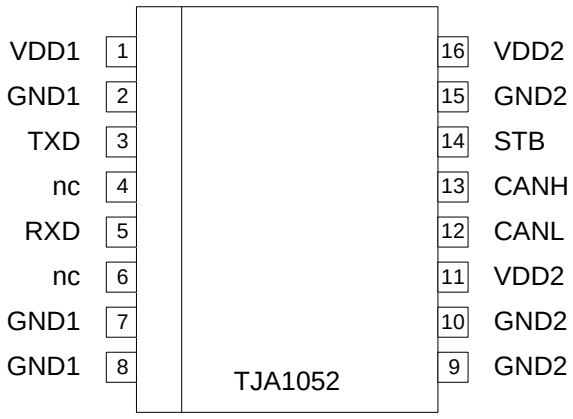


Fig 4. pinning of the TJA1052i

Table 1. Pin description

Pin No	Symbol	Description
1	VDD1	Supply voltage 1
2	GND1	Ground of supply 1
3	TXD	Transmit data input
4	n.c.	Not connected
5	RXD	Receive data output
6	n.c.	Not connected
7	GND1	Ground of supply 1
8	GND1	Ground of supply 1
9	GND2	Ground of supply 2
10	GND2	Ground of supply 2
11	VDD2	Supply voltage 2
12	CANL	Low level CAN bus line
13	CANH	High level CAN bus line
14	STB	Standby mode input
15	GND2	Ground of supply 2
16	VDD2	Supply voltage 2

2.5 Functional Description

The isolator uses proprietary capacitive isolation technology to transmit and receive CAN signals. The isolation is placed within the TXD and RXD path.

An input signal is modulated by an RF oscillator using On-Off-Keying (OOK). The receiver demodulates according to its RF energy scheme. The modulation takes place in recessive state whereas the dominant state is silent see Fig 5.

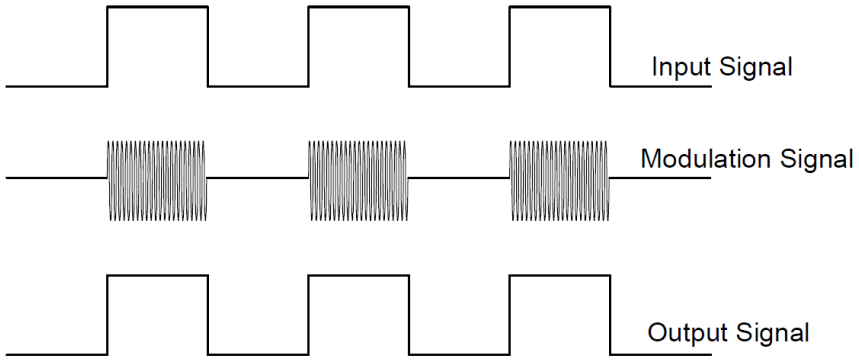


Fig 5. Input signal modulation

2.6 Power-up and power-down sequence

If the TJA1052i is used in a HS-CAN network that supports remote bus wake-up, the power- down sequence of the supplies must be managed properly to avoid a dominant pulse on the CAN bus.

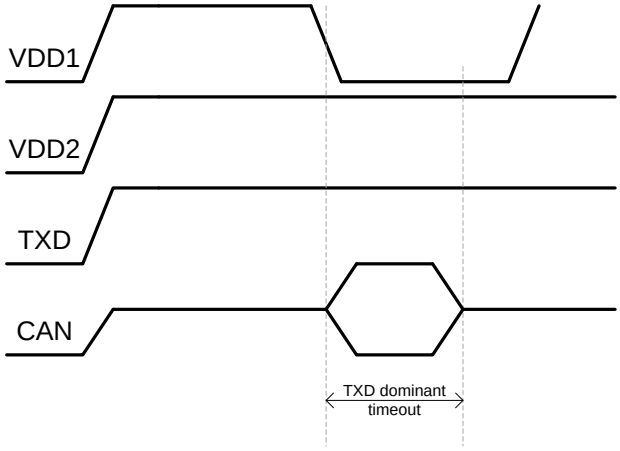


Fig 6. Power sequence of TJA1052i

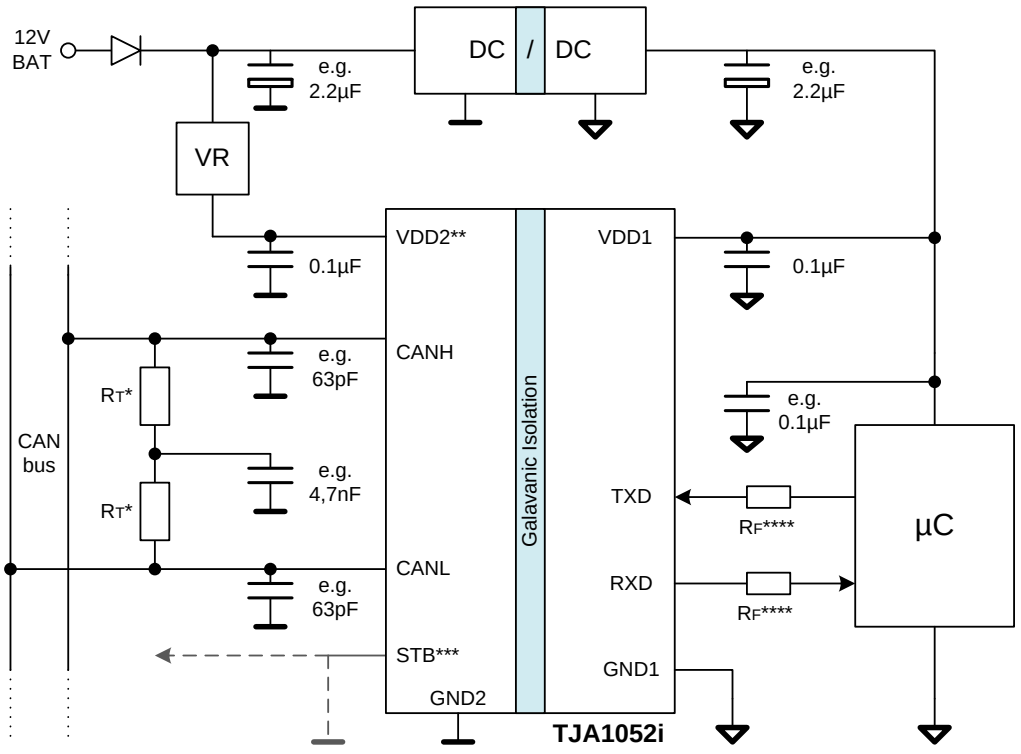
As soon as the undervoltage threshold of VDD1 is passed during ramp down the oscillation is also stopped and therefore the CAN bus is driven dominant until the TXD dominant time-out time overflows and the TJA1052i releases the CAN bus again.

In order to avoid the dominant pulse V_{DD2} should pass the minimum undervoltage threshold ($V_{uvd(stb)(VDD2)(min)}$) before V_{DD1} falls below its maximum undervoltage detection threshold ($V_{uvd(VDD1)(max)}$).

Power-up sequencing can happen in any order. Note, that the isolator takes maximum 500 µs before the modulation is stable (see data sheet $t_{startup}$). The start-up time is the time from the application of power to valid data at the output.

3. Application Information (Hardware)

Fig 7 illustrates the reference design of the isolated HSCAN transceiver TJA1052i. The device is able to operate from 5V down to 3.3V on the primary side that allows connecting 3V and 5V microcontrollers. The secondary side needs to be supplied out of 5V for the CAN transceiver.



* For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept“. For stub nodes an optional "weak" termination of e.g. R_T = 4,7kOhm can be foreseen, if required by the OEM.
A dedicated application may depend on specific OEM requirements

** Both VDD2 input pins should be buffered with 0.1µF. and the capacitors should be placed as close as possible to the input pins

*** Setting STB HIGH disables the CAN bus connection; Setting to LOW sets the transceiver into Normal mode; see chapter 3.3 for further information

**** R_F is an optional series resistor for improving EMC performance

Fig 7. TJA1052i – Application circuitry with single supply

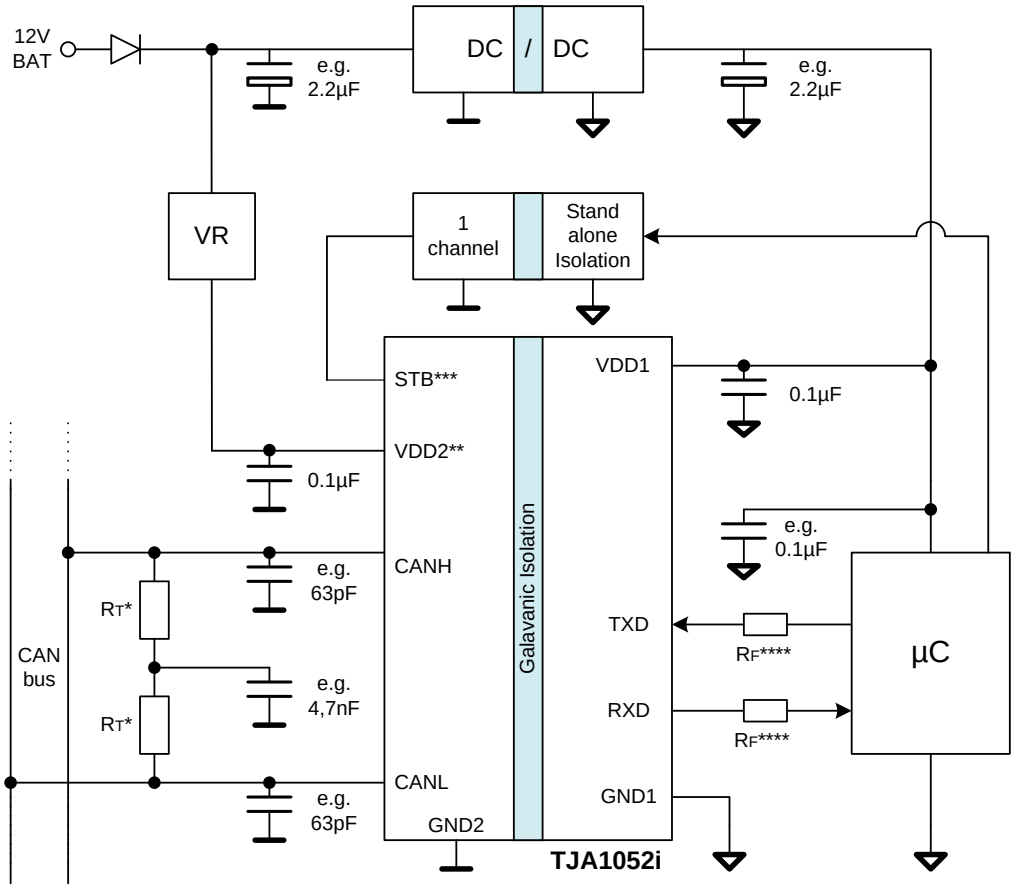


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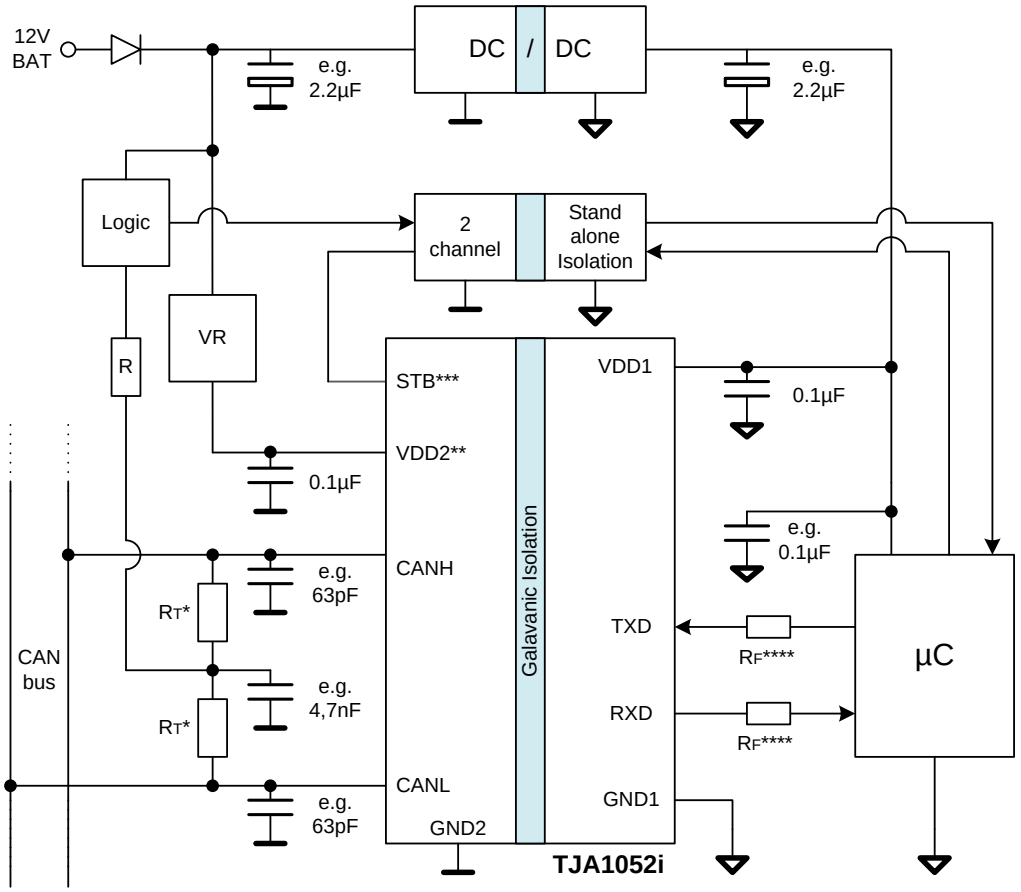
Fig 8. TJA1052i – Application circuitry with single supply and isolated STB mode control



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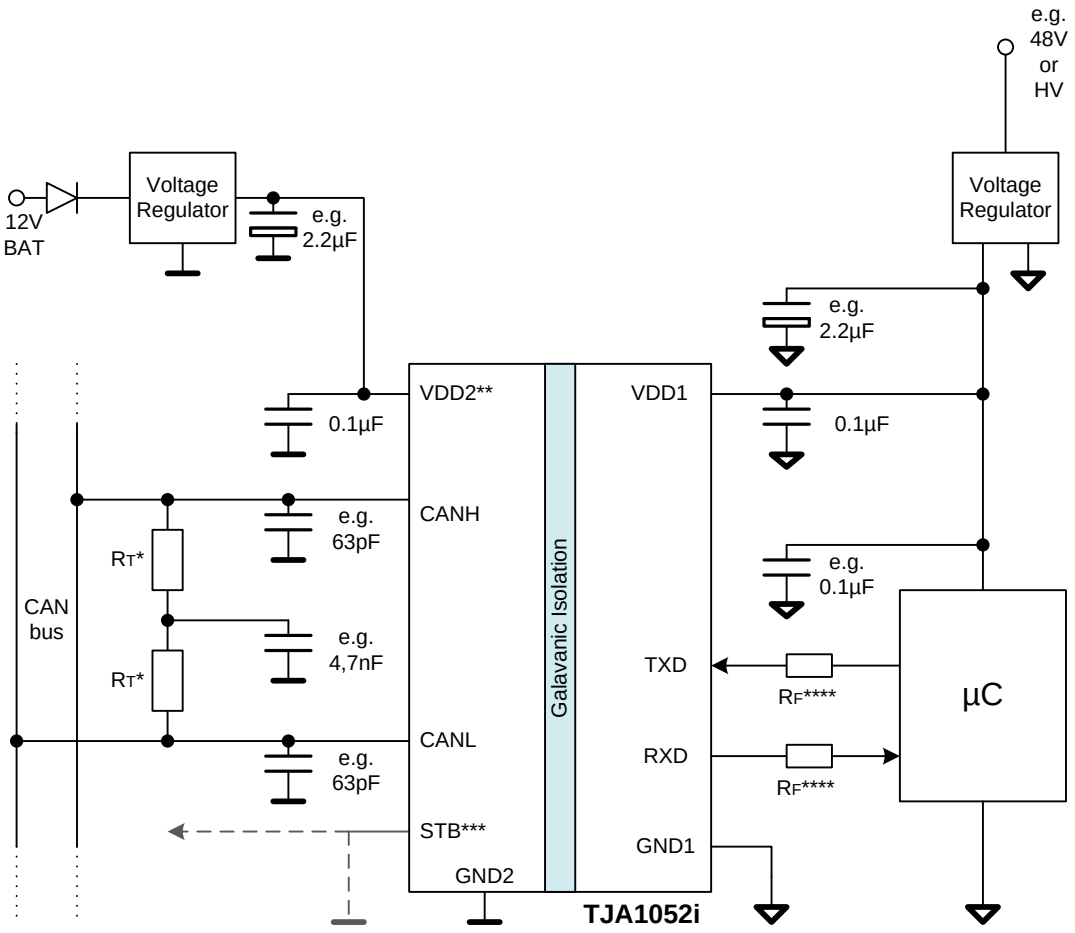
A dedicated application may depend on specific OEM requirements

** Both VDD2 input pins should be buffered with 0.1µF. and the capacitors should be placed as close as possible to the input pins

*** Setting STB HIGH disables the CAN bus connection; Setting to LOW sets the transceiver into Normal mode; see chapter 3.3 for further information

**** R_F is an optional series resistor for improving EMC performance

Fig 9. TJA1052i – Application circuitry with single supply, isolated STB mode control and CAN state feedback



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A dedicated application may depend on specific OEM requirements

** Both VDD2 input pins should be buffered with 0.1µF. and the capacitors should be placed as close as possible to the input pins

*** Setting STB HIGH disables the CAN bus connection; Setting to LOW sets the transceiver into Normal mode; see chapter 3.3 for further information

**** R_F is an optional series resistor for improving EMC performance

Fig 10. TJA1052i – Application circuitry with dual power supply

3.1 Power Supply Pins

3.1.1 Pin VDD1

The VDD1 supply provides the current needed for the RXD and TXD interface pins. The TJA1052i requires a 0.1µF buffer capacitor between VDD1 and GND1. The capacitor should be placed as close as possible to the transceiver.

In order to further improve the robustness of a design, it is recommended that also a 1µF bypass capacitor is added.

3.1.2 Pin VDD2

The V_{DD2} supply provides the current needed for the transmitter and receiver of the integrated high speed CAN transceiver. The V_{DD2} supply must be able to deliver current of 65mA in average for the transceiver (see chapter 3.1.2.1).

Two capacitors between 47nF and 100nF are recommended being connected between V_{DD2} and GND2 close to the transceiver pins. These capacitors buffer the supply voltage during the transition from recessive to dominant, when there is a sharp rise in current demand. For reliability reasons it might be useful to apply two capacitors in series connection between V_{DD2} and GND2. A single shorted capacitor (e.g. damaged device) cannot short-circuit the V_{DD2} supply.

Using a linear voltage regulator, it is recommended to stabilize the output voltage with an additional bypass capacitor (see chapter 3.1.2.2) that is usually placed at the output of the voltage regulator. Its purpose is to buffer disturbances on the battery line and to buffer extra supply current demand in the case of bus failures. The calculation of the bypass capacitor value is shown in chapter 3.1.2.2, while in chapter 3.1.2.1 the average V_{DD2} supply current is calculated for thermal load considerations of the V_{DD2} voltage regulator. This can be done in absence and in presence of bus short-circuit conditions.

3.1.2.1 Thermal load consideration for the V_{DD2} voltage regulator

The averages V_{DD2} supply current can be calculated in absence (see Table 2) and in presence (see Table 3) of bus short-circuit conditions [1].

Assuming a transmit duty cycle of 50% on pin TXD the maximum average supply current in absence of bus failures calculates to:

$$I_{DD2\_norm\_avg} = 0.5 \bullet (I_{DD2\_REC\_MAX} + I_{DD2\_DOM\_MAX})$$

Table 2. Maximum V_{DD2} supply current in recessive and dominant state

Device	$I_{DD2\_REC\_MAX}$ [mA]	$I_{DD2\_DOM\_MAX}$ [mA]
TJA1052i	10	70

In presence of bus failures the V_{DD2} supply current for the transceiver can increase significantly. The maximum dominant V_{DD2} supply current $I_{DD2\_DOM\_SC\_MAX}$ flows in case of a short circuit from CANH to GND2. Along with the CANH short circuit output current $I_{O(dom)}$ the maximum dominant supply current $I_{DD2\_DOM\_SC\_MAX}$ calculates to about 110mA.

Table 3. Average V_{DD2} supply current

Device	$I_{DD2\_norm\_avg}$ [mA]	$I_{DD2\_AVG\_SC\_MAX}$ [mA]
TJA1052i	40	110

3.1.2.2 Dimensioning the bypass capacitor of the voltage regulator

Depending on the power supply concept, the required worst-case bypass capacitor and the extra current demand in the case of bus failures can be calculated.

Dimensioning the capacitor gets very important with a shared voltage supply. Here, extra current demand with bus failures may not lead to an unstable supply. This input is used to determine the bypass capacitor needed to keep the voltage supply stable under the assumption that all the extra current demand has to be delivered from the bypass capacitor.

The quiescent current delivered from the voltage regulator to the transceiver is determined by the recessive V_{DD2} supply current I_{DD2_REC}.

In absence of bus failures the maximum extra supply current is calculated by:

$$\Delta I_{DD2\_max} = (I_{DD2\_DOM\_MAX} - I_{DD2\_REC\_MIN})$$

Considering the worst case of a short circuit from CANH to GND2 the maximum extra supply current is calculated by:

$$\Delta I_{DD2\_max\_sc} = (I_{DD2\_DOM\_SC\_MAX} - I_{DD2\_REC\_MIN})$$

3.1.2.3 Example

With $I_{DD2\_dom\_sc\_max}$ = 120 mA (estimated) and $I_{DD2\_rec\_min}$ = 2 mA the maximum extra supply current calculates to

$$\Delta I_{DD2\_max\_sc} = 118 \text{ mA}$$

In the case of a short circuit from CANH to GND2, the bus is clamped to recessive state, and according to the CAN protocol the uC transmits 17 subsequent dominant bits. That would mean the above calculated maximum extra supply current has to be delivered for at least 17 bit times[1].

Assuming that the complete extra supply current during the 17 bit times has to be buffered by the bypass capacitor, the worst-case bypass capacitor calculates to:

[1] The reason for the 17 bit times is that at the moment the CAN controller starts a transmission, the dominant Start Of Frame bit is not fed back to RXD and forces an error frame due to the bit failure condition. The first bit of the error frame again is not reflected at RXD and forces the next error frame until the CAN controller reaches the Error Passive state.

$$C_{BUFF} = \frac{\Delta I_{DD2\_max\_sc} \cdot t_{dom\_max}}{\Delta V_{max}}$$

Whereas ΔV_{max} is the maximum allowed voltage drop at pin V_{DD2} and t_{dom_max} is the dominant time of 17 bit times at 500kbit/s.

Table 4. Average V_{DD2} supply current (assuming 500kbit/s)

Device	$\Delta I_{DD2\_max\_sc}$	t_{dom_max}	ΔV_{max}	C_{BuFF}
TJA1052i	108mA	34µs	0,25V	≈ 15µF

Of course, depending on the regulation capabilities of the used voltage regulator the bypass capacitor may be much smaller.

3.1.3 Pins GND1 & GND2

GND1 is the reference of the primary side of the TJA1052i and GND2 is the reference of the secondary side.

3.2 Interface Pins

3.2.1 TXD pin

The transceiver receives the digital bit stream to be transmitted onto the bus via the pin TXD. When applied signals at TXD show very fast slopes, it may cause a degradation of the EMC performance. Depending on the OEM an optional series resistor of up to 1kΩ within the TXD line between transceiver and microcontroller might be useful. Along with pin capacitance this would help to smooth the edges for some degree. For high bus speeds (close to 1 Mbit/s) the additional delay within TXD has to be taken into account. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

3.2.2 RXD pin

The analog bit stream received from the bus is output at pin RXD for further processing within the CAN-controller. As with pin TXD a series resistor of up to 1 kΩ can be used to smooth the edges at bit transitions. Again the additional delay within RXD has to be taken into account, if high bus speeds close to 1 Mbit/s are used. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

3.3 Mode control pin STB

This input pin is a mode pin and used for mode control. It is usually connected directly to an output port pin of a microcontroller. But due to the insulation barrier the STB pin is not directly accessible for the microcontroller. For that reason the pin should be connected to GND2 in order to set the TJA1052i in Normal mode.

If the Standby functionality should be used this pin can be controlled using an additional isolator channel (see also Fig 8 or Fig 9). If it is important to know the state of the CAN network if it is in Standby or Normal mode, the center voltage of the CAN bus split termination can be used and feedback to the microcontroller. But this must also be done by an additional isolator channel (see also Fig 8 or Fig 9).

3.4 Bus Pins CANH / CANL

The transceiver is connected to the bus via pin CANH/L. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Instead of a one-resistor termination it is highly recommended using the so-called Split Termination, illustrated in Fig 15. EMC measurements have shown that the Split Termination is able to improve significantly the signal symmetry between CANH and CANL, thus reducing emission. Basically each of the two termination resistors is split into two resistors of equal value, i.e. two resistors of 60Ω (or 62Ω) instead of one resistor of 120Ω. The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. The recommended value for this capacitor is in the range of 4,7nF to 47nF.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: <1%).

Additionally it is recommended to load the CANH and CANL pin each with a capacitor of up to 100pF close to the connector of the ECU (see Fig 14). The main reason is to increase the robustness to automotive transients and ESD. The matching tolerance of the two capacitors should be as low as possible.

OEMs might have dedicated circuits prescribed in their specifications. Please refer to the corresponding OEM specifications for individual details.

3.5 Operation Modes

Referred to the secondary side where the CAN chip is present the TJA1052i has the possibility to be used in 2 different power modes, Normal Mode and Standby Mode which are selectable via STB pin. Taking into account the undervoltage detection a third power mode is available, the so-called OFF Mode.

Based on the fact that the STB pin is not directly accessible for the microcontroller this pin should be connected to GND2 in order to set the TJA1052i in Normal mode. Nevertheless there are applications which might use the Standby functionality.

Fig 11 shows how the different operation modes can be entered. Every mode provides a certain behavior and terminates the CAN channel to a certain value. The following sub-chapters give a short overview of those features.

3.5.1 Normal Mode

In Normal Mode the CAN communication is enabled. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The bus lines are biased to $V_{DD2}/2$ in recessive state and the transmitter is enabled. The Normal Mode is entered setting pin STB to LOW.

In Normal Mode the transceiver provides following functions:

- The CAN transmitter is active.
- The normal CAN receiver is active.
- The low power CAN receiver is active.
- CANH and CANL are biased to $V_{DD2}/2$.
- The isolation carrier signal is on.
- Pin RXD reflects the normal CAN Receiver.
- V_{DD2} undervoltage detectors for Standby Mode ($V_{uvd(stb)(VDD2)}$) and for Off Mode ($V_{uvd(swoff)(VDD2)}$) are active.

3.5.2 Standby Mode

In Standby mode the TJA1052i is not capable of transmitting and receiving regular CAN messages, but it monitors the bus for CAN messages.

Only the isolation and the low power CAN receiver are active, monitoring the bus lines for activity. The bus wake-up filter ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on the RXD pin.

To reduce the current consumption the CAN bus is terminated to GND rather than biased to $V_{DD2}/2$ as in Normal mode. The Standby mode is selected setting pin STB to HIGH or by standby undervoltage detection on pin V_{DD2} ($V_{uvd(swoff)(VDD2)} < V_{DD2} < V_{uvd(stb)(VDD2)}$). Due to an internal pull-up function on the STB pin it is the default mode if pin STB is unconnected.

In Standby Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.

- The low power CAN receiver is active.
- CANH and CANL are biased to GND.
- The isolation carrier signal is on.
- Pin RXD reflects the low-power CAN receiver.
- V_{DD2} undervoltage detectors for Standby mode ($V_{uvd(stb)(VDD2)}$) and for Off Mode ($V_{uvd(swoff)(VDD2)}$) are active.

3.5.3 OFF Mode

The non-operation OFF Mode is introduced offering total passive behaviour to the CAN bus system. The OFF Mode is entered by off undervoltage detection on pin V_{DD2} ($V_{DD2} < V_{uvd(swoff)(VDD2)}$).

In OFF Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is off.
- CANH and CANL are floating (lowest leakage current on bus pins).
- The isolation carrier signal is off.
- V_{DD2} undervoltage detectors for Standby mode ($V_{uvd(stb)(VDD2)}$) and for Off Mode ($V_{uvd(swoff)(VDD2)}$) are active.

3.6 State diagram for CAN chip

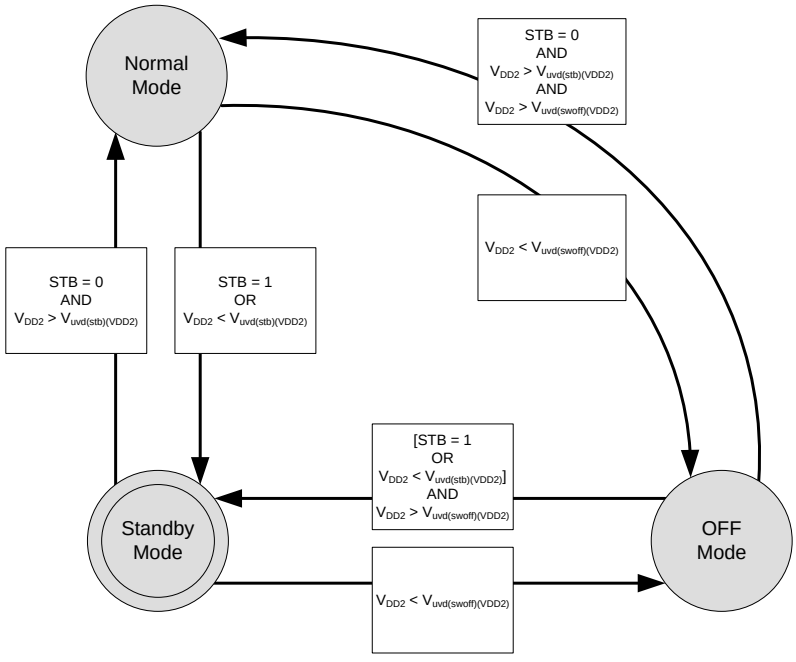


Fig 11. State diagram for secondary side (CAN)

4. Safety Related Information

4.1 Standard Compliance

For safety reasons it is necessary to separate high voltage domains (>60Vdc or 30Vac) from the safe low voltage domains (<60Vdc or 30VAC) by a certain distance called creepage and clearance distances (see chapter 4.2). Additionally the insulation barrier must provide a sufficient high voltage breakdown protection that is specifies as rated voltage (see chapter 4.5) and refers to the working voltage.

The TJA1052i will be certified against international standards IEC61010-Ed2 and IEC60950 [6], [4].

The link between working voltage, creepage/clearance, rated voltage, and withstand voltage is relevant for all end-use system standards. The TJA1052i does not need to be compliant to all different standards, instead it is more important to know what kind of parameters are relevant to meet the safety requirements.

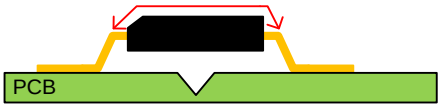
4.2 Creepage and Clearance Distances

From a device point of view the isolator package geometry is important to prevent electrical arcing across package surfaces. Referring to different standards the package creepage and clearance dimensions are specified as a function of test voltage.

Clearance is the shortest distance in air between two conductive parts (see Fig 12b). The major factors affecting clearance are air pressure (altitude) & temperature, overvoltage category, homogenous vs. inhomogeneous fields, and temporary overvoltages or recurring peak voltages.

Creepage is the shortest distance along the surface of the insulating material and through air between two conductive surfaces (see Fig 12a). The major factors affecting creepage are pollution degree, humidity, dust deposition, and material properties (CTI).

a. Clearance distance



b. Creepage distance

Fig 12. Figure title here

The data sheet [1] specifies the creepage and clearance distances of the TJA1052i. Table 5 shows the specification as included in the data sheet. Note that the clearance distance can principally not be larger than the creepage distance.

Table 5. Creepage and Clearence Distances

Symbol	Parameter	Min. Value	Unit
L_{IO1}	Minimum air gap – clearance	8.6	mm
L_{IO2}	Minimum external tracking – creepage	8.1	mm

These package specific values can be calculated using the data of the package outline (see Table 6). The formulas are listed below.

Please also take into account that these values are only valid it an external passivation is used so that the tie bars stubs must not be taken into account as well (see chapter 4.3)

Table 6. Values from package outline for calculation of creepage distance

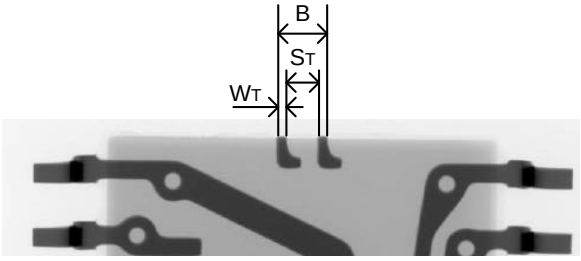
Parameter	Value	Unit
D min	10.1	mm
e (7x)	1.27 (8.89)	mm
bp max	0.49	mm
E min	7.4	mm
Results	**8.12**	**mm**
B [1]	1.02	mm

[1] See chapter 4.3 for more details about B

Creepage: L(IO2) = Dmin – 7xe – bpmax + Emin

4.3 Tie bar stubs

For production reasons the package includes intervening, non connected conductive parts also called as tie bar stubs. Based on IEC60950-1 (Annex F) [4] and IEC60664-1 [5] the distance between the unconnected conductive parts must be subtracted from creepage path if it is less than 1.0mm. Referring to Fig 13 that means the distance B must be subtracted from the creepage distance (taken from the outline plan) if S_T < 1.0mm. But only if there is no external coating is used.



S_T: spacing between tie bar stubs as visible from outside

W_T: width of tie bar stub

B: to be subtracted from creepage

$B = S_T + 2x0.25 = 1.02$ mm

Fig 13. Presence of an intervening, unconnected conductive part

4.4 Rated working voltage

This is the voltage value that could be present continuously between the terminals of the TJA1052i. It is the largest voltage difference that occurs within the system. For 3-phase circuits it is expressed as the voltage between phases. It is need to determine the rated insulation voltage, the insulation withstand voltage, and the overvoltage category.

For a battery supplied system it is the maximum voltage of the battery including, e.g. +/- 10% variation in the supply voltage.

4.5 Rated Voltage

Table 7 shows the rated voltage of the TJA1052i. This voltage specifies the test voltage for the dielectric strength tests. The insulation withstands this high voltage for at least 1 minute without any damage. During production each TJA1052i is tested with 1.2 times the maximum rated voltage for at least 1s.

Table 7. Rated voltages and production test voltages

Type	Rated Voltage for [60s]	Production Test Voltage [for 1s]
TJA1052i/5	5000 V_{RMS}	6000 V_{RMS}
TJA1052i/2	2500 V_{RMS}	3000 V_{RMS}
TJA1052i/1	1500 V_{RMS}	1800 V_{RMS}

Which type is selected depends on the dedicated system requirements specified by the module manufacturer based on various different standards. For automotive the ISO6469-3 is important and it depends on the intention of the ECU that means is it indented to be class 1 or class 2 equipment. An example how to select the right type of the TJA1052i is shown in chapter 5.

The dielectric strength determined by the rated voltage is the basis for the selection of the isolation classification (e.g. basic, supplementary or reinforced).

Basic isolation provides a single level of protection against electrical shock ([4], [5]) and cannot be considered as failsafe.

Reinforced isolation provides two levels of protection for failsafe operation that is equivalent to double insulation (basic plus supplementary insulation) and allows user access.

4.6 Rated impulse withstand voltage

The highest peak value of an impulse voltage of prescribed form 1.2/50, which does not cause breakdown under specified conditions of test

5. Example: How to select the right device

This chapter describes how to determine the working voltage and the insulation voltage that is important to select the right type of the TJA1052i.

As mentioned before the working voltage is the highest continues voltage that occurs between the high and low voltage side. This voltage is related to mains voltage of the equipment or the connected battery. But there must also be taken into account the maximum recurring peak voltage [5] of the supply voltage. That means if the module is supplied out of a battery with a nominal voltage of 450Vdc there could be +/- 10% variation in the supply voltage on top. For this reason the maximum working voltage calculates to V_{IORM} = 1.1xV_{BAT} = 495Vdc (for further calculations let's assume 500Vdc). A lot of standards are based on RMS voltages, so the 500Vdc can be considered as ~350V_{RMS}.

As next step it needs to be defined towards which end use standard (like IEC61010 or IEC60950) the module must comply with. Those standards dictate the required creepage (see Table 8) and clearance distances for the system. The TJA1052i is designed for material group 2 and pollution degree 2.

Table 8. Creepage for dedicated mains voltages [1]

IEC60950, Pollution Degree 2, Values given in millimeters [mm]

Working Voltage (V_{RMS})	Functional, Basic, and Supplementary Insulation		Reinforced Insulation	
	Material Group		Material Group	
	II	III	II	III
150	1.1	1.6	2.2	3.2
300	2.2	3.2	4.4	6.4
400	2.8	4.0	5.6	8.0
500	3.6	5.0	7.2	10.0
600	4.5	6.3	9.0	12.6

[1] This table is not indented to be used for system design, please refer to the dedicated standard

Based on the overvoltage category and the working voltage the mains transient voltage can be selected just going into the IEC specifications. Table 9 summarizes the transient voltages specified in IEC60950 for overvoltage category 2.

Table 9. Defined transient voltages

IEC60950, Pollution Degree 2

Supply voltage V_{RMS}	Transient voltage [V_{peak}]
Over 100 up to 150	1500
Over 150 up to 300	2500
Over 300 up to 600	4000
Over 600 up to 1000	6000

Taking the transient voltage from Table 9 it's possible to select also the required clearance distances. The last step would be to select the qualification test voltage for the

chosen isolated component based on the required grade of insulation (see Table 10, e.g. basic or reinforced).

Table 10. Test voltages for strength test

IEC60950 table 5B part 1 & part 2

Grade of Insulation	Working voltage	
	210 < U ≤ 420	420 < U ≤ 1.41kV
Basic	1500	1605 up to 2814
Reinforced	3000	3000

Summary of parameters

Table 11. Summary of parameters

Maximum working voltage	$350V_{RMS}$ or $500V_{DC}$
Material Group	2
Pollution Degree	2
Overvoltage Category	2
Grade of Insulation	Reinforced
	⇓
Transient Voltage	4000 Vpeak
Clearance	6.4 mm
Creepage	5.6 mm → 6.4 mm Remark: The clearance distance cannot be larger than the creepage distance
Qualification test voltage	3000Vrms → defines the rated voltage of the TJA1052i

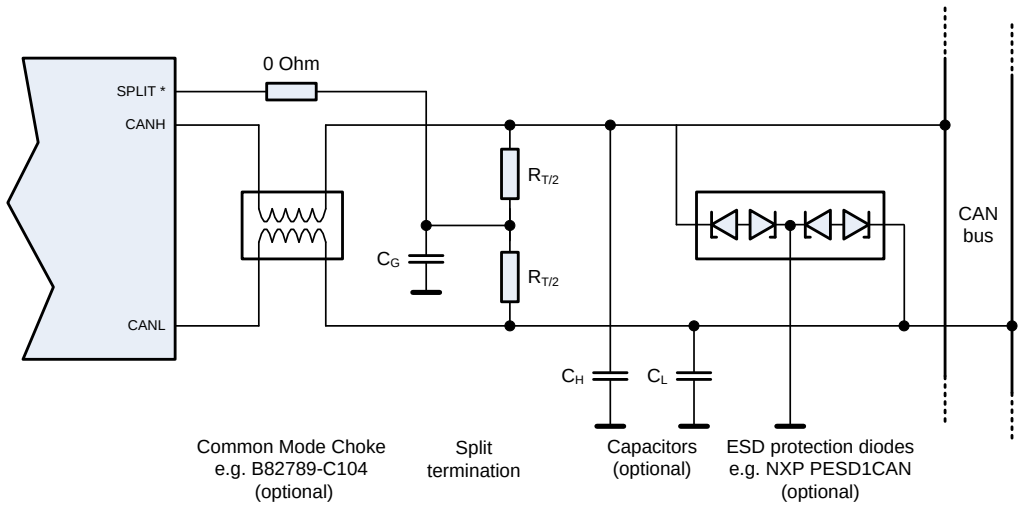
The TJA1052i/5 fits to the requirements defined by the IEC60950-1.

6. EMC aspects of high speed CAN

Achieving a high EMC performance is not only a matter of the transceiver, a careful system implementation (termination, topology, external circuitry, and PCB layout) is also very important.

The possibilities to further improve the EMC performance include differential and common mode filters, shielded twisted pair cable and ESD protections diodes. Additionally the PCB layout is critical to maximize the effectiveness of the EMC improvement circuit. All additional circuits could distort the signal waveform and they are also limited by the physical layer specifications.

This chapter presents some application hints (all are referenced to Fig 14) aiming to exploit the outstanding EMC performance of the 3rd generation high speed CAN transceivers.



* TJA1042, TJA1043 only.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 14. Optional circuitry at CANH and CANL

6.1 Common mode choke

A common mode choke provides high impedance for common mode signals and low impedance for differential signals. Due to this, common mode signals produced by RF noise and/or by non-perfect transceiver driver symmetry get effectively attenuated while passing the choke. In fact, a common mode choke helps to reduce emission and to improve immunity against common mode disturbances without adding a large amount of distortion on CAN lines.

Former transceiver devices usually needed a common mode choke to fulfill the stringent emission and immunity requirements of the automotive industry when using unshielded twisted-pair cable. The entire 3rd generation high speed CAN transceivers have the potential to build in-vehicle bus systems without chokes. Whether a choke is needed or not finally depends on the specific system implementation like the wiring harness and the symmetry of the two bus lines (matching tolerances of resistors and capacitors).

Besides the RF noise reduction the stray inductance (non-coupled portion of inductance) may establish a resonant circuit together with pin capacitance. This can result in unwanted oscillations between the bus pins and the choke, both for differential and common mode signals, and in extra emission around the resonant frequency. To avoid such oscillations, it is highly recommended to use only chokes with stray inductance lower than 500nH. Bifilar wound chokes typically show an even lower stray inductance. Fig 14 shows an application, using a common mode choke. As shown the choke shall be placed nearest to the transceiver bus pins.

6.2 Capacitors

Matching capacitors (in pairs) at CANH and CANL to GND2 (CH and CL) are frequently used to enhance immunity against electromagnetic interference. Along with the impedance of corresponding noise sources (RF), capacitors at CANH and CANL to GND form an RC low-pass filter. Regarding immunity the capacitor value should be as large as possible to achieve a low corner frequency. The overall capacitive load and impedance of the output stage establish a RC low-pass filter for the data signals. The associated corner frequency must be well above the data transmission frequency. This results in a limit for the capacitor value depending on the number of nodes and the data transmission frequency. Notice that capacitors increase the signal loop delay due to reducing rise and fall times. Due to that, bit timing requirements, especially at 500kbit/s, call for a value of lower than 100pF (e.g. 63pF, see also SAE J2284 and ISO11898). At a bit rate of 125kbit/s the capacitor value should not exceed 470pF. Typically, the capacitors are placed between the common mode choke (if applied at all) and the optional ESD clamping diodes as shown in Fig 14.

6.3 ESD protection diodes

The 3rd generation high speed CAN transceivers is designed to withstand ESD pulses of up to

- ±8kV according to the IEC61000-4-2 and
- ±8kV according to the Human Body Model
- ±300V according to the Machine Model
- ±500V according to the Charged Device Model

at bus pins CANH, CANL and thus typically does not need further external measures. Nevertheless, if much higher protection is required, external clamping devices can be applied to the CANH and CANL line.

NXP Semiconductors offers a dedicated protection device for the CAN bus, providing high robustness against ESD and automotive transients. The so-called PESD1CAN [2] and PESD2CAN [3] protection devices featuring a very fast diode structure with very low capacitance (typ. 11pF), is compliant to IEC61000-4-2 (level 4), thus allowing air and contact discharge of more than 15kV and 8kV, respectively. Tests at an independent test house have confirmed typically more than 20kV ESD robustness for ECUs equipped with the PESD1CAN and a choke. To be most effective the PESD1CAN diode shall be placed close to the connector of the ECU as shown in Fig 14.

6.4 Power supply buffering

Emission and immunity of transceivers also depend on signal dynamic behaviour. The capacitors placed at voltage supply pins buffer the voltage and provide the sharp rise current needed during the transition from recessive to dominant state. To calculate the size of the capacitance please refers to chapter **3.1.2.2**.

6.5 Split termination concept

The transceiver is connected to the bus via pins CANH and CANL. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Practice has shown that effective reduction of emission can be achieved by a modified bus termination concept called split termination. Instead of a one-resistor termination it is highly recommended using the split termination, illustrated in Fig 15. In addition this concept contributes to higher immunity of the bus system.

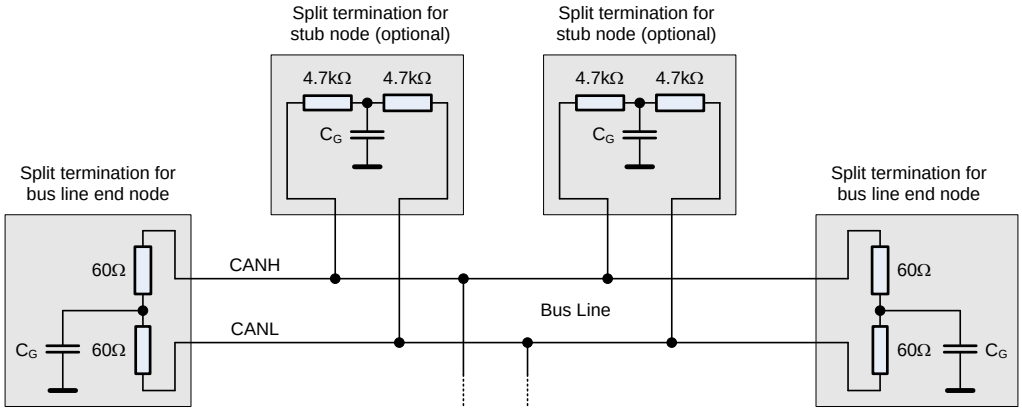


Fig 15. Typical split termination concept

Basically each of the two termination resistors of the bus line end nodes is split into two resistors of equal value, i.e. two resistors of 60Ω instead of one resistor of 120Ω. As an option, stub nodes, which are connected to the bus via stubs, can be equipped with a similar split termination configuration. The resistor value for the stub nodes has to be chosen such that the bus load of all the termination resistors stays within the specified range from 45Ω to 65Ω. As an example for up to 10 nodes (8 stub nodes and 2 bus end nodes) a typical resistor value is 4.7 kΩ. The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. Together with the resistors this termination concept works as a low pass filter. The recommended value for this capacitor is in the range of 4,7nF and 47nF.

In case of many high-ohmic stub nodes it can be considered to increase the main bus termination of 2 times 60Ω towards 2 times 62Ω or more. Since an automotive bus system is never “ideal” with respect to “beginning” and “end”, the overall termination is always a compromise. With that in mind, it might even be considered to have just one central bus termination in the star point of a system using 2 times 31Ω as an example.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: < 2 %).

Generally the termination strategy is prescribed by the individual OEM. Please refer to the corresponding specifications for details.

6.6 Summary of EMC improvements

The EMC performance of the 3rd generation high speed CAN transceivers has been optimized for use of the split termination without a choke. Hence, it is highly recommended to implement the split termination. The excellent output stage symmetry allows going without chokes as shown by different emission measurements. If, however, the system performance is still not sufficient, there will be the option to use additional measures like common mode chokes, capacitors and ESD clamping diodes.

7. Appendix

7.1 PIN FMEA

7.1.1 Failure Classification

This chapter provides an FMEA (Failure Mode and Effect Analysis) for typical failure situations, when dedicated pins of the isolated HS-CAN transceiver is short-circuited to supply voltages like V_{BAT}, V_{DD1}, V_{DD2}, GND1, 2 or to neighbored pins or simply left open. The individual failures are classified, due to their corresponding effects on the transceiver and bus communication in Table 12.

Table 12. Classification of failure effects

Class	Effects
A	- Damage to transceiver - Bus may be affected
B	- No damage to transceiver - No bus communication possible
C	- No damage to transceiver - Bus communication possible - Corrupted node excluded from communication
D	- No damage to transceiver - Bus communication possible - Reduced functionality of transceiver

7.1.2 FMEA TJA1052i

Table 13. TJA1052i FMEA matrix for pin short-circuits to VBAT and VCC

Pin	Short to V_{BAT} (12V … 400V)		Short to V_{DD1} (3 .. 5V) / V_{DD2} (5V)	
	Class	Remark	Class	Remark
(1) VDD1	A	Limiting value exceeded	-	-
(2) GND1	A	Limiting value exceeded	C	Undervoltage detected; TRX is left unpowered
(3) TXD	A	Limiting value exceeded	C	TXD clamped recessive
(4) nc	-	-	-	-
(5) RXD	A	Limiting value exceeded	C	RXD clamped recessive; Bus communication may be disturbed if Trx is transmitting
(6) nc	-	-	-	-
(7) GND1	A	Limiting value exceeded	C	Undervoltage detected; TRX is left unpowered
(8) GND1	A	Limiting value exceeded	C	Undervoltage detected; TRX is left unpowered
(9) GND2	A	Limiting value exceeded	C	VCC undervoltage detected; TRX goes to Sleep
(10) GND2	A	Limiting value exceeded	C	VCC undervoltage detected; TRX goes to Sleep
(11) VDD2	A	Limiting value exceeded	-	-
(12) CANL	B A	Vshort < 40V → No bus communication Vshort > 40V → Limiting value exceeded	B	No bus communication
(13) CANH	B A	Vshort < 40V → No bus communication Vshort < 40V → Limiting value exceeded	D	Degradation of EMC; Bit timing violation possible
(14) STB	A	Limiting value exceeded	D	Trx enters Standby mode
(15) GND2	A	Limiting value exceeded	C	VCC undervoltage detected; TRX goes to Sleep
(16) VDD2	A	Limiting value exceeded	-	-

Table 14. TJA1052i FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) VDD1	C	Undervoltage detected; TRX is left unpowered	C	Undervoltage detected; TRX is left unpowered
(2) GND1	-	-	C	Undervoltage detected; TRX is left unpowered if also pin 8 is open
(3) TXD	C	Trx is not able to transmit CAN messages;	C	Trx is not able to transmit CAN messages
(4) nc	-	-	-	-
(5) RXD	C	Trx is not able to provide received CAN messages;	C	Trx is not able to provide received CAN messages
(6) nc	-	-	-	-
(7) GND1	-	-	C	Undervoltage detected; TRX is left unpowered if also pin 2 & 8 are open
(8) GND1	-	-	C	Undervoltage detected; TRX is left unpowered if also pin 2 is open
(9) GND2	-	-	C	Undervoltage detected; TRX is left unpowered if also pin 15 is open
(10) GND2	-	-	C	Undervoltage detected; TRX is left unpowered if also pin 9 & 15 are open
(11) VDD2	C	Undervoltage detected; TRX is left unpowered	C	Undervoltage detected; TRX is left unpowered
(12) CANL	C	Degradation of EMC; Bit timing violation possible	C	Trx is not able to transmit or receive CAN messages; Bus communication may be disturbed if Trx is transmitting
(13) CANH	B	No bus communication	C	Trx is not able to transmit or receive CAN messages; Bus communication may be disturbed if Trx is transmitting
(14) STB	D	Standby mode not selectable	D	Pull-up to VDD2, Normal mode not selectable
(15) GND2	-	-	C	Undervoltage detected; TRX is left unpowered if also pin 9 is open
(16) VDD2	C	Undervoltage detected; TRX is left unpowered	C	Undervoltage detected; TRX is left unpowered

Table 15. TJA1052i FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
VDD1 – GND1	C	Undervoltage detected; TRX is left unpowered
GND1 – TXD	C	Trx is not able to transmit CAN messages
TXD – nc	-	-
RXD – nc	-	-
GND1 – nc	-	-
VDD2 – GND2	C	Undervoltage detected; TRX is left unpowered
GND2 – STB	D	Standby mode not selectable
STB – CANH	C	Trx is leaving Normal mode if the bus is driven dominant
CANH – CANL	B	No bus communication
CANL – VDD2	B	No bus communication
VDD2 – GND2	C	Undervoltage detected; TRX is left unpowered

7.2 PCB Footprint SO16WB (Reflow Soldering)

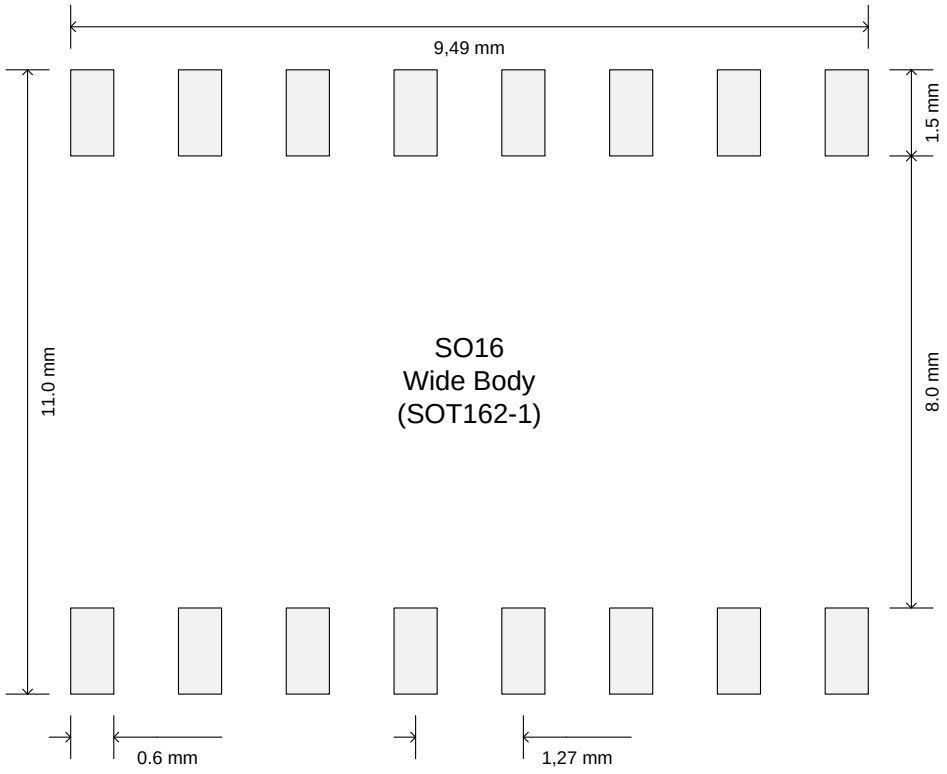


Fig 16. PCB Footprint dimensions (mm) [7]

8. References

[1] Product data sheet TJA1052i, Galvanic Isolated High-speed CAN transceiver – NXP Semiconductors, Rev. 04, 2009 Oct 20

[2] Product data sheet PESD1CAN, CAN bus ESD protection diode – NXP Semiconductors, Rev. 04, 2008 Feb 15

[3] Product data sheet PESD2CAN, CAN bus ESD protection diode – NXP Semiconductors, Rev. 01, 2006 Dec 22

[4] IEC60950-1:2005 (2nd Edition) – Information technology equipment – Safety; Part 1: General requirements

[5] IEC60664-1:2007 (2nd Edition) – Isolation coordination for equipment within low-voltage systems; Part 1: Principles, requirements and tests

[6] IEC 61010-1:2001 (2nd Edition) – Safety requirements for electrical equipment for measurement, control, and laboratory use; Part 1: General requirements

[7] SO & SOJ FOOTPRINT (REFLOW SOLDERING); Philips Semiconductors; 2001 Feb 19

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