Internal Peripheral Space Memory Map

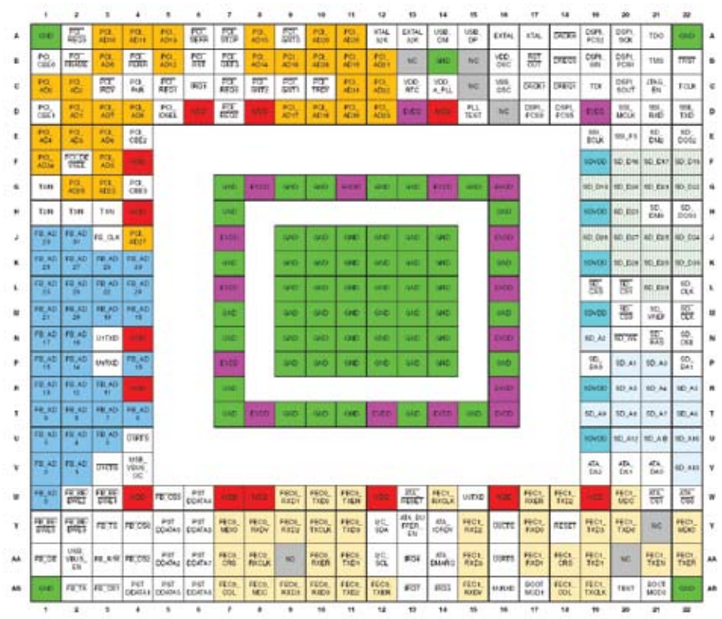
Base Address	Slot #	Peripheral
0xFC00_0000	0	SCM (MPR and PACRs)
0xFC00_4000	1	Cross-Bar Switch
0xFC00_8000	2	FlexBus
0xFC03_0000	12	FEC0
0xFC03_4000	13	FEC1
0xFC03_C000	15	Real-Time Clock
0xFC04_0000	16	SCM (CWT and Core Fault Registers)
0xFC04_4000	17	eDMA Controller
0xFC04_8000	18	Interrupt Controller 0
0xFC04_C000	19	Interrupt Controller 1
0xFC05_4000	21	Interrupt Controller IACK
0xFC05_8000	22	I²C
0xFC05_C000	23	DSPI
0xFC06_0000	24	UART0
0xFC06_4000	25	UART1
0xFC06_8000	26	UART2
0xFC07_0000	28	DMA Timer 0
0xFC07_4000	29	DMA Timer 1
0xFC07_8000	30	DMA Timer 2
0xFC07_C000	31	DMA Timer 3
0xFC08_0000	32	PIT 0
0xFC08_4000	33	PIT 1
0xFC08_8000	34	PIT 2
0xFC08_C000	35	PIT 3
0xFC09_4000	37	Edge Port
0xFC0A_0000	40	CCM, Reset Controller, Power Management
0xFC0A_4000	41	GPIO Module
0xFC0A_8000	42	PCI Controller
0xFC0A_C000	43	PCI Arbiter
0xFC0B_0000	44	USB On-the-Go
0xFC0B_4000	45	RNG
0xFC0B_8000	46	SDRAM Controller
0xFC0B_C000	47	SSI
0xFC0C_0000	48	ATA Controller
0xFC0C_4000	49	PLL

Default Jumper Locations

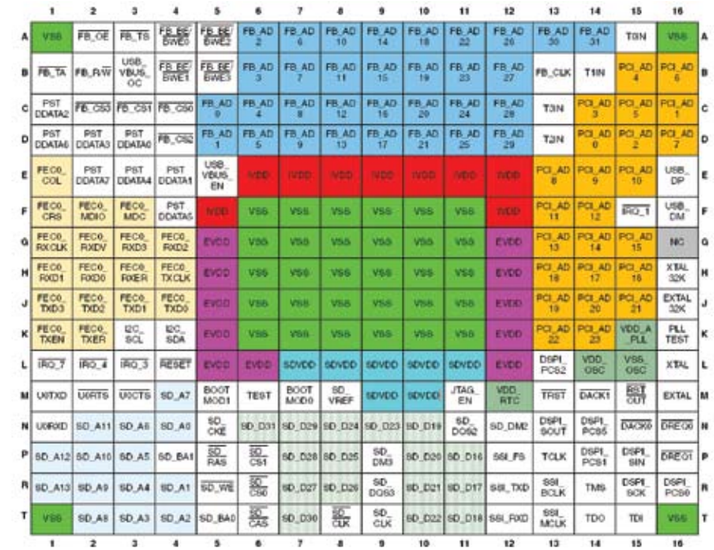
Option	Purpose	Default
PWR_SEL	+5V input source select	PWR
USB_CLK	ULPI clock enable	1-2
BOOT 0 /1	MCF54451 Boot mode	Installed
JTAG_EN	MCF54451 BDM Port Mode	Open
BDM_MODE	BDM_PORT Mode	2-3
JP1	MCF52211 U4_BDM Port Mode	Installed
JP2	U4 SPI Select	1-2
JP3	Serial Flash Select enable	Installed
JP4	Stereo CODEC SSI enable	Installed
JP5	+VDC enable	Installed
JP6	SDCARD Select	1-2
JP7	Stereo CODEC Select enable	Installed
JP8	10/100 PHY IRQ	Installed
JP9	FXO CODEC Select enable	Installed
JP10	FXS CODEC Select enable	Installed
JP11	FXO/FXS IRQ1 Enable	Installed
JP12	U4_BDM Mode	Open
JP13	MCF54451 3.3V	Installed
JP14	MCF54451 1.5V	Installed
JP15	MCF54451 1.8V	Installed
JP16	SDCARD IRQ Enable	Installed
U4_MODE1/2	U4 Application	Installed

System Memory Map

Internal Address[31:28]	Address Range	Destination Slave	Slave Memory Size
00xx	0x0000_0000–0x3FFF_FFFF	FlexBus	1024 MB
01xx	0x4000_0000–0x7FFF_FFFF	SDRAM Controller	1024 MB
1000	0x8000_0000–0x8FFF_FFFF	Internal SRAM	256 MB
1001	0x9000_0000–0x9FFF_FFFF	ATA Controller	256 MB
101x	0xA000_0000–0xBFFF_FFFF	PCI Controller	512 MB
110x	0xC000_0000–0xDFFF_FFFF	FlexBus	512 MB
1110	0xE000_0000–0xEFFF_FFFF	Reserved	256 MB
1111	0xF000_0000–0xFFFF_FFFF	Internal Peripheral Space	256 MB



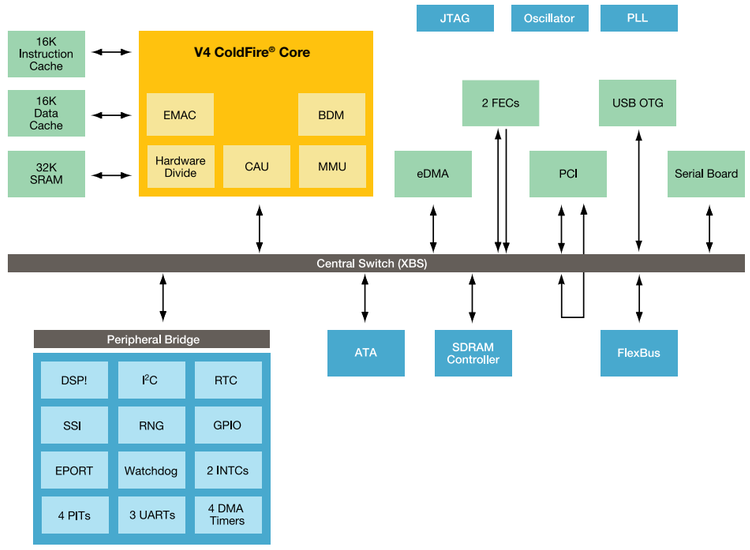
MCF54452, MCF54453, MCF54455, and MCF54455 Pinout (360 TEPBGA)



MCF54450 and MCF54451 Pinout (256 MAPBGA)

MCF5445x Family Configurations

Module	MCF54450	MCF54451	MCF54452	MCF54453	MCF54454	MCF54455
V4 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit)	X	X	X	X	X	X
Core (System) Clock	up to 240 MHz		up to 266 MHz			
Peripheral Bus Clock (Core Clock ÷ 2)	up to 120 MHz		up to 133 MHz			
External Bus Clock (Core Clock ÷ 4)	up to 60 MHz		up to 66 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 370 MIPS		up to 410 MIPS			
Independent Data/Instruction Cache	16 KB each					
Static RAM (SRAM)	32 KB					
PCI Controller	-	-	X	X	X	X
Cryptography Acceleration Unit (CAU)	-	X	-	X	-	X
ATA Controller	-	-	-	-	X	X
DD R SDRAM Controller	X	X	X	X	X	X
FlexBus External Interface	X	X	X	X	X	X
USB 2.0 On-the-Go	X	X	X	X	X	X
UTMI+ Low Pin Interface (ULPI)	X	X	X	X	X	X
Synchronous Serial Interface (SSI)	X	X	X	X	X	X
Fast Ethernet Controller (FEC)	1	1	2	2	2	2
UARTs	3	3	3	3	3	3
I²C	X	X	X	X	X	X
DSPI	X	X	X	X	X	X
Real-Time Clock	X	X	X	X	X	X
32-bit DMA Timers	4	4	4	4	4	4
Watchdog Timer (WDT)	X	X	X	X	X	X
Periodic Interrupt Timers (PIT)	4	4	4	4	4	4
Edge Port Module (EPORT)	X	X	X	X	X	X
Interrupt Controllers (INTC)	2	2	2	2	2	2
16-channel Direct Memory Access (DMA)	X	X	X	X	X	X
General Purpose I/O Module (GPIO)	X	X	X	X	X	X
JTAG—IEEE® 1149.1 Test Access Port	X	X	X	X	X	X
Package	256 MAPBGA		360 TEPBGA			



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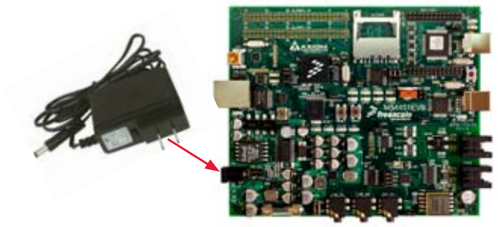
Quick Start Guide

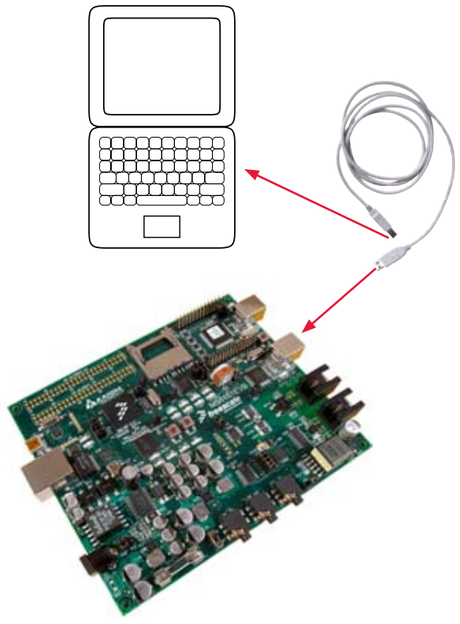
ColdFire® M54451EVB
Board Connection/Setup

The M54451EVB comes pre-programmed with U-Boot and Linux preconfigured to run a demo application. This section describes how to setup the evaluation board to access the bootloader how to start Linux. The default communication interface with the M54455EVB is a simple serial port console. A terminal emulator on a host PC and the supplied serial cable is required to interact with the serial port.

STEP 1 Plug in power cable and turn power switch on.

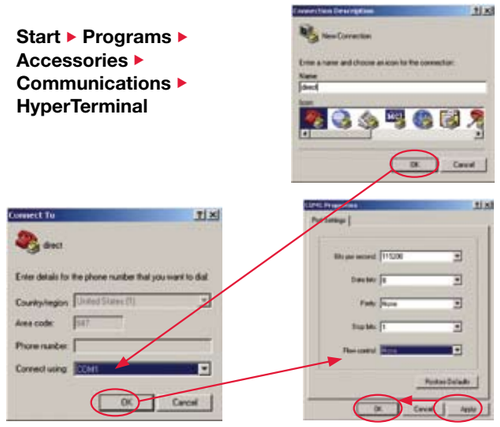


STEP 2 Connect the USB cable connector to the board (J3).



STEP 3 Open and configure HyperTerminal as follows making sure to select the appropriate COM port assigned to the board

Start ▸ Programs ▸ Accessories ▸ Communications ▸ HyperTerminal



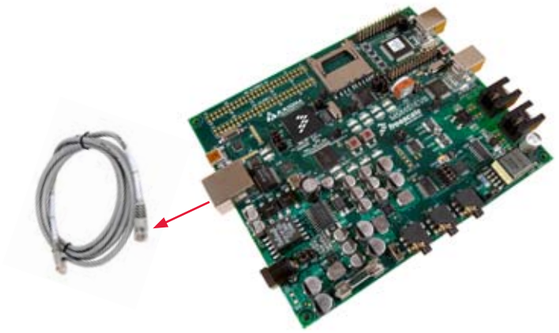
If HyperTerminal shows "Auto-detect" then it did not configure correctly. Select the phone icon to disconnect, then go to files ▸ properties in the HyperTerminal window, click on the configure button which will open a panel like the "COM1 Properties" above. Verify the configuration is as pictured above, then select OK. Then just hit enter in the HyperTerminal Window.

This is what the status bar under the HyperTerminal window should look like.

Parameter	Setting
Baud rate	115200 bps
Data bits	8
Parity	None
Stop bits	1
Flow control	None

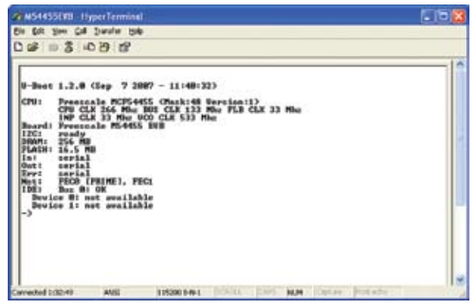
STEP 4 Connect the Ethernet cable

Plug one end of the provided Ethernet cable into a network or host PC with a DHCP server running. Plug the other end of the cable into the Ethernet connector of the M54451EVB.



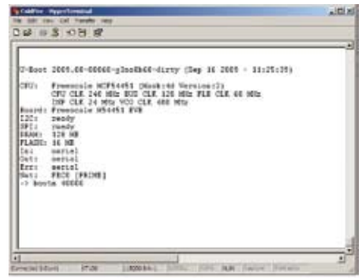
STEP 5 Press reset button near the center of the M54451EVB, verify splash screen on HyperTerminal

The U-Boot banner (example below) should appear in the terminal window.



STEP 6 To Boot Linux, issue the following U-Boot command

Type command –> bootm 40000



STEP 7 The M54451EVB will serve up a Web page with more information on the available demos

At the command prompt type 'ifconfig' then press return.

The demo application will print out a banner message to the serial terminal including the IP address that it obtained from the DHCP server. Launch a Web client (e.g. Firefox or Internet Explorer) and copy the internet address into the web browser appending /index.html.

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