KM3x – Metrology MCUs based on Arm® Cortex®-M0+ Core

Up to 512 KB Flash and 64 KB SRAM

1. KM MCU Series

KM metering MCUs expand the successful line of NXP MCUs portfolio based on the Arm® Cortex™-M0+ core. The KM series supports low-cost, highly integrated solutions for one-, two-, and three- phase meters with a high accuracy sigma-delta ADC metering front end.

KM metering MCUs address specific regional needs including neutral disconnect or split phase for North America and Japan. Full metrology software, including time or filter based, is provided as well as fast Fourier transform. These devices include high electrostatic discharge immunity with high accuracy RTC with less than 5 ppm drift over temperature.

Standard Tower System boards and regional reference designs with complete software libraries are available for design evaluation.

2. KM3x MCU Family

The KM3x MCU family adds a segment LCD controller in addition to the KM1x series. The KM3x MCU family includes KM33 and KM34 and KM35 with the key difference of 24 bit sigma- delta model number to address metering requirement from different region.

- KM33 – With up to 50 MHz Cortex M0+ core, up to 128 KB flash and 16 KB SRAM, featuring 3x 24-

Contents

bit sigma-delta ADC models, 16-bit SAR ADC, and high accuracy internal VREF. Up to 100 pins package offering 36x8/40x4 segment LCD

- KM34 – With up to 75MHz Cortex M0+ core, up to 256 KB Flash and 32 KB SRAM, featuring 4x 24-bit sigma-delta ADC models, 16-bit SAR ADC, and high accuracy internal VREF. Up to 144 pins package offering 56x8/ 58x6/ 60x4 segment LCD

- KM35 – With up to 75MHz Cortex M0+ core, up to 512 KB Flash and 64 KB SRAM, featuring 4x 24-bit sigma-delta ADC models, 16-bit SAR ADC, and high accuracy internal VREF. Up to 144 pins package offering 56x8/ 58x6/ 60x4 segment LCD

3. KM3x MCU Family Key Features

- Core
    - Arm® Cortex®-M0+ core up to 75 MHz
    - Memory-mapped Arithmetic Unit (MMAU)
    - Memory Mapped Cryptographic Acceleration Unit(MMCAU)
- Memories
    - 128 KB to 512 KB program flash memory
    - 16 KB to 64 KB SRAM
- Clocks
    - FLL and PLL
    - 4 MHz internal reference clock
    - 32 kHz internal reference clock
    - 1 kHz LPO clock
    - 32.768 kHz crystal oscillator in iRTC power domain
    - 1 MHz to 32 MHz crystal oscillator
- Low power features
    - 13 power modes to provide power optimization based on application requirements
    - 8.82 mA @ 75 MHz run current
    - Less than 124.4 µA/MHz very low power run current
    - 6.05 µA very low power stop current
    - Down to 357 nA deep sleep current
    - VBAT domain current < 1 µA with iRTC operational
    - Low-power boot with less than 2.33 mA peak current
- System peripherals
    - Memory Protection Unit (MPU)

- 4-channel DMA controller
- Watchdog and EWM
- Low-leakage Wakeup Unit (LLWU)
- SWD debug interface and Micro Trace Buffer (MTB)
- Bit Manipulation Engine (BME)
- Inter-peripheral Crossbar Switch (XBAR)
- Analog
  - Up to 4 AFE channels (4× 24-bit Sigma Delta ADCs with PGA)
  - 16-channel 16-bit SAR ADC with 4 result registers
  - High-speed analog comparator containing a 6-bit DAC and programmable reference input
  - Internal 1.2 V reference voltage 10–15 ppm/$℃°$
- Communication interfaces
  - 16-bit SPI modules
  - Low power UART module
  - UART module complying with ISO7816-3
  - Basic UART module
  - I2C with SMBus
- Timers
  - Quad Timer
  - Periodic Interrupt Timer (PIT)
  - Low Power Timer (LPTMR)
  - Programmable Delay Block (PDB)
  - Watchdog Timer
  - External Watchdog Monitor (EWM)
  - Independent Real Time Clock (iRTC)
- Human machine interface
  - Up to 4×60 (8×56, 6×58) segment LCD controller operating in all low-power modes
  - General purpose input/output (GPIO)
- Security and integrity modules
  - Memory Mapped Cryptographic Acceleration Unit (MMCAU) for AES encryption
  - Random Number Generator (RNGA), complying with NIST: SP800-90
  - Cyclic Redundancy Check (PCRC)

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- 80-bit unique identification number per chip
- Operating conditions
  - Voltage range: 1.71 to 3.6 V (without AFE)
  - Voltage range: 2.8 to 3.6 V (with AFE)
  - iRTC battery supply voltage range: 1.71 to 3.6 V
  - Temperature range: –40 to 105 °C
- Packages
  - 144-pin LQFP 20×20 mm 0.5 mm pitch
  - 100-pin LQFP 14×14 mm 0.5 mm pitch

4. KM3x MCU Family Feature Summary

Sub-Family	KM33	KM34Z128	KM34Z256	KM35Z256	KM35Z512
CPU Frequency	50MHz	50MHz	75MHz	75MHz	75MHz
Memory-mapped Arithmetic Unit (MMAU)	-	-	Yes	Yes	Yes
Flash Memory	64-128 KB	128 KB	256 KB	256 KB	512 KB
SRAM	16 KB	16 KB	32 KB	64 KB	64 KB
Memory Mapped Cryptographic Acceleration Unit (MMCAU)	-	-	Yes	Yes	Yes
Inter Peripheral Crossbar In/Out Pin	5/5 - 9/9	9/9	9/9 - 11/11	9/9 - 11/11	9/9 - 11/11
Segment LCD	20x8/ 22x6/ 24x4 – 36x8/38x6/40x4	36x8/ 38x6/ 40x4	36x8/ 38x6/ 40x4 – 56x8/58x6/60x4	36x8/ 38x6/ 40x4 – 56x8/58x6/ 60x4	36x8/ 38x6/ 40x4 - 56x8/ 58x6/ 60x4
Analog	24bit ADC, 16bit ADC,PGA, CMP w/ 6bit DAC, VREF	24bit ADC, 16bit ADC,PGA, CMP w/ 6bit DAC, VREF	24bit ADC, 16bit ADC,PGA, CMP w/ 6bit DAC, VREF	24bit ADC, 16bit ADC,PGA, CMP w/ 6bit DAC, VREF	24bit ADC, 16bit ADC,PGA, CMP w/ 6bit DAC, VREF

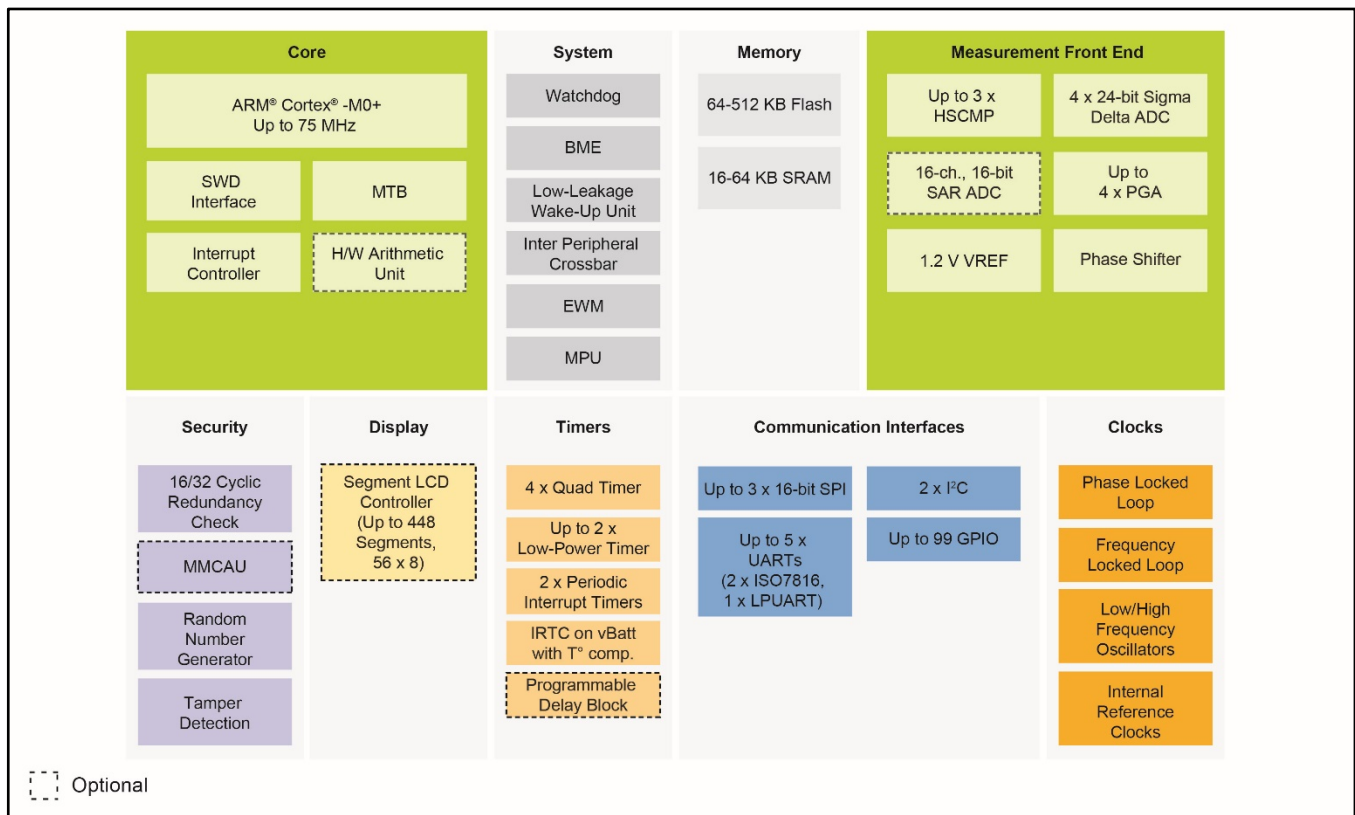| Connectivity	UART w/ ISO7816, SPI, I2C	UART w/ ISO7816, SPI, I2C	UART w/ ISO7816, LPUART, SPI, I2C	UART w/ ISO7816, LPUART, SPI, I2C	UART w/ ISO7816, LPUART, SPI, I2C
Package	64LQFP, 100LQFP	100LQFP	100LQFP, 144LQFP	100LQFP, 144LQFP	100LQFP, 144LQFP

5. KM3x MCU Family Block Diagram

Figure 1 KM3x MCU Family Block Diagram

6. KM3x MCU Family Common Features

The following features are present on all KM3x MCUs:

- 2-pin serial wire debug (SWD), micro trace buffer (MTB)
- 4-channel DMA controller
- Integrated bit manipulation engine (BME)

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- Random number generator

- Low- and high-frequency OSC

- iRTC, with 32KHz OSC, tamper detection and temperature compensation

- 4ch Quad Timer, 2 PIT, LPTMR

- High-speed analog comparator containing a 6-bit DAC for programmable reference input

- Power management controller (PMC) with nine power modes

- Non-maskable interrupt (NMI)

- Software and COP watchdog

- 80-bit unique identification number per chip

- Voltage range 1.71 V – 3.6 V

- Temperature range (TA) -40°C – 105°C

7. KM3x MCU Family Differences

Table 1 KM3x MCU family differences

	Subfamily	KM33	KM34Z128	KM34Z256	KM35Z256	KM35Z512
Core	**Frequency**	50MHz	50MHz	75MHz	75MHz	75MHz
	Memory Mapped Arithmetic Unit (MMAU)	–	–	Yes	Yes	Yes
	Flash / SRAM Size	64 KB/16 KB - 128 KB/16 KB	128 KB/16 KB	256 KB/32 KB	256 KB/64 KB	512 KB/64 KB
Communication	**LPUART**	–	–	1	1	1
	UART	2	2	2	2	2
	UART w/ ISO7816	2	2	2	2	2
	SPI	2	2	2	3	3
	I2C	2	2	2	2	2
Analog Modules	**24-bit Sigma Delta ADC (PGA number)**	3(2)	4(2)	4(4)	4(4)	4(4)
	16-bit ADC (channels)	1(7 - 12)	1(12)	1(12 - 16)	1(12 - 16)	1(12 - 16)
	CMP w/ 6bit DAC	2	2	3	3	3
Other	**Inter Peripheral Crossbar In/Out Pin**	5/5 - 9/9	9/9	9/9 - 11/11	9/9 - 11/11	9/9 - 11/11
	MMCAU	–	–	Yes	Yes	Yes
	Segment LCD	20x8/ 22x6/ 24x4 – 36x8 /38x6 /40x4	36x8/ 38x6/ 40x4	36x8/ 38x6/ 40x4 - 56x8/ 58x6/ 60x4	36x8/ 38x6/ 40x4 - 56x8/ 58x6/ 60x4	36x8/ 38x6/ 40x4 - 56x8/ 58x6/ 60x4

Total GPIOs	38/68	68	72/99	72/99	72/99
Package	64LQFP, 100LQFP	100LQFP	100LQFP, 144LQFP	100LQFP, 144LQFP	100LQFP, 144LQFP

8. Comprehensive enablement solutions

8.1. Integrated development environments

- IAR Embedded Workbench® iar.com/kinetis

- Arm Keil® Microcontroller Development Kit keil.com/nxp

- NXP MCUXpresso nxp.com/mcuxpresso

  - An open-source software development kit (SDK)

  - An easy-to-use integrated development environment (IDE)

  - A comprehensive suite of system configuration tools, including pins, clocks, SDK builder and more

  - Broad Arm ecosystem support through NXP Connect partners

8.2. Development hardware

NXP Tower System development board platform is a modular development platform for 8-bit, 16- bit, and 32-bit microcontrollers that enable advanced development through rapid prototyping. Featuring multiple development boards or modules, the Tower System development board platform provides designers with building blocks for entry-level to advanced microcontroller development.

J27 Power/ OpenSDA Micro USB
J26 K20 JTAG Header
SW4 Reset Button
D2 Yellow LED
SW1
J23 TWRPI
J31 PWM Header
J22 TWRPI

DS1 Segment LCD
SW3
J25 GPIO Header
U12 MKM35Z512VLQ7
J24 KM35 JTAG/ SWD
D3/D4/D5 LEDs
IRDA
SW2

U5 Accelerometer MMA8451Q
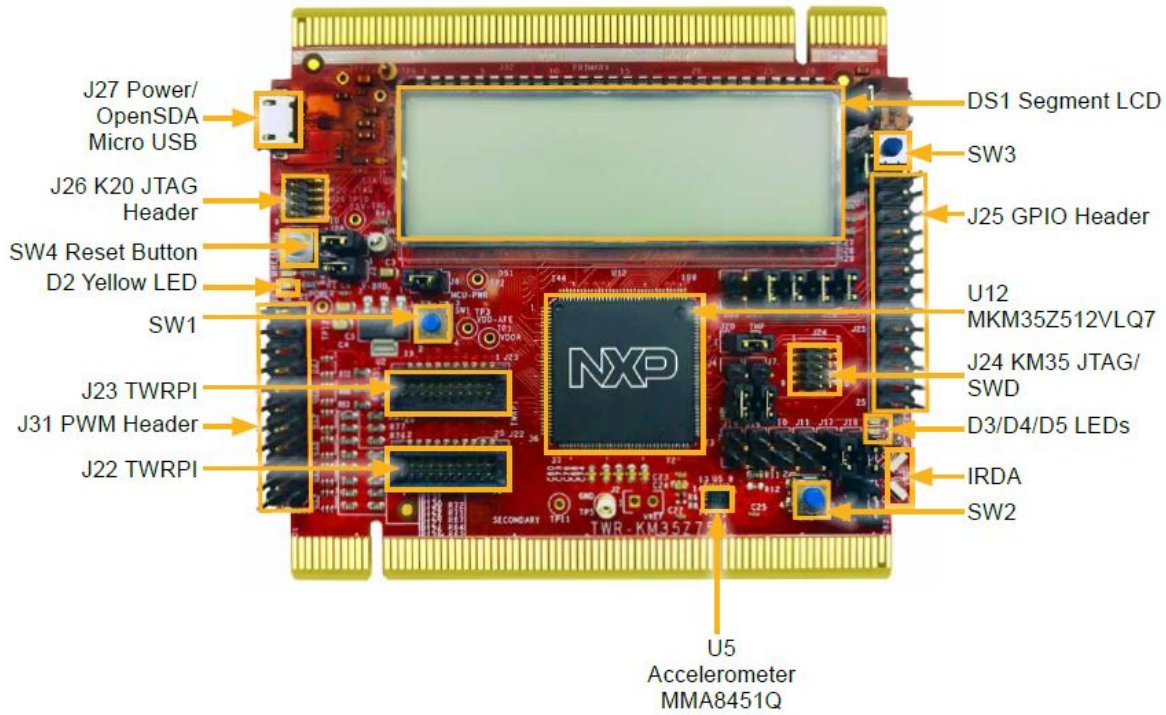
Figure 2 NXP Tower System development board platform

R21 Potentiometer
U4 SPI NOR Flash

U6 K20 OpenSDA
Battery Receptacle

Tower-compatible microcontroller module

- USB interface with Mini-B/Micro-B USB connector
- Large 160-seg. glass LCD
- On-board debug circuit: open source SWD (OpenSDA) with virtual serial port
- Three-axis accelerometer/anti tamper tilt sensor (MMA8451Q)

- Four user-controllable LEDs
- Two user pushbutton switches for GPIO interrupts
- One user pushbutton switch for tamper detection
- One user pushbutton switch for MCU reset
- Potentiometer
- Headers for direct GPIO and ADC access
- External Tamper pins
- Independent, battery-operated power supply for Real Time Clock (RTC) and tamper detection modules
- IRDA support
- NTC temperature sensor
- General-purpose Tower Plug-in (TWRPI) socket

9. Part identification

9.1. Description

The chip part numbers have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

9.2. Format

The device part numbers have the following format: Q KM## A FFF T PP CC (N)

9.3. Fields

The following table lists the possible values for each field in the part number. However, not all combinations are valid.

Table 2 Part number field descriptions

Field	Description	Values
Q	Qualification status	M = Fully-qualified, general market flow P = Prequalification
KM##	K family	KM33 KM34 KM35
A	Key attribute	Z = Cortex-M0+

FFF	Program Flash memory size	64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB
R	Silicon revision	(Blank) = Main A = Revision after main
T	Temperature range	C = =40°C – 85°C V = -40°C – 105°C
PP	Package identifier	LH = 64LQFP (10mm × 10mm × 1.4mm, Pitch 0.5mm) LL = 100LQFP (14mm x 14mm × 1.7mm, Pitch 0.5mm) LQ = 144LQFP (20mm x 20mm x 1.6mm, Pitch 0.5mm)
CC	Maximum CPU frequency (MHz)	5 = 50 MHz 7 = 75 MHz
N	Packaging type	R = Tape and reel (Blank) = Trays

10. Orderable part numbers

Table 3 Ordering information

Product	Core and Security			Memory		Package		Analog and HMI			
MC Part number	Frequency	MMAU	MMCAU	Flash (KB)	SRAM (KB)	Pin Count	Package	24 bit Sigma Delta ADC (PGA number)	Comparator	LCD Segments	GPIOs
MKM33Z64ACLH5	50MHz	-	-	64	16	64	LQFP	3(2)	2	20x8/22x6/24x4	38
MKM33Z64ACLL5	50MHz	-	-	64	16	100	LQFP	3(2)	2	36x8/38x6/40x4	68
MKM33Z128ACLH5	50MHz	-	-	128	16	64	LQFP	3(2)	2	20x8/22x6/24x4	38
MKM33Z128ACLL5	50MHz	-	-	128	16	100	LQFP	3(2)	2	36x8/38x6/40x4	68
MKM34Z128ACLL5	50MHz	-	-	128	16	100	LQFP	4(2)	2	36x8/38x6/40x4	68
MKM34Z256VLL7	75MHz	Yes	Yes	256	32	100	LQFP	4(4)	3	36x8/ 38x6/ 40x4	72
MKM34Z256VLQ7	75MHz	Yes	Yes	256	32	144	LQFP	4(4)	3	56x8/ 58x6/ 60x4	99
MKM35Z512VLL7	75MHz	Yes	Yes	512	64	100	LQFP	4(4)	3	36x8/ 38x6/ 40x4	72
MKM35Z512VLQ7	75MHz	Yes	Yes	512	64	144	LQFP	4(4)	3	56x8/ 58x6/ 60x4	99
MKM35Z256VLL7	75MHz	Yes	Yes	256	64	100	LQFP	4(4)	3	36x8/ 38x6/ 40x4	72
MKM35Z256VLQ7	75MHz	Yes	Yes	256	64	144	LQFP	4(4)	3	56x8/ 58x6/ 60x4	99

11. Revision history

Revision number	Date	Substantive changes
0	06/2015	Initial release
1	04/2020	Added KM35