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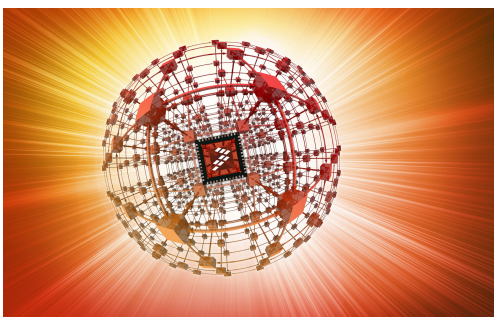
KL03 Product Brief

Supports all KL03 devices



Contents

1 KL03 sub-family introduction

The device is highly-integrated, market leading ultra low-power 32-bit microcontroller based on the enhanced Cortex-M0+ (CM0+) core platform. The features of the KL03 family derivatives are as follows.

- Core platform clock up to 48 MHz, bus clock up to 24 MHz
- Memory option is up to 32 KB flash, 2 KB RAM and 8 KB ROM with build-in boot loader
- Wide operating voltage ranges from 1.71–3.6 V with fully functional flash program/erase/read operations
- Multiple package options from 16-pin to 24-pin
- Ambient operating temperature ranges from –40 °C to 85 °C for WLCSP package and –40 °C to 105 °C for all the other packages.

The family acts as an ultra low-power, cost-effective microcontroller to provide developers an appropriate entry-level 32-bit solution. The family is the next-generation MCU solution for low-cost, low-power, high-performance devices applications. It’s valuable for cost-sensitive, portable applications requiring long battery life-time.

2 Key feature

- Operating conditions

    - Voltage range: 1.71 to 3.6 V
    - Temperature range: -40 to 105 °C for QFN packages and -40 to 85 °C for WLCSP package
- Packages
    - 24-pin QFN 4x4 mm 0.5 mm pitch
    - 20-pin WLCSP 2x1.6 mm 0.5 mm pitch
    - 16-pin QFN 3x3 mm 0.5 mm pitch
- Core
    - ARM Cortex-M0+ core up to 48 MHz
- Memories
    - Up to 32 KB program flash memory
    - 2 KB SRAM
    - 8 KB ROM with build-in boot loader
- Clocks
    - 48 MHz high accuracy internal reference clock
    - 8/2 MHz low power internal reference clock
    - 32 kHz to 40 kHz crystal oscillator
    - 1 kHz LPO clock
- Low power features (refer to the KL03 Data Sheet for the accurate power consumption data)
    - 9 low power modes to provide power optimization based on application requirements
    - 209 µA at 4 MHz Very-Low-Power-Run mode (code running in SRAM)
    - 121 µA at Very-Low-Power-Wait mode
    - 2.2 µA at Very-Low-Power-Stop mode
    - 566 nA at Very-Low-Leakage-Stop mode with system register files retained
- System peripherals
    - Watchdog
    - SWD debug interface and Micro Trace Buffer
    - Bit Manipulation Engine
    - Low power wakeup unit
    - Supporting boot up from ROM to program flash array through I2C, LPUART and SPI
    - Optional reset into VLPR mode controlled by flash configuration field bit
- Analog
    - 12-bit SAR ADC with internal voltage reference, up to 1Msps and 7 channels
    - High-speed analog comparator containing a 6-bit DAC and programmable reference input
    - High precision 1.2 V VREF
- Communication interfaces
    - One 8-bit SPI module
    - One low power UART module
    - One I2C modules supporting up to 1 Mb/s, with double buffer
- Timers
    - Two 2-channel Timer/PWM modules
    - One low power timer
    - Real time clock
- Human machine interface
    - General purpose input/output up to 22
- Security and integrity module
    - 80-bit unique identification number per chip

3 Block diagram

The following figure shows a superset block diagram of the device. Other devices within the family have a subset of the features.

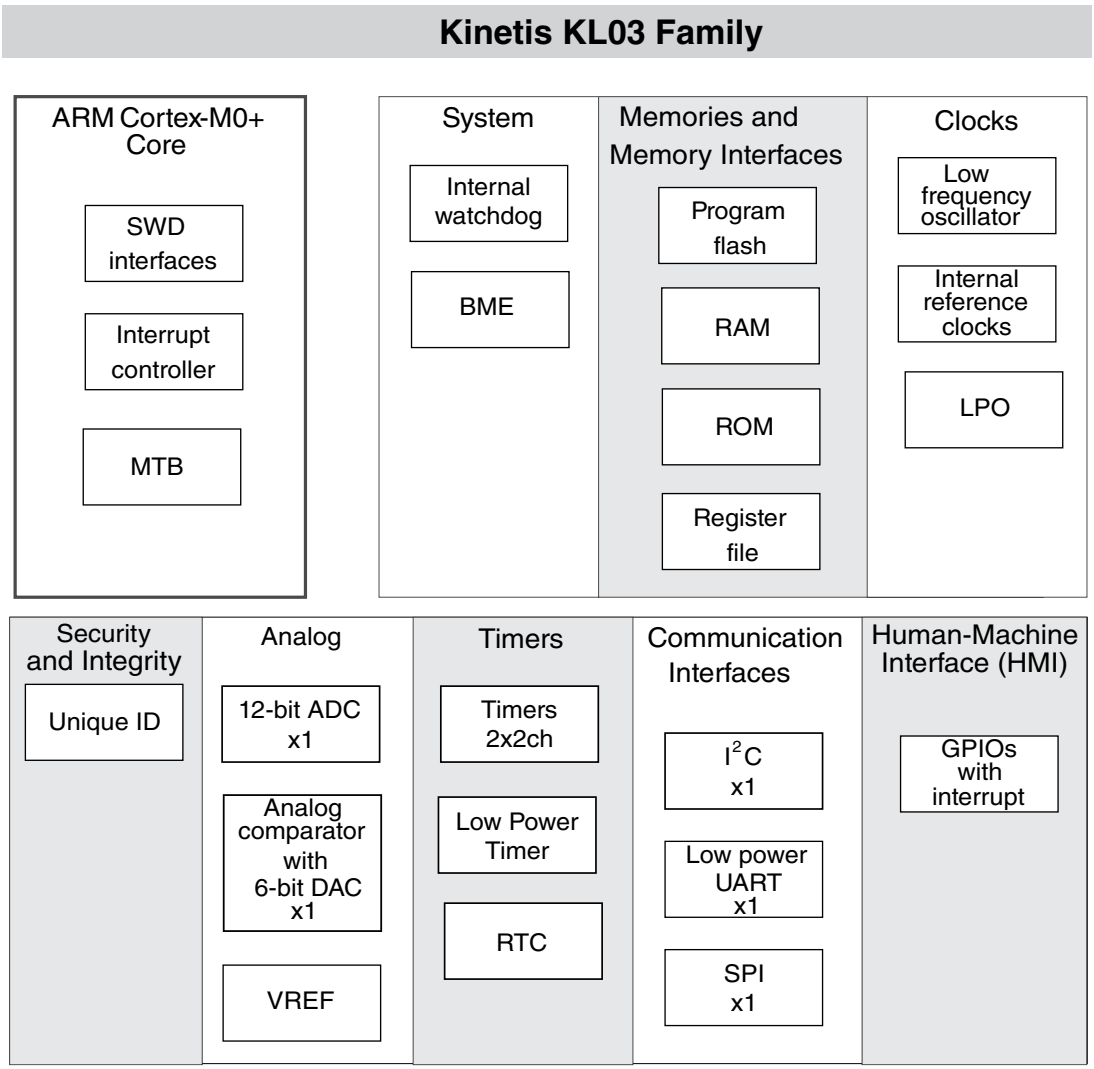


Figure 1. KL03 family block diagram

4 Features

4.1 High level feature comparison

Table 1. High level feature comparison

Features	KL03
CPU Frequency	48 MHz
Flash Memory	Up to 32 KB
SRAM	2 KB
USB Slave FS	—
USB Vreg	—

Table continues on the next page...

Table 1. High level feature comparison (continued)

Features	KL03
Segment LCD	—
16-pin QFN	Yes
24-pin QFN	Yes
20-pin WLCSP	Yes

4.2 Common features

Table 2. KL03 common features

Core/System Modules			Timers Modules	
Core	ARM Cortex-M0+		General Purpose Timer/PWM	2x2ch
CPU Frequency	48 MHz		Low Power Timer	1
DMA	-		PIT (32-bit)	-
Bit Manipulation Engine	Yes		Communication interface	
Debug	SWD		Low Power UART	1
Trace	MTB		UART w/ ISO7816-3	-
LLWU	-[1]		UART	-
Memories			8-bit SPI	1
Flash	up to 32 KB		I2C	1
SRAM	2 KB		I2S	-
ROM	up to 8 KB		USB Slave FS	-
Regfile	16 bytes		USB Vreg	-
Clock Modules			Human Machine Interface	
MCG-Lite	Yes		Segment LCD	-
Main OSC	32 - 40 kHz		Open drain pads with 5 V tolerance	2
RTC	Yes		NMI	Yes
Embedded USB Clock Generator	-		Total GPIOs	up to 22
Security and Integrity			GPIOs w/ Interrupt	up to 12
Watchdog	Yes		High Current GPIOs	3
Analog Modules			Operating Characteristics	
ADC	1x 12-bit SAR, up to 7 ch		Voltage Range	1.71 V - 3.6 V
Analog Comparator	1, 6-bit DAC, up to 5-ch		Flash Write Voltage	1.71 - 3.6 V
VREF	1.2 V		Temp Range	• -40 to 85 °C for WLCSP, • -40 to 105 °C for all the others

1. KL03 has two LLWU pins, but it has no LLWU module.

4.3 Feature differences per package

Package	16-pin QFN	20-pin WLCSP	24-pin QFN
Flash	up to 32 KB	32 KB	up to 32 KB
SRAM	2 KB	2 KB	2 KB
Segment LCD	—	—	—
Total GPIOs	up to 14	up to 18	up to 22
GPIOs w/ Interrupt	9	10	12
High Current GPIOs	3	3	3

4.4 Orderable part numbers

The following table summarizes the part numbers of the devices covered by this document.

Table 4. Orderable part numbers summary

Freescale part number	CPU frequency	Pin count	Package	Total flash memory	RAM	Temperature range
MKL03Z8VFG4(R)	48 MHz	16	QFN	8 KB	2 KB	-40 to 105 °C
MKL03Z16VFG4(R)	48 MHz	16	QFN	16 KB	2 KB	-40 to 105 °C
MKL03Z32VFG4(R)	48 MHz	16	QFN	32 KB	2 KB	-40 to 105 °C
MKL03Z8VFK4(R)	48 MHz	24	QFN	8 KB	2 KB	--40 to 105 °C
MKL03Z16VFK4(R)	48 MHz	24	QFN	16 KB	2 KB	-40 to 105 °C
MKL03Z32VFK4(R)	48 MHz	24	QFN	32 KB	2 KB	-40 to 105 °C
MKL03Z32CAF4R	48 MHz	20	WLCSP	32 KB	2 KB	-40 to 85 °C

4.5 Power modes

The Power Management Controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide partial power-down or full power-down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For each run mode, there is a corresponding Wait and Stop mode. Wait modes are similar to ARM Sleep modes. Stop modes (VLPS, STOP) are similar to ARM Sleep Deep mode. The Very Low Power Run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are Run, Wait, and Stop. The WFI instruction invokes both Wait and Stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 5. Chip power modes

Chip mode	Description	Core mode	Normal recovery method
Normal Run	Allows maximum performance of chip. • Default mode out of reset • On-chip voltage regulator is on.	Run	—
Normal Wait - via WFI	Allows peripherals to function while the core is in Sleep mode, reducing power. • NVIC remains sensitive to interrupts • Peripherals continue to be clocked.	Sleep	Interrupt
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection. • NVIC is disabled. • AWIC is used to wake up from interrupt. • Peripheral clocks are stopped.	Sleep Deep	Interrupt
VLPR (Very Low-Power Run)	On-chip voltage regulator is in a low-power mode that supplies only enough power to run the chip at a reduced frequency. Only MCG-Lite modes LIRC and EXT can be used in VLPR. • Reduced frequency Flash access mode (1 MHz) • LVD off • In LIRC clock mode, only the internal reference oscillator (LIRC8M) is available to provide a low power nominal 4 MHz source for the core with the nominal bus and flash clock required to be <1 MHz • Alternatively, EXT clock mode can be used with an external clock or the crystal oscillator providing the clock source.	Run	—
VLPW (Very Low-Power Wait) -via WFI	Same as VLPR but with the core in Sleep mode to further reduce power. • NVIC remains sensitive to interrupts (FCLK = ON). • On-chip voltage regulator is in a low-power mode that supplies only enough power to run the chip at a reduced frequency.	Sleep	Interrupt
VLPS (Very Low-Power Stop)-via WFI	Places chip in static state with LVD operation off. Lowest power mode with ADC and pin interrupts functional. • Peripheral clocks are stopped, but OSC, LPTMR, RTC, CMP can be used. • LPUART and TPM can optionally be enabled if their clock source is enabled. • NVIC is disabled (FCLK = OFF); AWIC is used to wake up from interrupt. • On-chip voltage regulator is in a low-power mode that supplies only enough power to run the chip at a reduced frequency. • All SRAM is operating (content retained and I/O states held).	Sleep Deep	Interrupt
VLLS3 (Very Low-Leakage Stop3)	• Most peripherals are disabled (with clocks stopped), but OSC, LLWU, LPTMR, RTC, CMP can be used. • NVIC is disabled; LLWU is used to wake up. • SRAM_U and SRAM_L remain powered on (content retained and I/O states held).	Sleep Deep	Wake-up Reset[1]
VLLS1 (Very Low-Leakage Stop1)	• Most peripherals are disabled (with clocks stopped), but OSC, LLWU, LPTMR, RTC, CMP can be used. • NVIC is disabled; LLWU is used to wake up.	Sleep Deep	Wake-up Reset[1]

Table continues on the next page...

Table 5. Chip power modes (continued)

Chip mode	Description	Core mode	Normal recovery method
	• All of SRAM_U and SRAM_L are powered off. • The 16-byte system register file remains powered for customer-critical data		
VLLS0 (Very Low-Leakage Stop 0)	• Most peripherals are disabled (with clocks stopped), but LLWU, LPTMR, RTC can be used. • NVIC is disabled; LLWU is used to wake up. • All of SRAM_U and SRAM_L are powered off. • The 16-byte system register file remains powered for customer-critical data • LPO disabled, optional POR brown-out detection	Sleep Deep	Wake-up Reset[1]

1. Follows the reset flow with the LLWU interrupt flag set for the NVIC.

4.6 Module-by-module feature list

The following sections describe the high-level module features for the family's superset device. See Common features for differences among the subset devices.

4.6.1 Core modules

4.6.1.1 ARM Cortex M0+ core

- Up to 48 MHz core frequency from 1.71 V to 3.6 V across temperature range of –40 °C to 105 °C
- Support up to 32 interrupt request sources
- 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the CM0 core
- Thumb instruction set combines high code density with 32-bit performance.
- Serial wire debug (SWD) reduces the number of pins required for debugging.
- Micro trace buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory.
- Single cycle 32 bits by 32 bits multiply

4.6.1.2 Nested Vectored Interrupt Controller (NVIC)

- Up to 15 external interrupt sources
- Includes a single nonmaskable interrupt

4.6.1.3 Wake-Up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low-power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to Very-Deep-Sleep mode

- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a nonmasked interrupt is detected.
- Contains no programmer's model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

4.6.1.4 Debug Controller

- 2-pin serial wire debug (SWD) provides external debugger interface
- Micro trace buffer (MTB) provides simple execution trace capability and operates as a simple AHB-Lite SRAM controller.

4.6.2 System modules

4.6.2.1 Power Management Control Unit (PMC)

- Separate digital (regulated) and analog (referenced to digital) supply outputs
- Programmable power saving modes
- No output supply decoupling capacitors required
- Available wake-up from power saving modes via RTC and external inputs
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Buffered bandgap reference voltage output
- Factory programmed trim for bandgap and LVD
- 1 kHz Low-Power Oscillator (LPO)

4.6.2.2 COP Watchdog module

- Independent clock source input
- Choice between the following clock sources
  - LPO oscillator
  - Bus clock
  - IRC8M/2M
  - OSCERCLK

4.6.2.3 System clocks

- System Oscillator (OSC)—Loop-control pierce oscillator; crystal or ceramic resonator range of 32 kHz to 40 kHz (low range mode)
- Multipurpose Clock Generator- Lite (MCG-Lite)
  - Internal reference clocks—Can be used as a clock source for other on-chip peripherals
    - 48 MHz high accuracy internal reference clock
    - 8/2 MHz low power internal reference clock
    - 1 kHz LPO clock

4.6.2.4 Low-Leakage Wakeup Unit (LLWU)

- Support for up to 2 external input pins with individual enable bits
- Input sources may be external pins.
- External pin wake-up inputs, each of which is programmable as falling-edge, risingedge, or any change

- Wakeup inputs that are activated if enabled after MCU enters a low-leakage power mode
- Optional digital filters provided to qualify an external pin detect.

4.6.3 Memories and memory interfaces

4.6.3.1 On-chip memory

- 48 MHz performance devices
  - Up to 32 KB program flash memory
  - 2 KB SRAM
  - Up to 8 KB ROM
  - 16 bytes regfile
- Security circuitry to prevent unauthorized access to RAM and flash memory contents

4.6.4 Analog

4.6.4.1 Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with up to 12-bit resolution
- Output modes:
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise operation
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for various programmable values
- Temperature sensor
- Hardware average function
- Selectable voltage reference
- Self-calibration mode

4.6.4.2 High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to five selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising-edge, falling-edge, or either rising or falling edges of the comparator output
- Comparator output supports:
  - Sampled
  - Windowed (ideal for certain PWM zero-crossing-detection applications
  - Digitally filtered using external sample signal or scaled peripheral clock
- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes except for VLLS0

4.6.4.3 Voltage reference (VREF)

- Programmable trim register with 0.5 mV steps, automatically loaded with factory trimmed value upon reset
- Programmable buffer mode selection:
  - Off
  - Bandgap enabled/standby (output buffer disabled)
  - Low power buffer mode (output buffer enabled)
  - High power buffer mode (output buffer enabled)
- 1.2 V output at room temperature
- Output pin VREF_OUT, shared with normal GPIO

4.6.5 Timers

4.6.5.1 Timer/PWM (TPM)

- Selectable source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Generation of hardware triggers

4.6.6 Communication interfaces

4.6.6.1 Inter-Integrated Circuit (I^2C)

- Compatible with I^2C bus standard
- Up to 400 kbit/s with maximum bus loading
- Up to 1 Mbit/s operation with maximum bus loading
- Multimaster operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when the processor is in low-power mode.

4.6.6.2 LPUART

- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock:
  - Baud rate can be configured independently of the bus clock frequency
  - Supports operation in Stop modes
- Interrupt or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
  - Receive data match
- Hardware parity generation and checking

- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

4.6.6.3 Serial Peripheral Interface (SPI)

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting

4.6.7 Human-machine interface

4.6.7.1 General-Purpose Input/Output (GPIO)

- Hysteresis and configurable pullup/pulldown device on all input pins
- Configurable drive strength on some output pins
- Independent pin value register to read logic level on digital pin

5 Part numbers and packaging

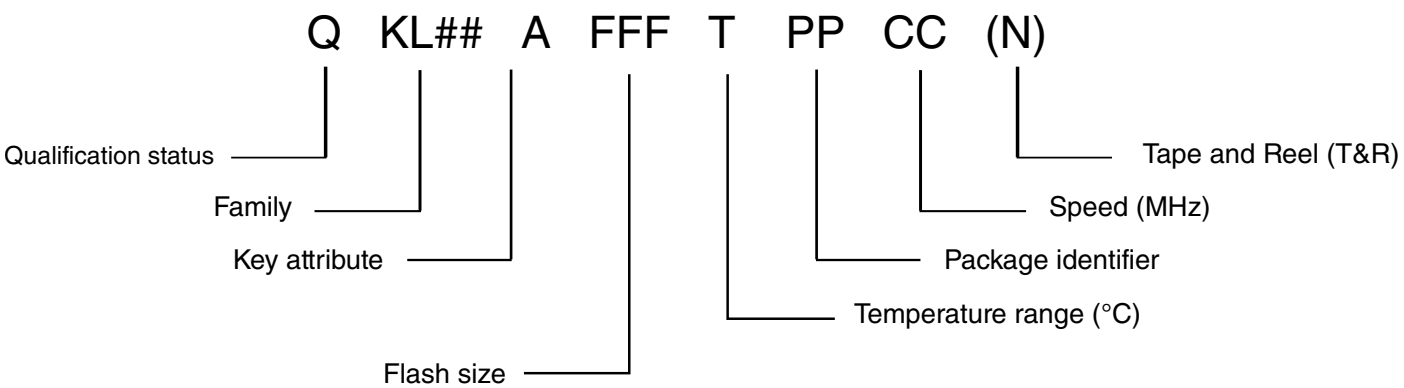


Figure 2. Part numbers diagrams

Table 6. Part number fields descriptions

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KL##	Kinetis family	• KL03
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 8 = 8 KB • 16 = 16 KB • 32 = 32 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• FG = 16 QFN (3 mm x 3 mm) • AF = 20 WLCSP (1.99 mm x 1.61 mm) • FK = 24 QFN (4 mm x 4 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel

6 Revision history

The following table provides a revision history for this document.

Table 7. Revision history

Rev. No.	Date	Substantial changes
2	2/2014	Initial public release. • Updated WLCSP package size. • Updated power modes section • Added LLWU feature lists
3	07/2014	Updated low power features in the Key feature section.

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