



SOT804-3(D)

HVQFN64, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 64 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.85 mm body

7 September 2018

Package information

1 Package summary

Terminal position code	Q (quad)
Package type descriptive code	HVQFN64
Package style descriptive code	HVQFN (thermal enhanced very thin quad flatpack; no leads)
Mounting method type	S (surface mount)
Issue date	20-07-2018
Manufacturer package code	98ASA01298D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	9	-	mm
package width	-	9	-	mm
package height	-	0.85	-	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	64	-	



HVQFN64, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 64 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.85 mm body

2 Package outline

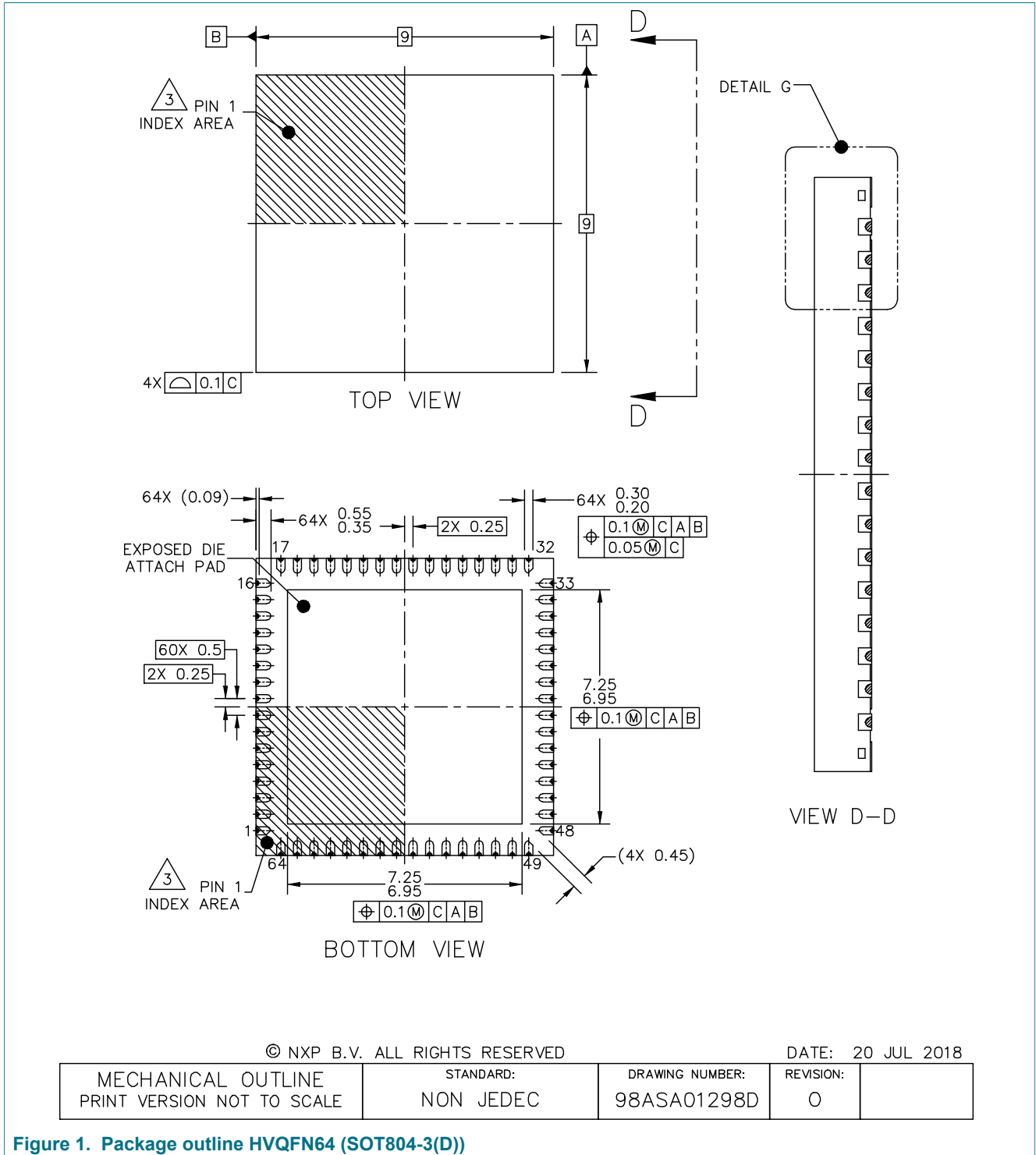


Figure 1. Package outline HVQFN64 (SOT804-3(D))

HVQFN64, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 64 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.85 mm body

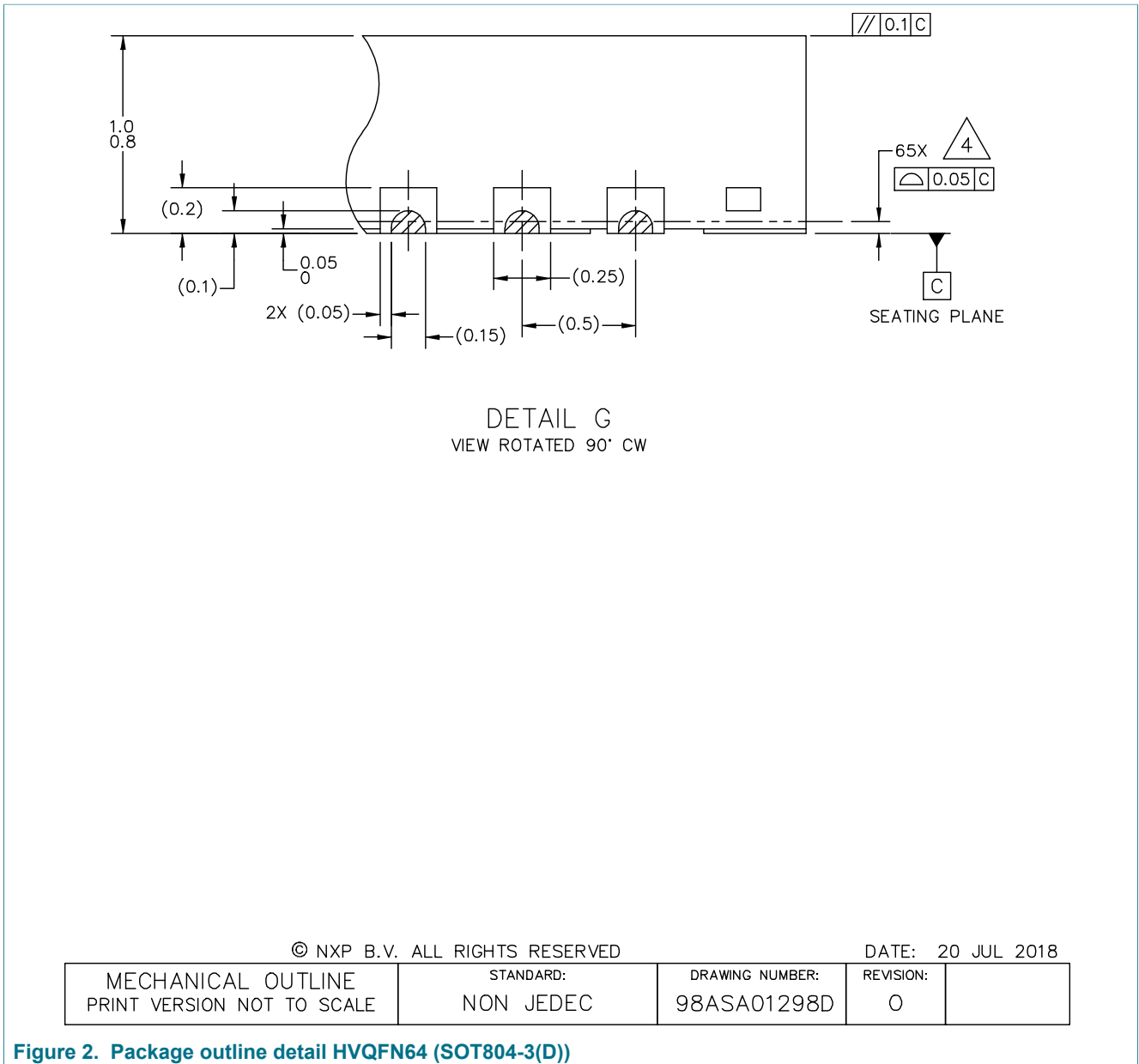


Figure 2. Package outline detail HVQFN64 (SOT804-3(D))

HVQFN64, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 64 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.85 mm body

3 Soldering

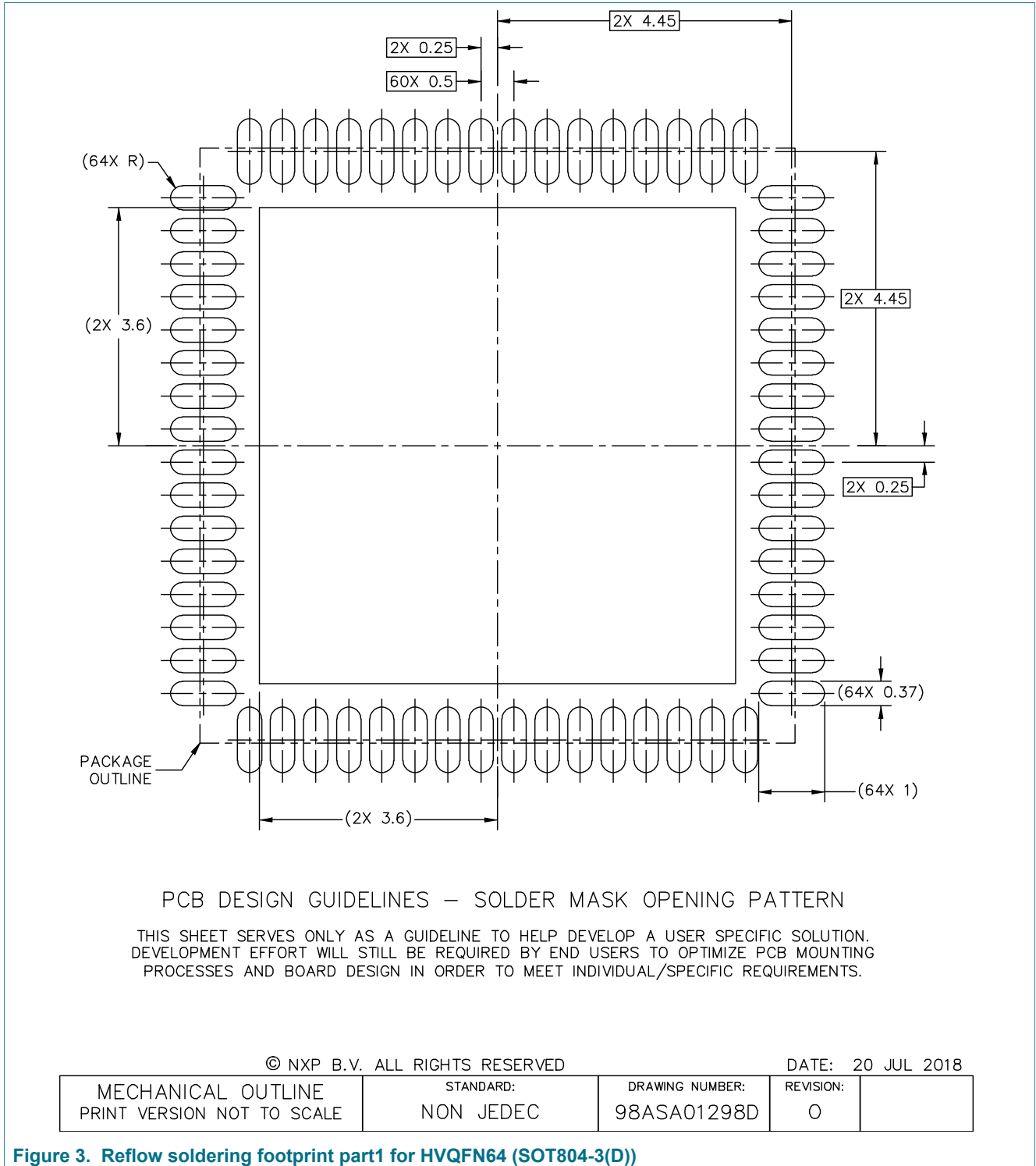
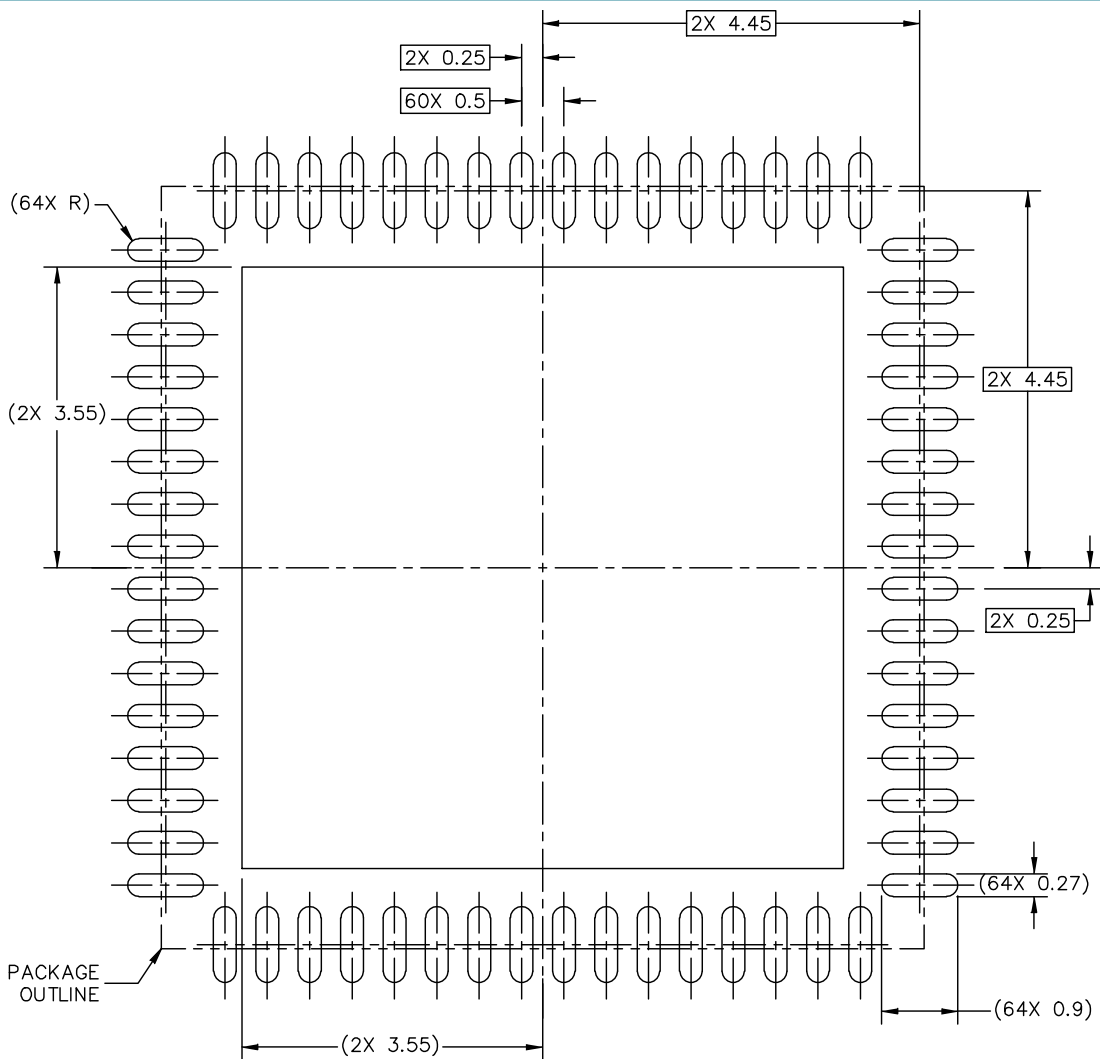


Figure 3. Reflow soldering footprint part1 for HVQFN64 (SOT804-3(D))

HVQFN64, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 64 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.85 mm body



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

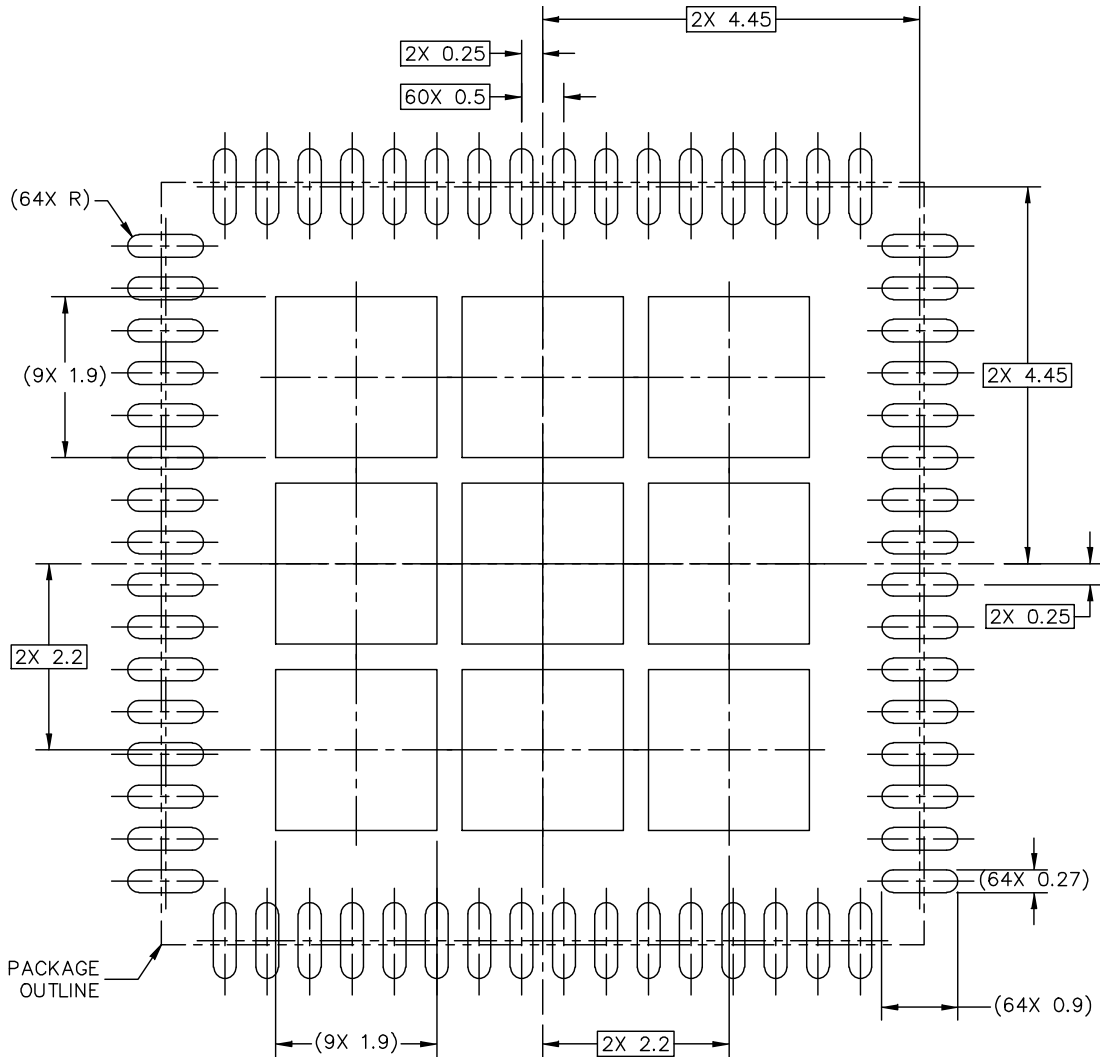
© NXP B.V. ALL RIGHTS RESERVED

DATE: 20 JUL 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01298D	REVISION: 0	
--	------------------------	--------------------------------	----------------	--

Figure 4. Reflow soldering footprint part2 for HVQFN64 (SOT804-3(D))

HVQFN64, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 64 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.85 mm body



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 20 JUL 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01298D	REVISION: 0	
--	------------------------	--------------------------------	----------------	--

Figure 5. Reflow soldering footprint part3 for HVQFN64 (SOT804-3(D))

HVQFN64, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 64 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.85 mm body

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.25 MM.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 20 JUL 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01298D	REVISION: 0	
--	------------------------	--------------------------------	----------------	--

Figure 6. Package outline note HVQFN64 (SOT804-3(D))

HVQFN64, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 64 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.85 mm body

4 Legal information

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

HVQFN64, thermal enhanced very thin quad flat package, no leads, dimple wettable flank; 64 terminals,
0.5 mm pitch, 9 mm x 9 mm x 0.85 mm body

Contents

1 Package summary1
2 Package outline2
3 Soldering4
4 Legal information8