

HVQFN40, plastic thermal enhanced very thin quad flatpack; no leads, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body

15 January 2018

Package information

1. Package summary

Terminal position code Q (quad)

Package type descriptive code HVQFN40

Package type industry code HVQFN40

Package style descriptive code HVQFN (thermal enhanced very thin quad

flatpack; no leads)

Package body material type P (plastic)

Mounting method type S (surface mount)

Issue date11-10-2017Manufacturer package code98ASA01113D

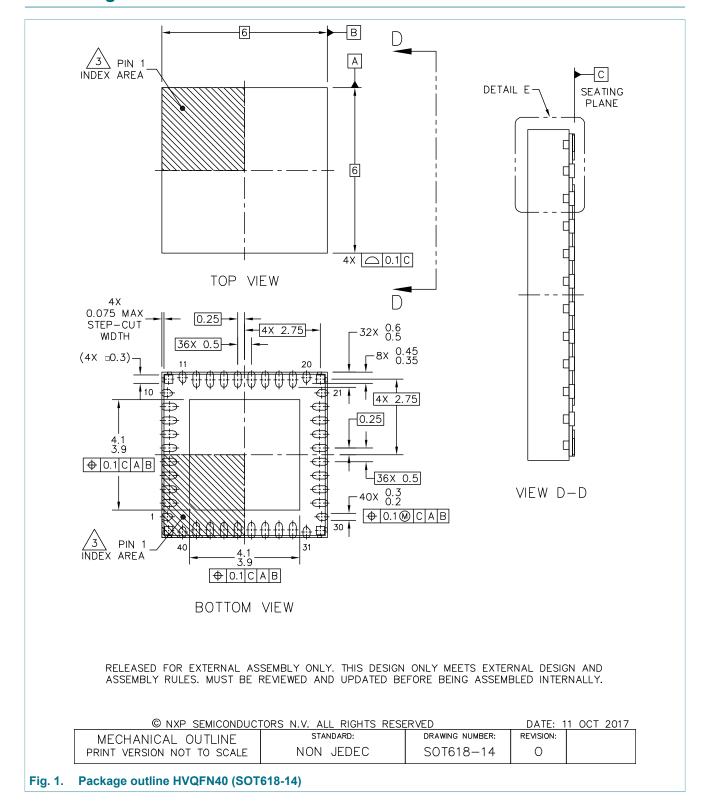
Table 1. Package summary

Symbol	Parameter	Min	Тур	Nom	Max	Unit
D	package length	-	-	6	-	mm
E	package width	-	_	6	_	mm
Α	seated height	-	-	0.85	-	mm
е	nominal pitch	-	-	0.5	-	mm
n ₂	actual quantity of termination	-	-	40	-	A/A



HVQFN40, plastic thermal enhanced very thin quad flatpack; no leads, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body

2. Package outline



HVQFN40, plastic thermal enhanced very thin quad flatpack; no leads, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body

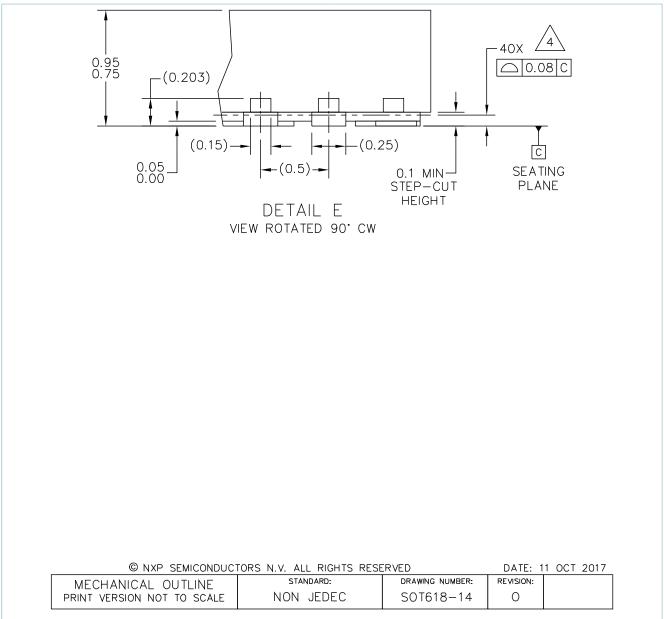


Fig. 2. Package outline dt1 HVQFN40 (SOT618-14)

HVQFN40, plastic thermal enhanced very thin quad flatpack; no leads, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3.

PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4.

COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

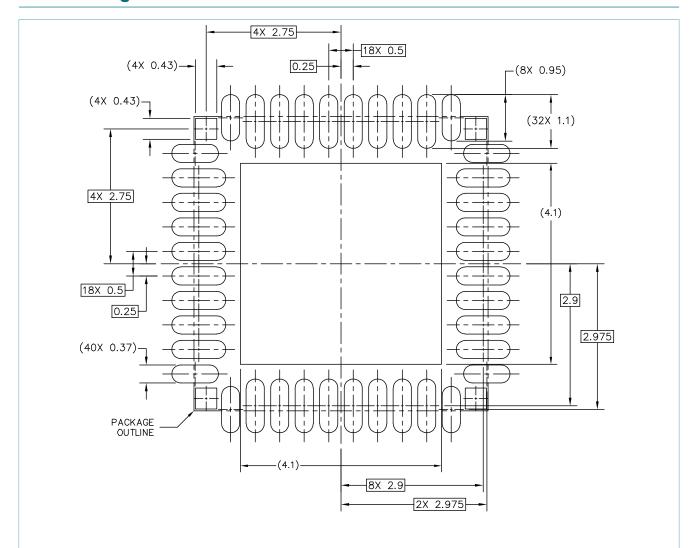
DATE: 11 OCT 2017

MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
PRINT VERSION NOT TO SCALE	NON JEDEC	SOT618-14	0	

Fig. 3. Package outline note HVQFN40 (SOT618-14)

HVQFN40, plastic thermal enhanced very thin quad flatpack; no leads, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body

3. Soldering



PCB DESIGN GUIDELINES - SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

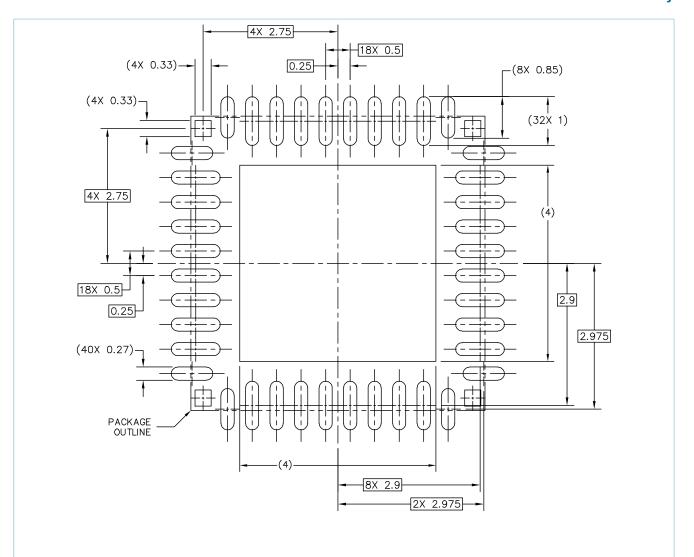
© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED			DATE: 1	1 OCT 2017	
	MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
	PRINT VERSION NOT TO SCALE	NON JEDEC	SOT618-14	0	

Reflow soldering footprint for HVQFN40 (SOT618-14) Fig. 4.

SOT618-14

© NXP B.V. 2018. All rights reserved

HVQFN40, plastic thermal enhanced very thin quad flatpack; no leads, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body



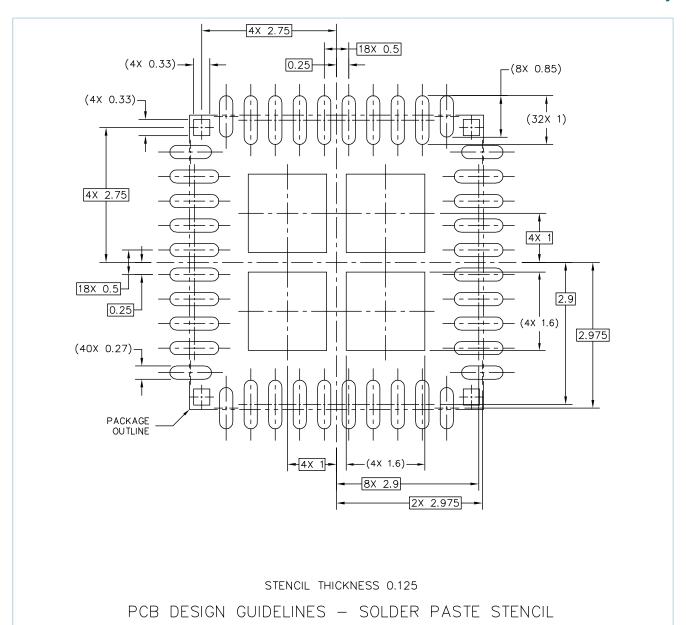
PCB DESIGN GUIDELINES - I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED			DATE: 1	1 OCT 2017
MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
PRINT VERSION NOT TO SCALE	NON JEDEC	SOT618-14	0	

Fig. 5. Reflow soldering footprint part2 for HVQFN40 (SOT618-14)

HVQFN40, plastic thermal enhanced very thin quad flatpack; no leads, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body



THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED			DATE: 1	1 OCT 2017
MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
PRINT VERSION NOT TO SCALE	NON JEDEC	SOT618-14	0	

Fig. 6. Reflow soldering footprint part3 for HVQFN40 (SOT618-14)

HVQFN40, plastic thermal enhanced very thin quad flatpack; no leads, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body

4. Legal information

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

HVQFN40, plastic thermal enhanced very thin quad flatpack; no leads, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.85 mm body

5. Contents

1.	Package summary	1
2.	Package outline	2
3.	Soldering	5
4.	Legal information	8

© NXP B.V. 2018. All rights reserved

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com Date of release: 15 January 2018