

SOT2172-1

VFBGA184, very thin fine-pitch ball grid array package, 184 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.86 mm body

14 April 2022

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	VFBGA184
Package style descriptive code	VFBGA (very thin fine-pitch ball grid array)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	21-12-2021
Manufacturer package code	98ASA01888D

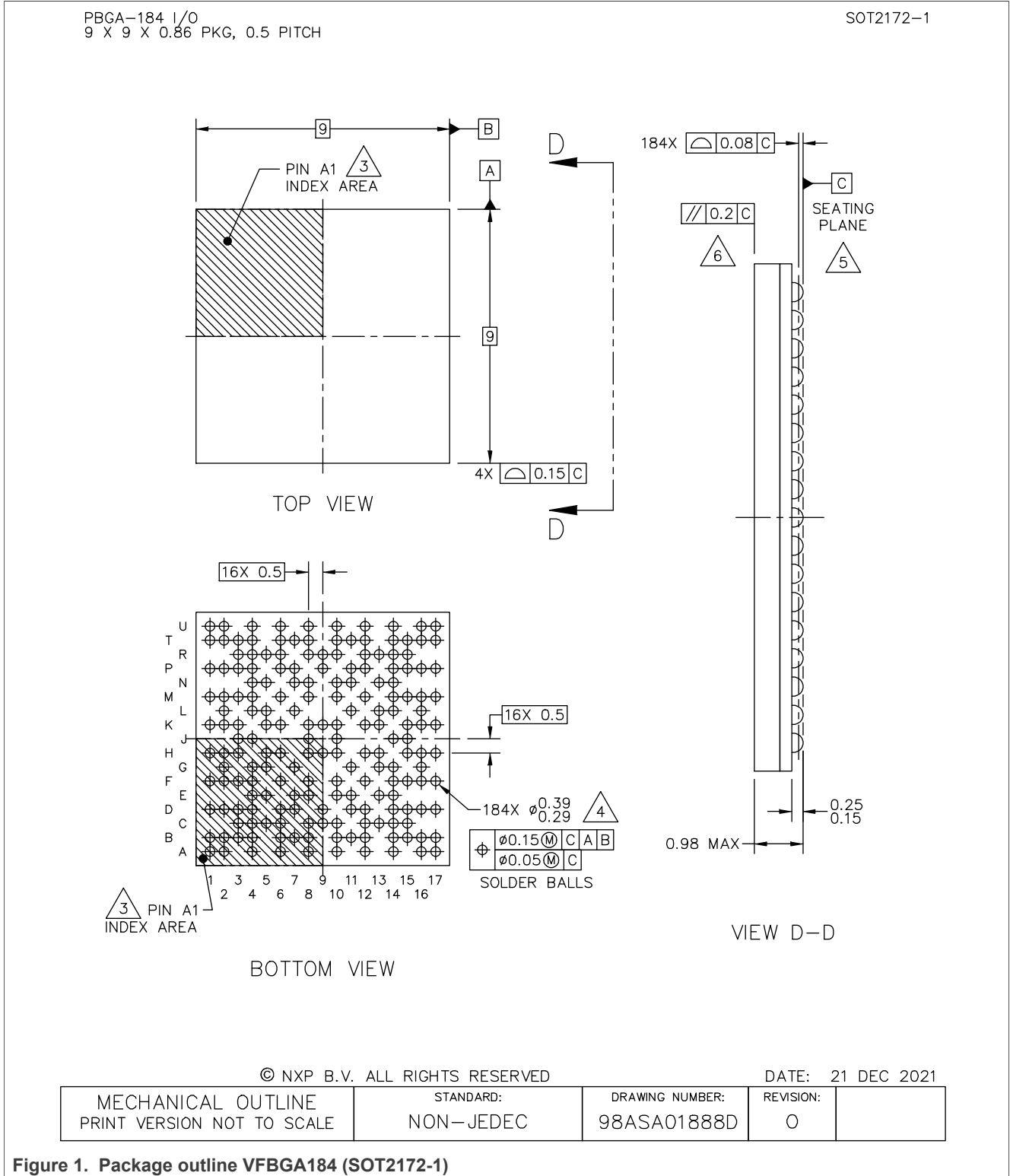
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	9	-	mm
package width	-	9	-	mm
seated height	-	0.86	0.98	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	184	-	

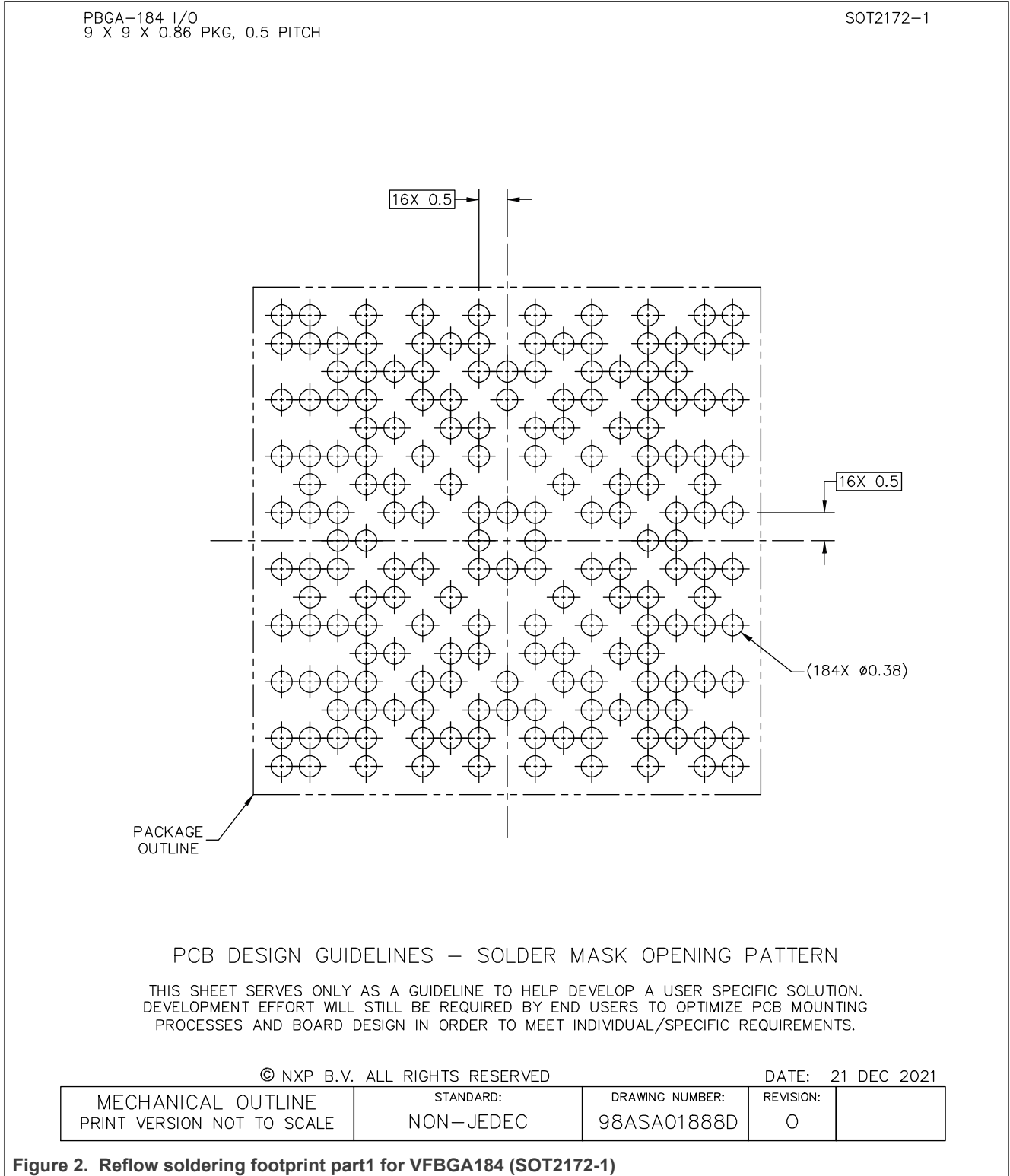


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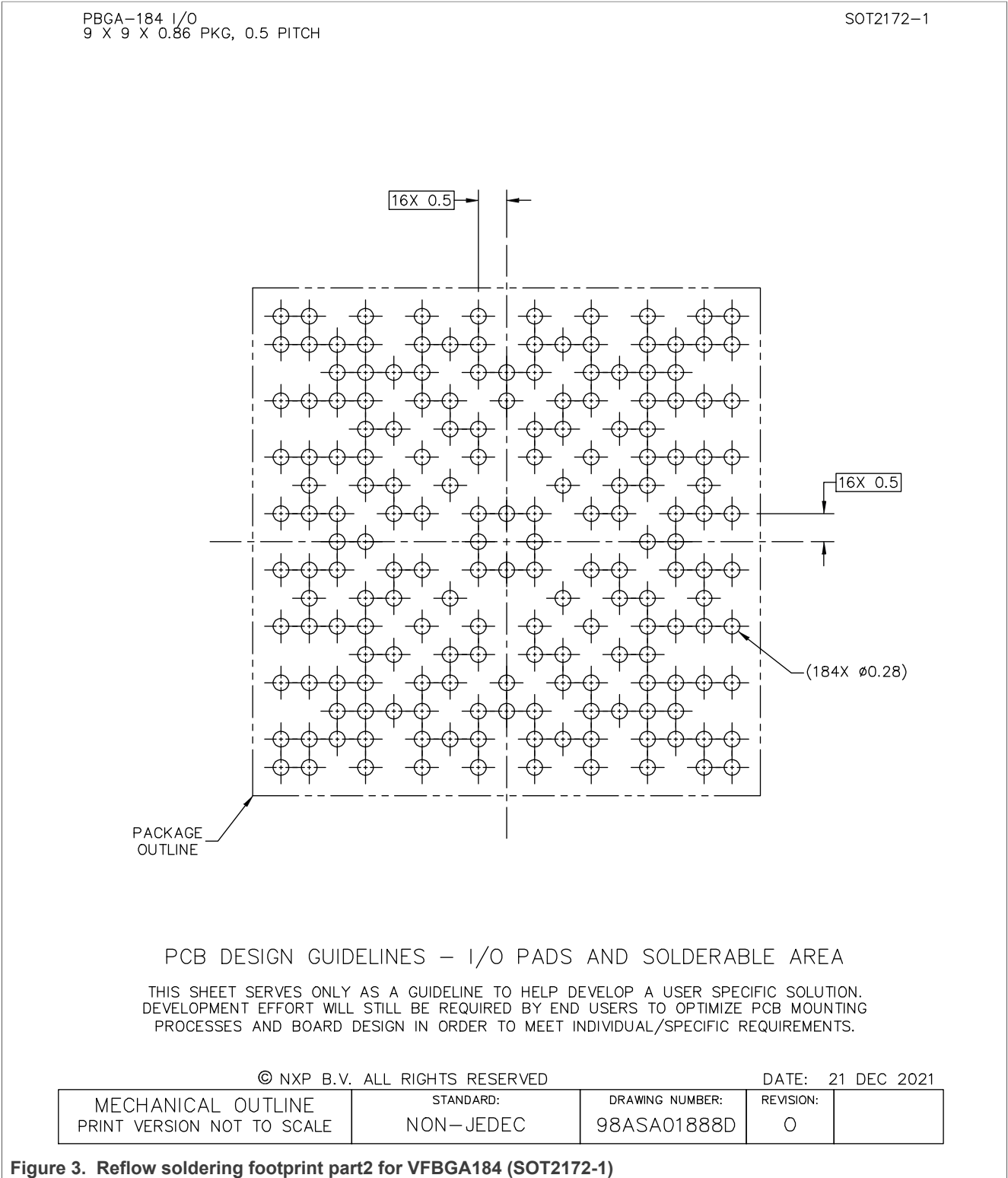
2 Package outline



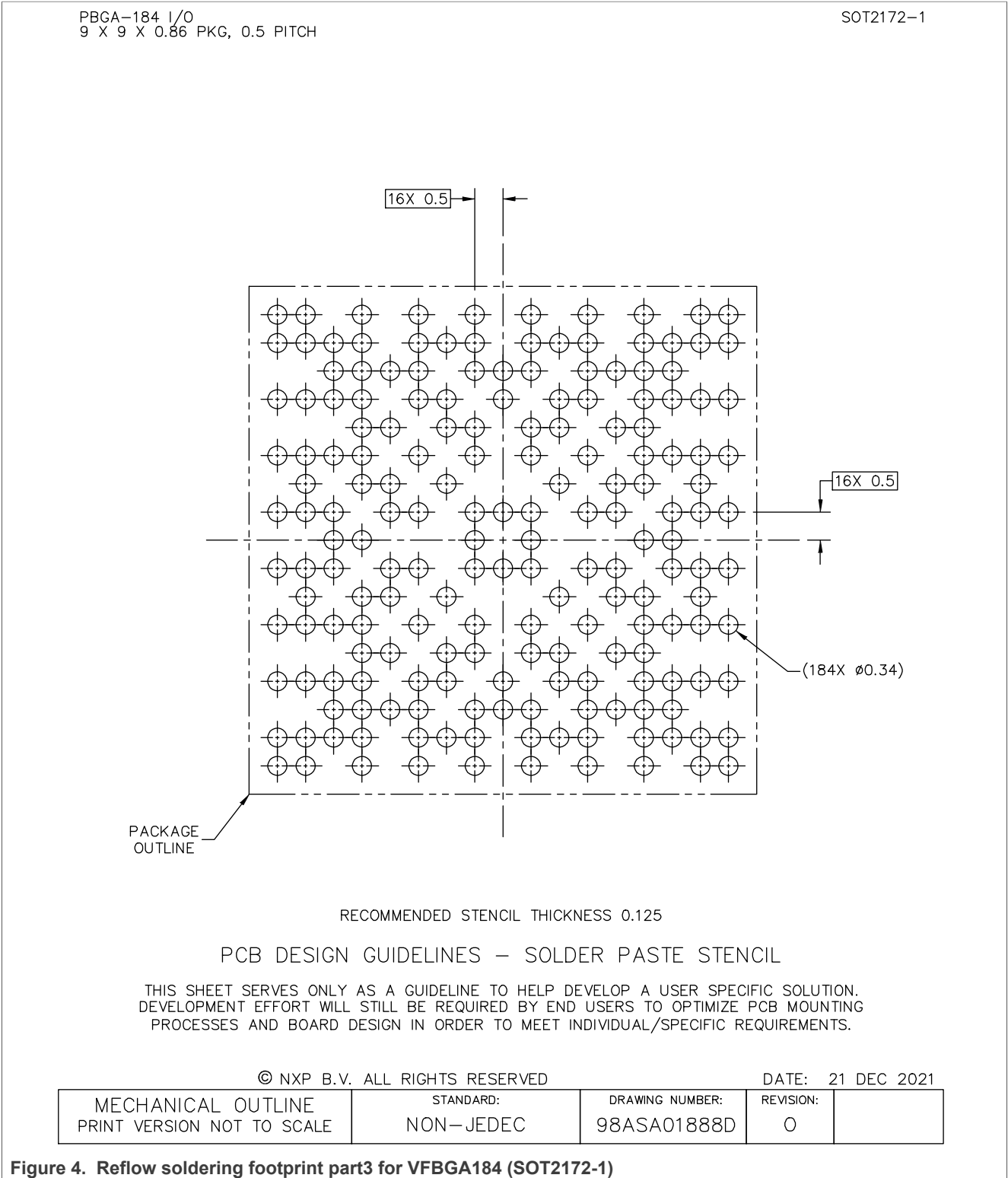
3 Soldering



VFBGA184, very thin fine-pitch ball grid array package, 184 terminals, 0.5 mm pitch, 9 mm x 9 mm x 0.86 mm body



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PBGA-184 I/O
9 X 9 X 0.86 PKG, 0.5 PITCH

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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DATE: 21 DEC 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01888D	REVISION: 0	
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Figure 5. Package outline note VFBGA184 (SOT2172-1)

4 Legal information

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