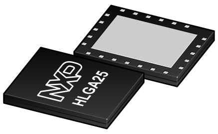


SOT2171-1

HLGA25, thermal enhanced land grid array package, 25 terminals, 2.5 mm pitch, 20 mm x 16 mm x 1.947 mm body

29 April 2022 Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	HLGA25
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	29-11-2021
Manufacturer package code	98ASA01875D

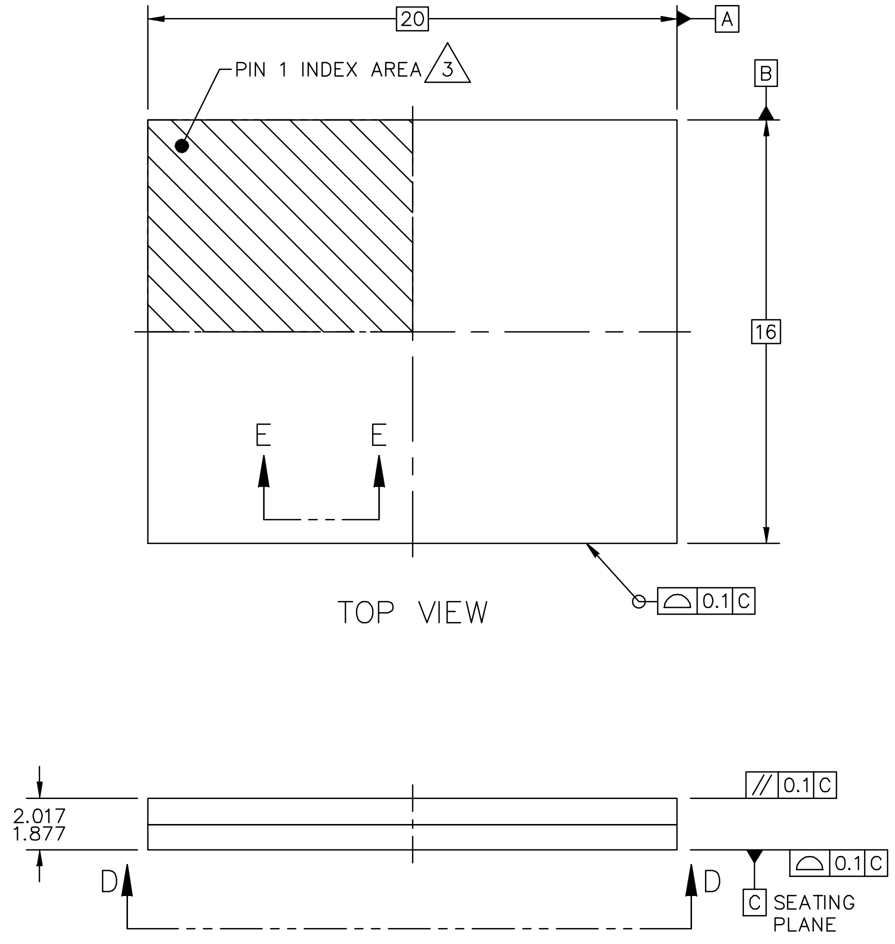
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	20	-	
package width	-	16	-	
seated height	1.877	1.947	2.017	
nominal pitch	-	2.5	-	
actual quantity of termination	-	25	-	

2 Package outline

H−PLGA−25 I/O
20 X 16 X 1.947 PKG, 2.5 PITCH

SOT2171−1



© NXP B.V. ALL RIGHTS RESERVED

DATE: 29 NOV 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON−JEDEC	DRAWING NUMBER: 98ASA01875D	REVISION: 0	

Figure 1. Package outline HLGA25 (SOT2171-1)

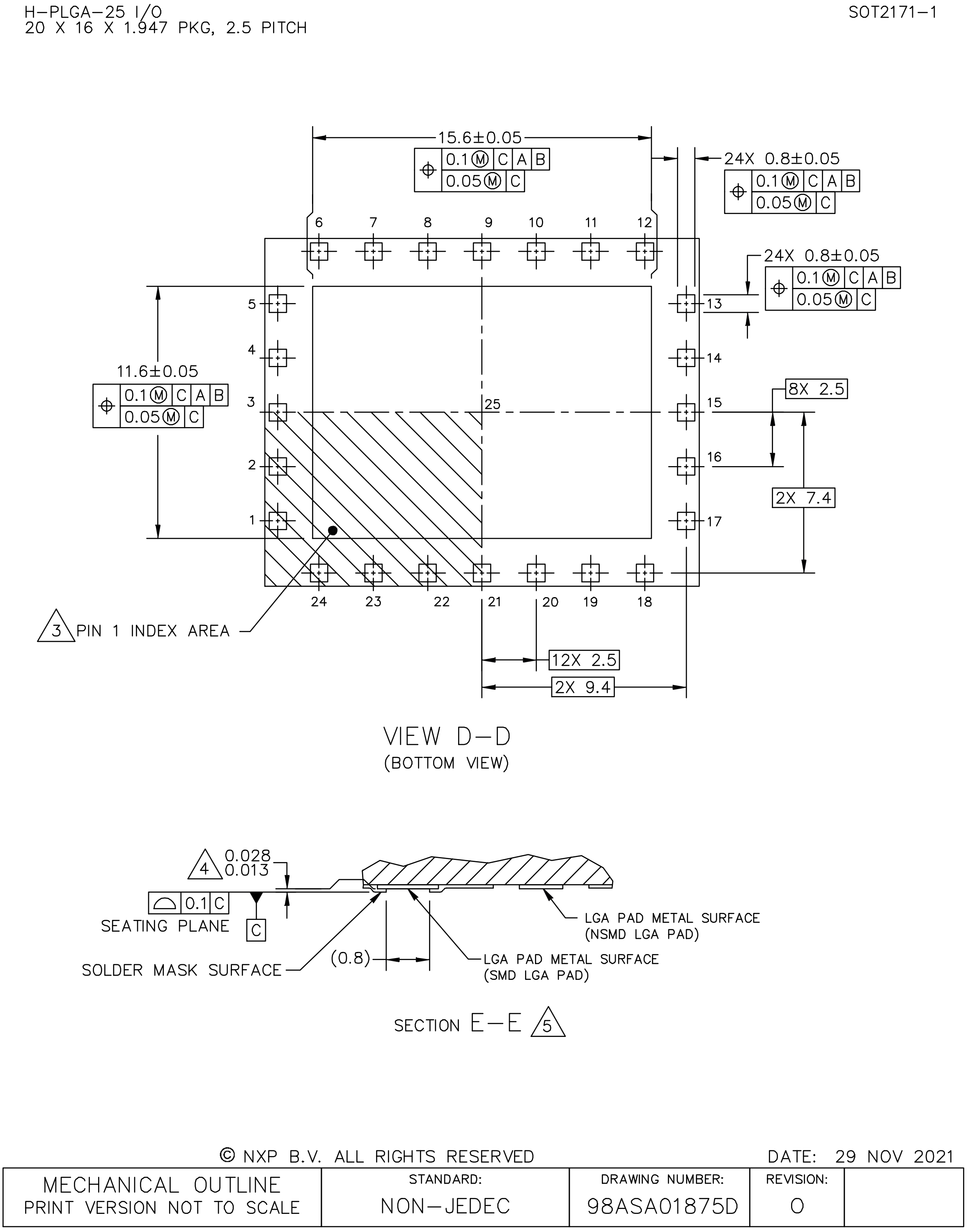
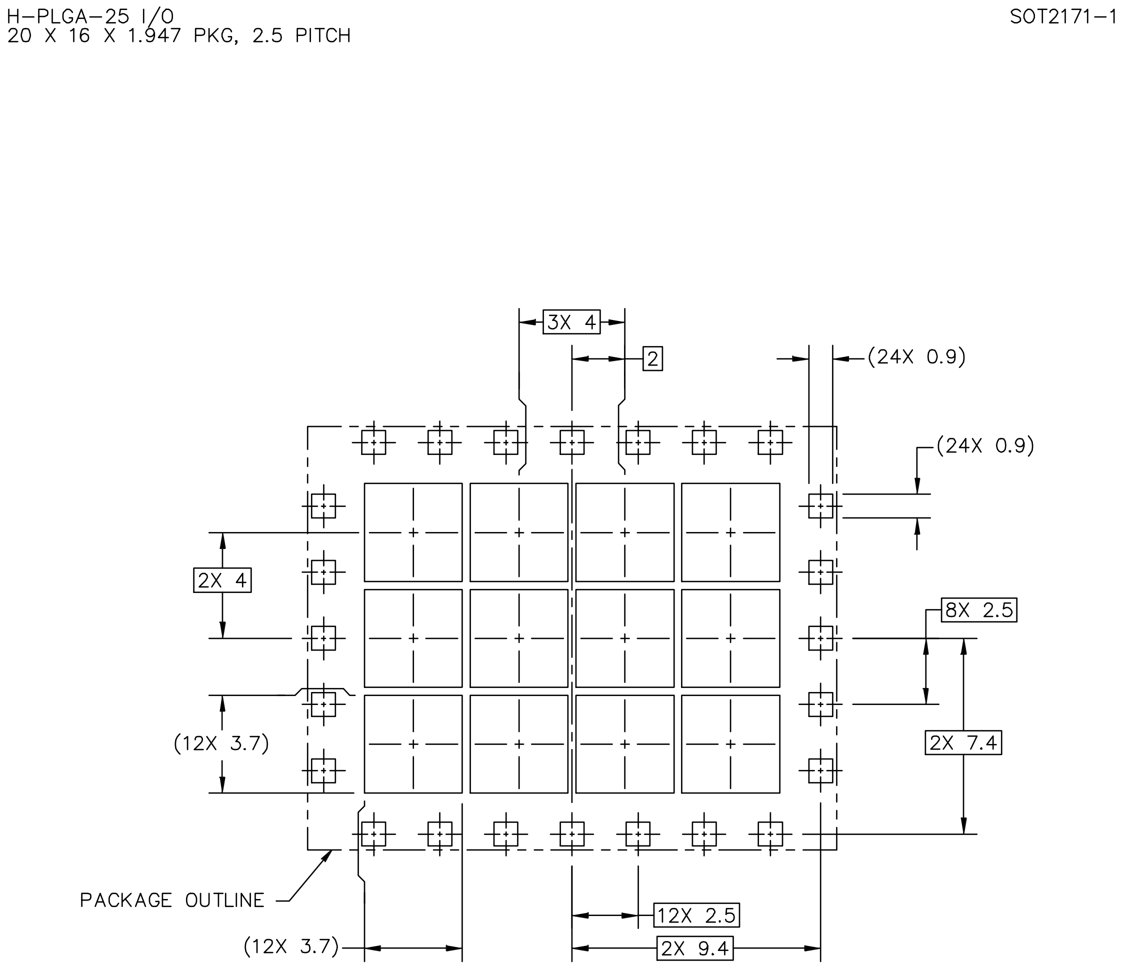


Figure 2. Package outline detail D-D and E-E of HLGA25 (SOT2171-1)

3 Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

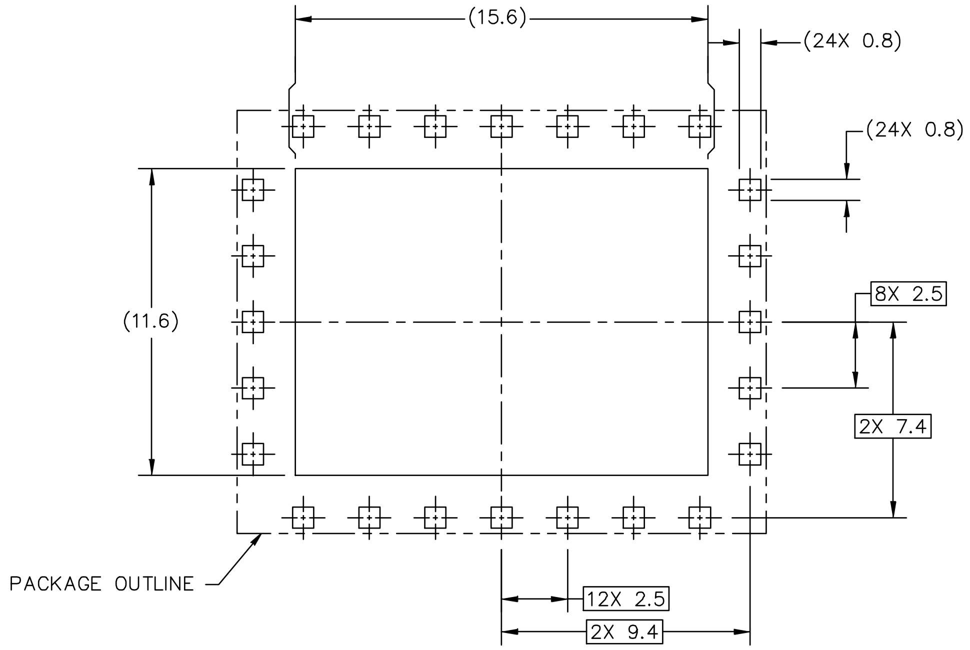
DATE: 29 NOV 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01875D	REVISION: O	

Figure 3. Reflow soldering footprint part1 for HLGA25 (SOT2171-1)

H-PLGA-25 I/O
20 X 16 X 1.947 PKG, 2.5 PITCH

SOT2171-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREAS

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

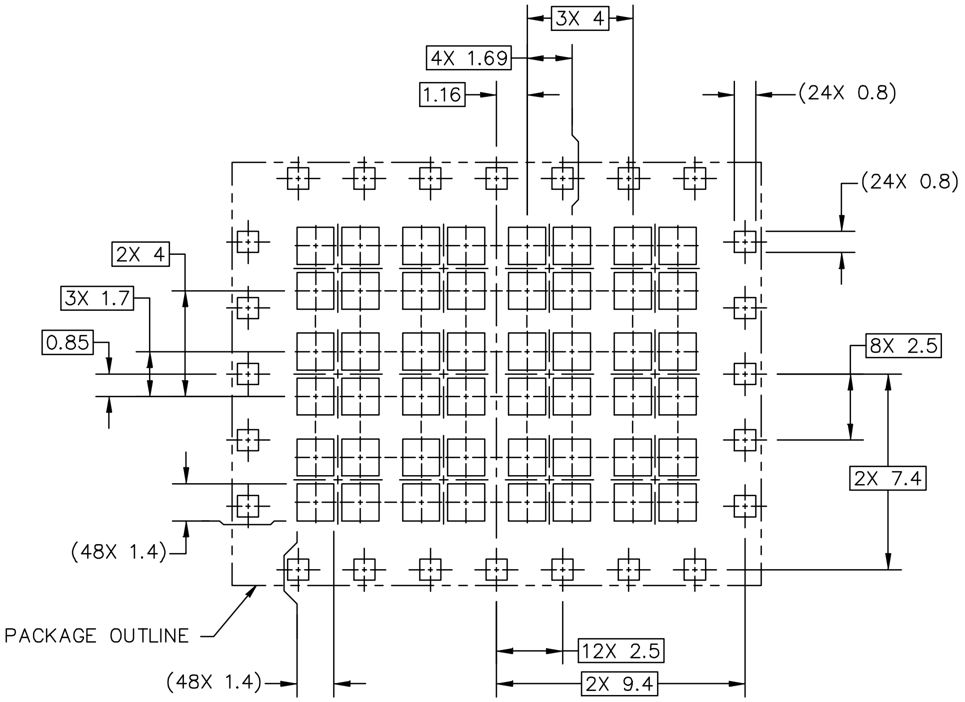
DATE: 29 NOV 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01875D	REVISION: O	

Figure 4. Reflow soldering footprint part2 for HLGA25 (SOT2171-1)

H–PLGA–25 I/O
20 X 16 X 1.947 PKG, 2.5 PITCH

SOT2171–1



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 29 NOV 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD:	DRAWING NUMBER:	REVISION:	
	NON–JEDEC	98ASA01875D	O	

Figure 5. Reflow soldering footprint part3 for HLGA25 (SOT2171-1)

H–PLGA–25 I/O
20 X 16 X 1.947 PKG, 2.5 PITCH

SOT2171–1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PINS 25) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).

DATE: 29 NOV 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01875D	REVISION: 0	

Figure 6. Package outline note HLGA25 (SOT2171-1)

4 Legal information

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

SOT2171-1

HLGA25, thermal enhanced land grid array package, 25 terminals, 2.5 mm pitch, 20 mm x 16 mm x 1.947 mm body

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 29 April 2022