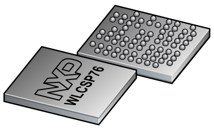


SOT2073-1

WLCSP76, wafer level chip scale package, 76 terminals, 3.95 mm x 3.565 mm x 0.495 mm body (backside coating included)

26 April 2021 Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP76
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	10-06-2020
Manufacturer package code	98ASA01673D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	3.535	3.565	3.595	mm
package width	3.92	3.95	3.98	mm
package height	-	0.495	0.53	mm
actual quantity of termination	-	76	-	

2 Package outline

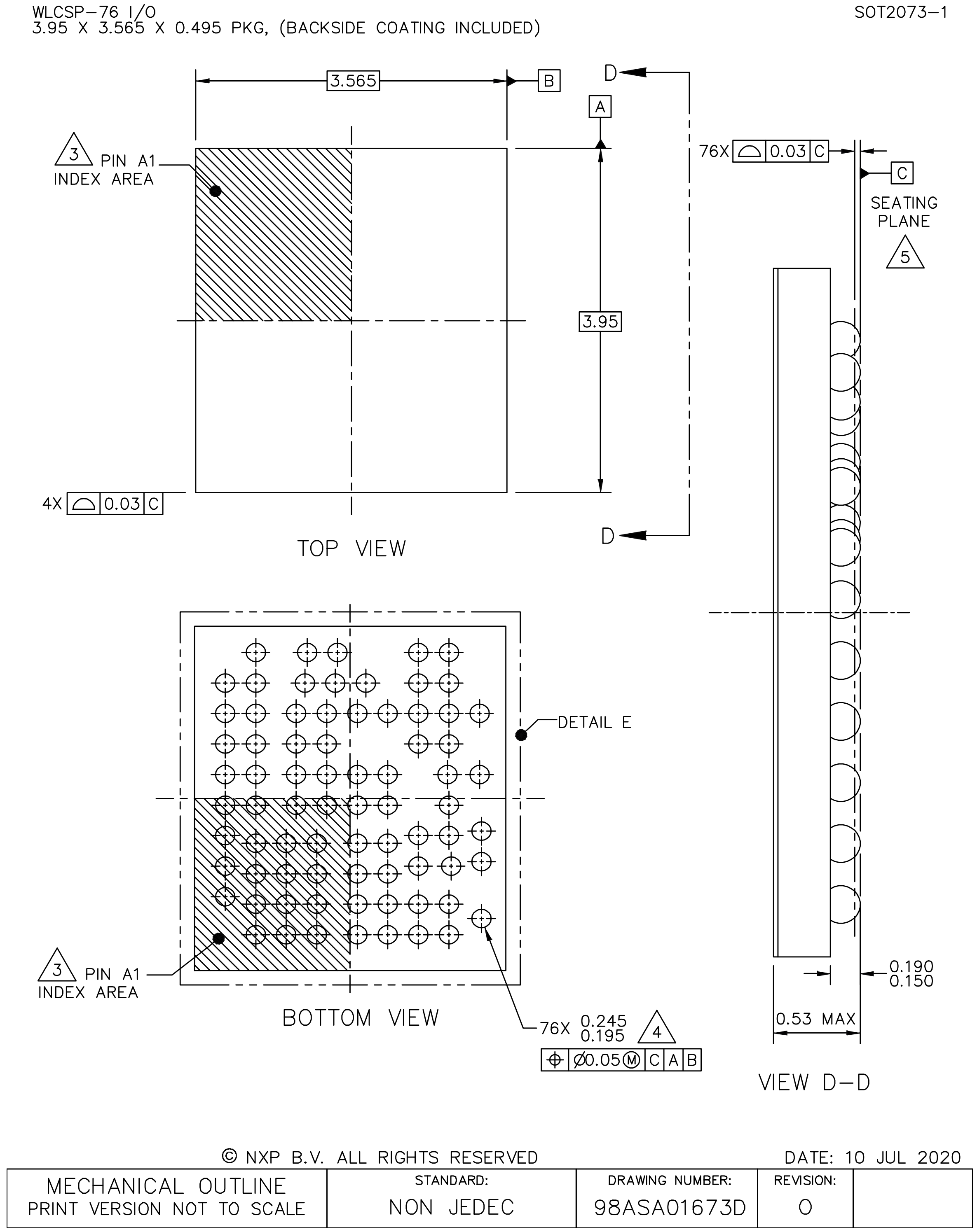
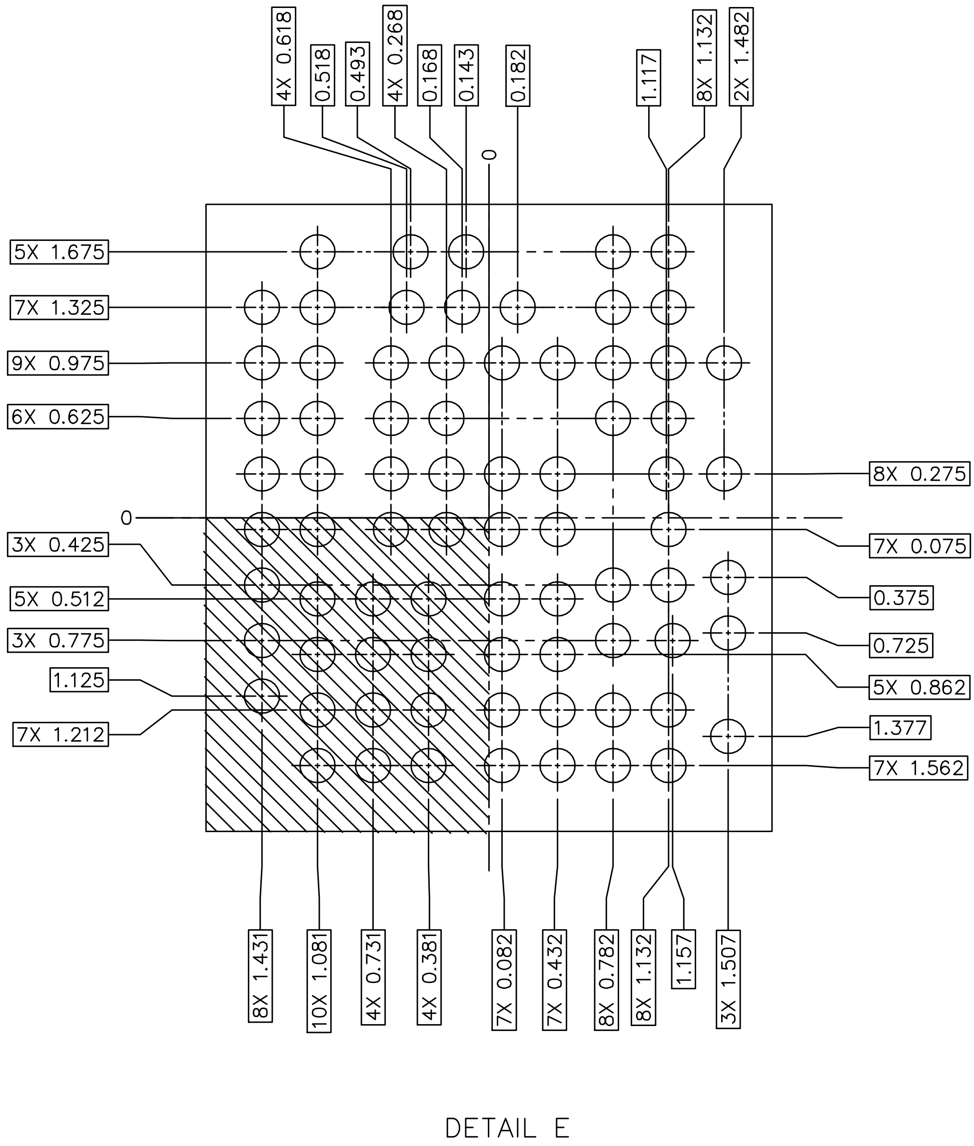


Figure 1. Package outline WLCSP76 (SOT2073-1)

WLCSP−76 I/O
3.95 X 3.565 X 0.495 PKG, (BACKSIDE COATING INCLUDED)

SOT2073−1



DATE: 10 JUL 2020

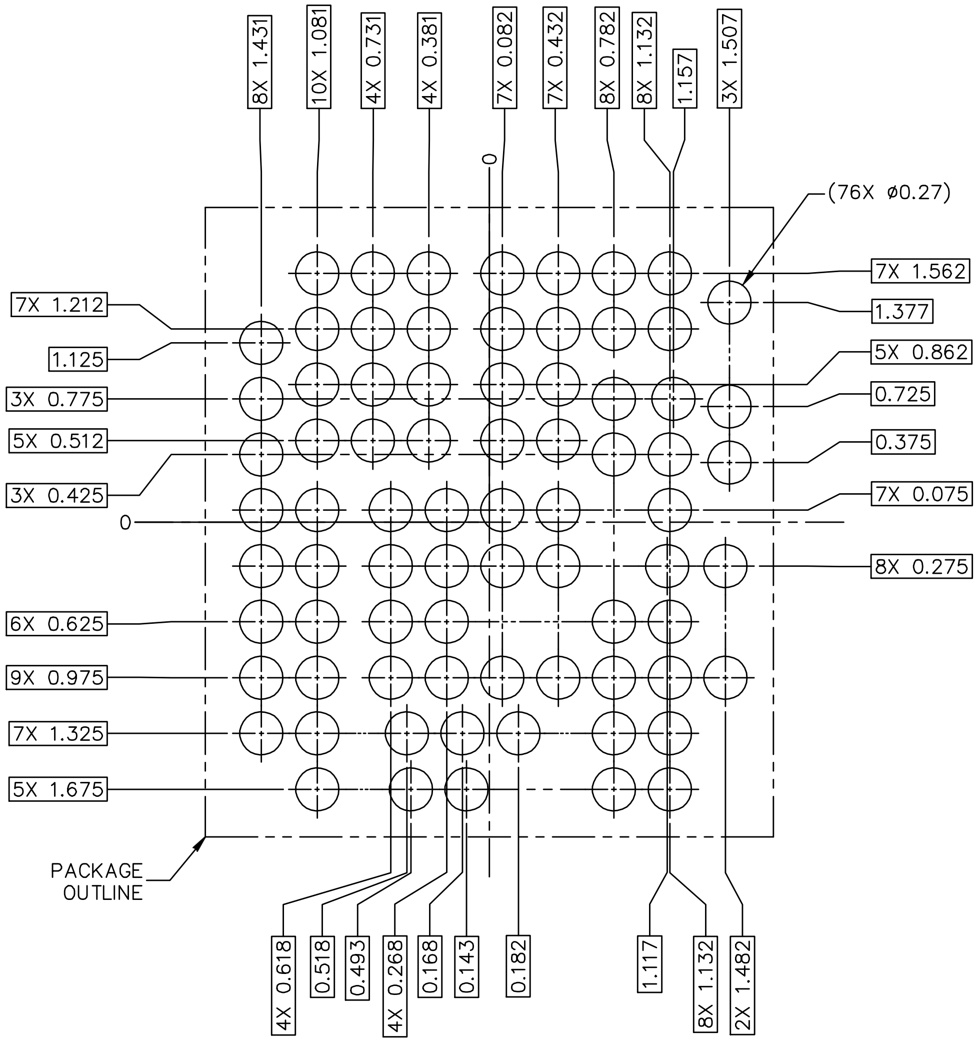
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01673D	REVISION: 0	

Figure 2. Package outline detail of WLCSP76 (SOT2073-1)

WLCSP76, wafer level chip scale package, 76 terminals, 3.95 mm x 3.565 mm x 0.495 mm body (backside coating included)

3 Soldering

WLCSP–76 I/O SOT2073–1
3.95 X 3.565 X 0.495 PKG, (BACKSIDE COATING INCLUDED)



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

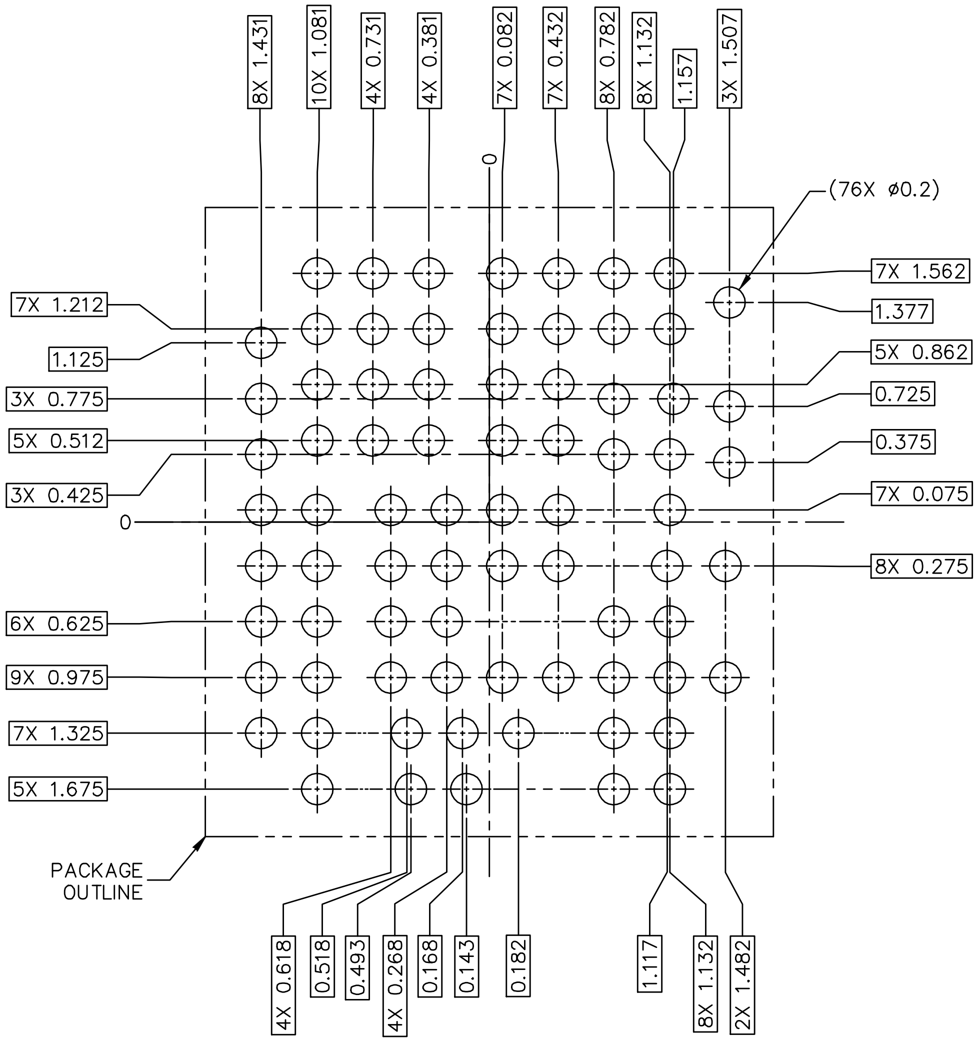
DATE: 10 JUL 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01673D	REVISION: O	

Figure 3. Reflow soldering footprint part1 for WLCSP76 (SOT2073-1)

WLCSP-76 I/O
3.95 X 3.565 X 0.495 PKG, (BACKSIDE COATING INCLUDED)

SOT2073-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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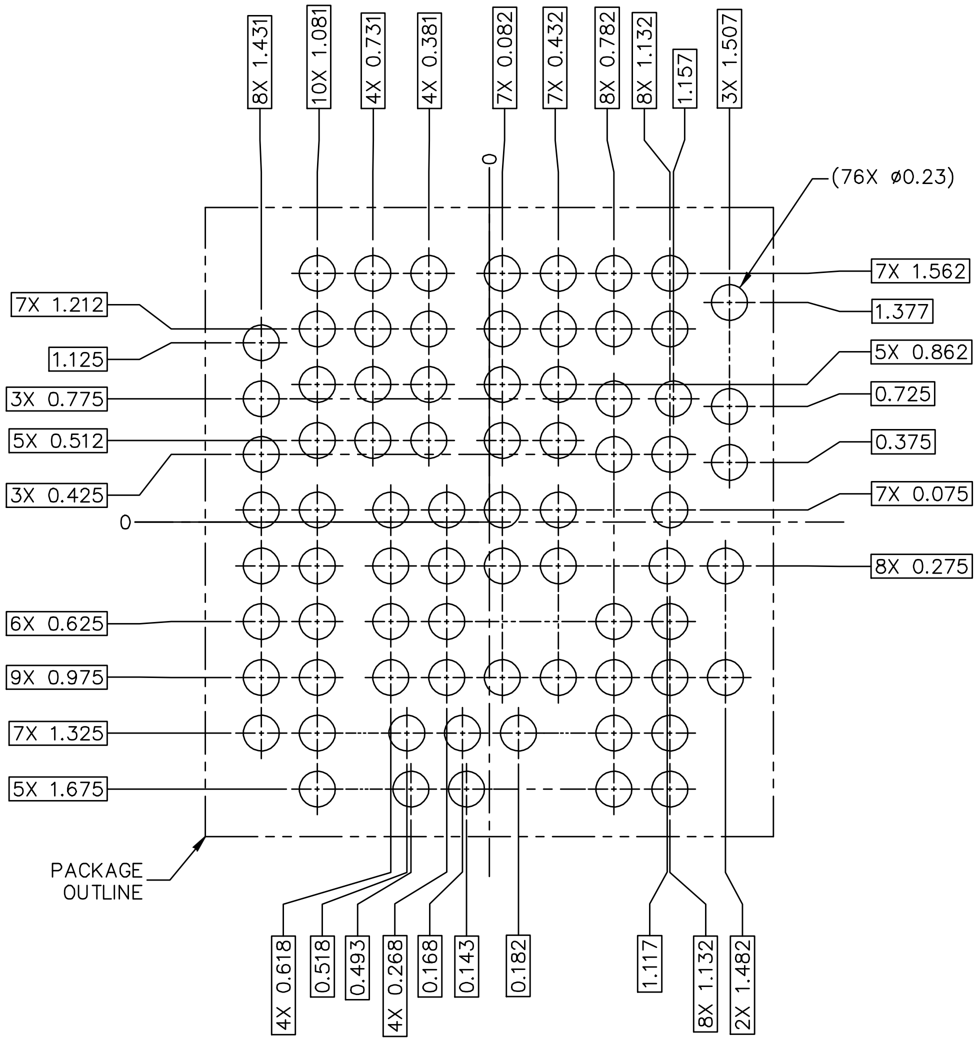
DATE: 10 JUL 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01673D	REVISION: O	

Figure 4. Reflow soldering footprint part2 for WLCSP76 (SOT2073-1)

WLCSP-76 I/O
3.95 X 3.565 X 0.495 PKG, (BACKSIDE COATING INCLUDED)

SOT2073-1



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 10 JUL 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01673D	REVISION: 0	

Figure 5. Reflow soldering footprint part3 for WLCSP76 (SOT2073-1)

WLCSP76, wafer level chip scale package, 76 terminals, 3.95 mm x 3.565 mm x 0.495 mm body (backside coating included)

WLCSP-76 I/O
3.95 X 3.565 X 0.495 PKG, (BACKSIDE COATING INCLUDED)

SOT2073-1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. △ PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. △ MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. △ DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

DATE: 10 JUL 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01673D	REVISION: O	

Figure 6. Package outline note WLCSP76 (SOT2073-1)

4 Legal information

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SOT2073-1

WLCSP76, wafer level chip scale package, 76 terminals, 3.95 mm x 3.565 mm x 0.495 mm body (backside coating included)

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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