

SOT1390-7

WLCSP12, wafer level chip-scale package; 12 bumps; 1.67 mm x 1.27 mm x 0.525 mm (backside coating included)

23 November 2021

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP12
Package type industry code	WLCSP12
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	24-04-2017
Manufacturer package code	SOT1390

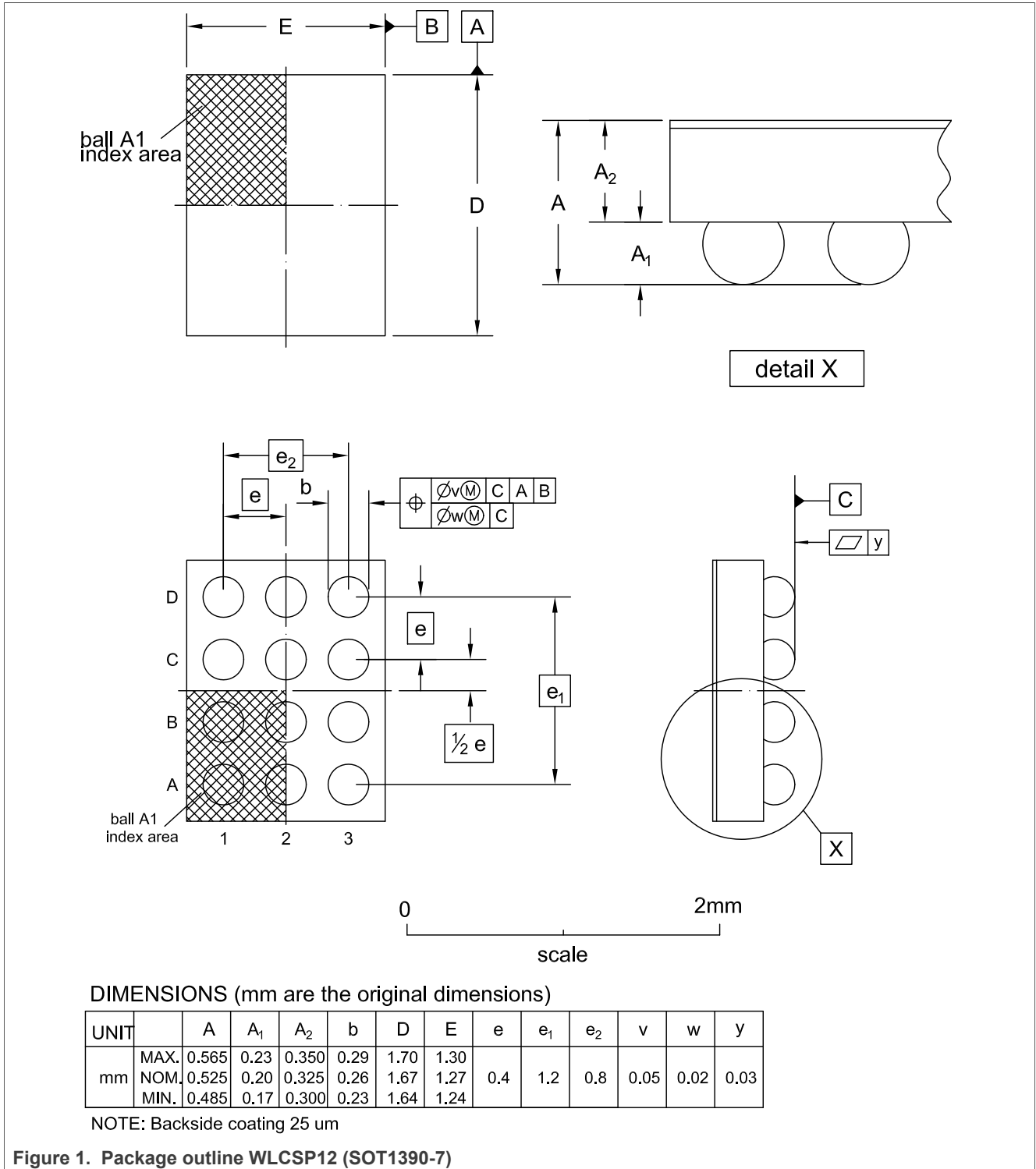
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	1.64	1.67	1.7	mm
package width	1.24	1.27	1.3	mm
seated height	0.485	0.525	0.565	mm
package height	0.3	0.325	0.35	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	12	-	



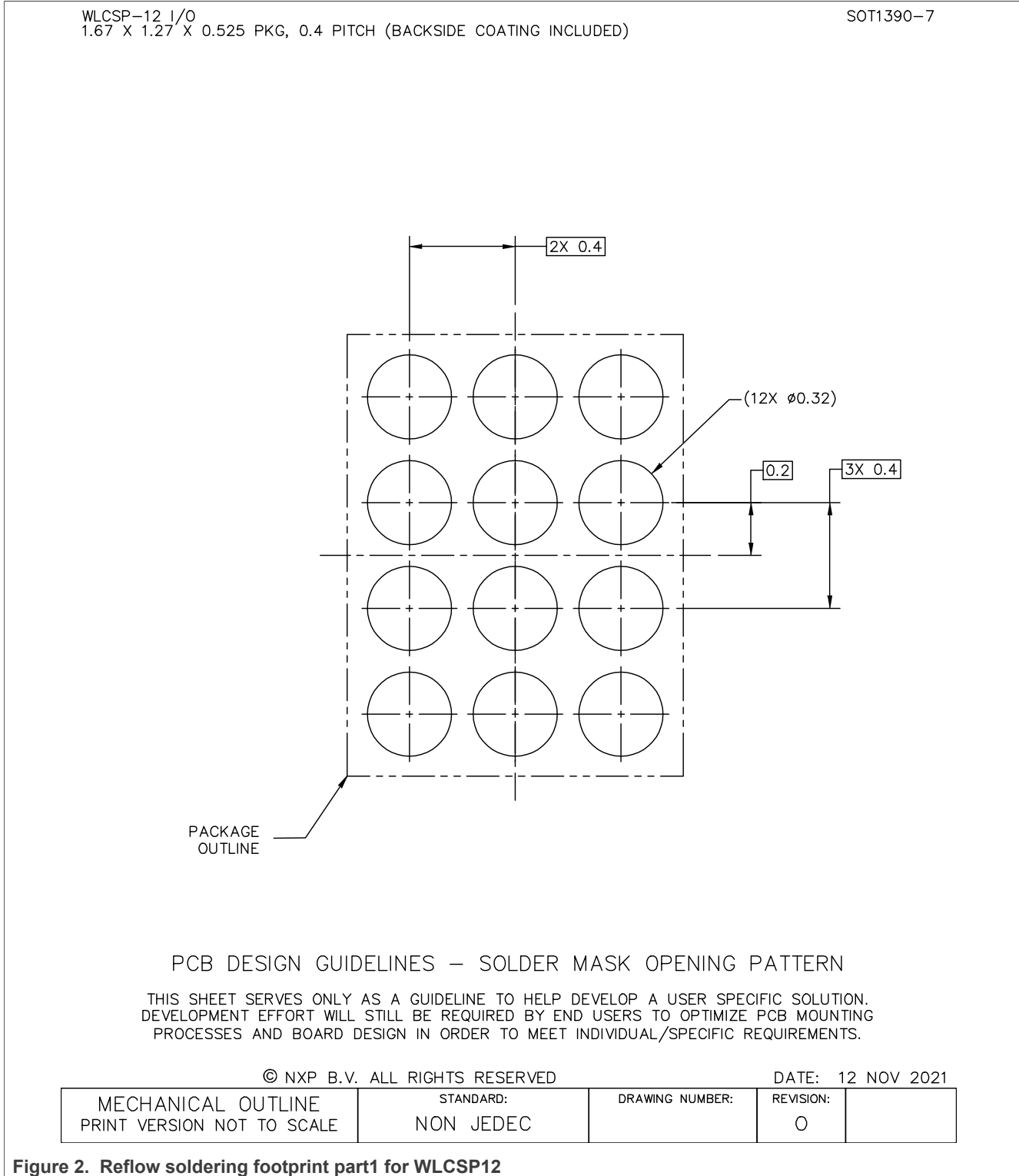
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2 Package outline



WLCSP12, wafer level chip-scale package; 12 bumps; 1.67 mm x 1.27 mm x 0.525 mm (backside coating included)

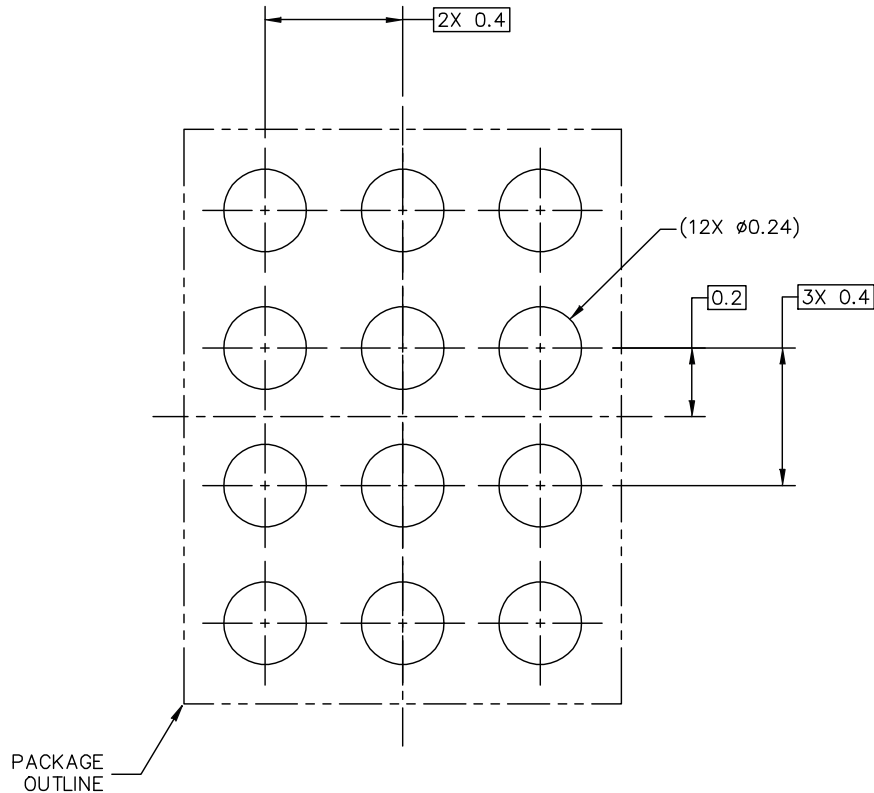
3 Soldering



WLCSP12, wafer level chip-scale package; 12 bumps; 1.67 mm x 1.27 mm x 0.525 mm (backside coating included)

WLCSP-12 I/O
1.67 X 1.27 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1390-7



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 12 NOV 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER:	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP12

WLCSP12, wafer level chip-scale package; 12 bumps; 1.67 mm x 1.27 mm x 0.525 mm (backside coating included)

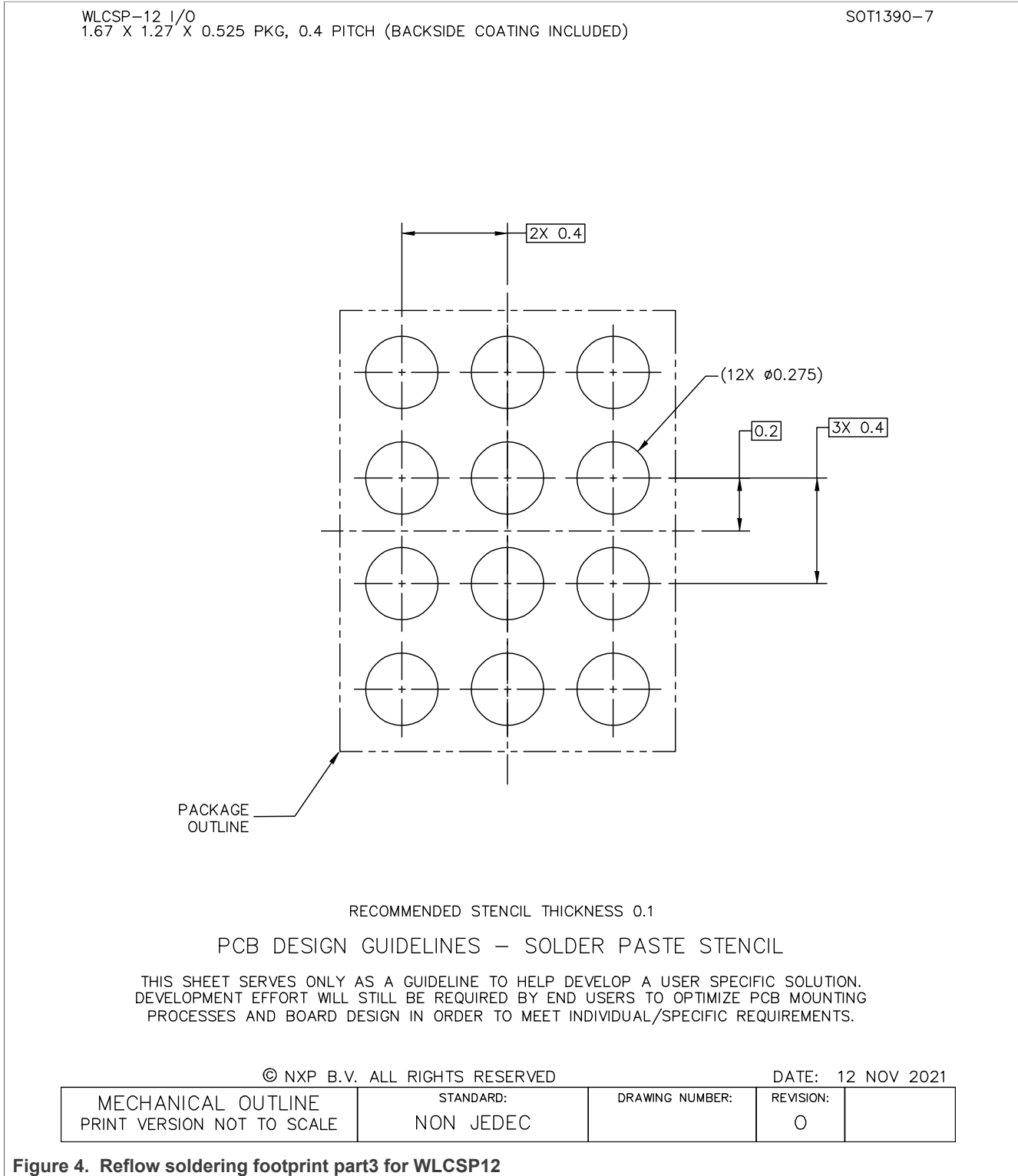


Figure 4. Reflow soldering footprint part3 for WLCSP12

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4 Legal information

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