SOT1384-5



1

wafer level chip-scale package; 9 bumps; 1.24 mm x 1.24 mm x 0.525 mm body (backside coating included)

8 August 2018

Package information

Package information

Package summary

Terminal position code B (bottom) WLCSP9 Package type descriptive code

Package style descriptive code WLCSP (wafer level chip-size package)

Mounting method type S (surface mount)

Issue date 08-08-2018 Manufacturer package code SOT1384

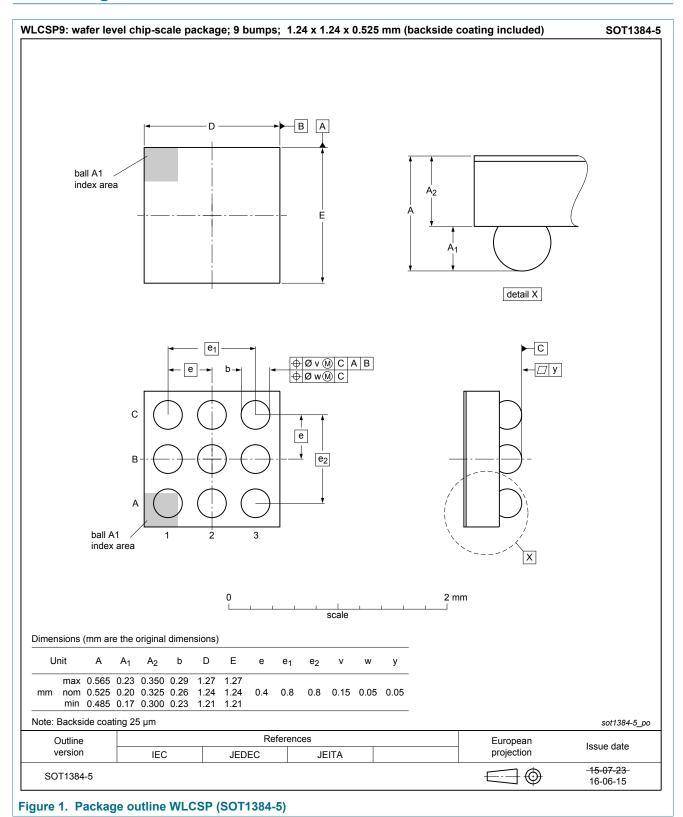
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	1.21	1.24	1.27	mm
package width	1.21	1.24	1.27	mm
seated height	0.485	0.525	0.565	mm
nominal pitch	-	0.4	-	mm



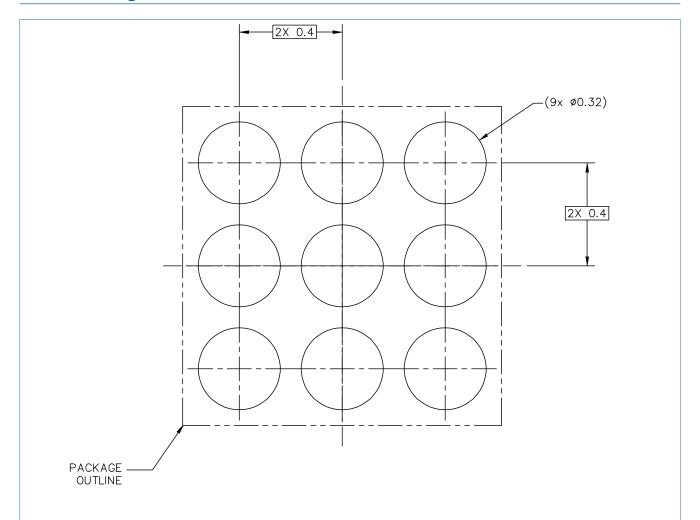
wafer level chip-scale package; 9 bumps; 1.24 mm x 1.24 mm x 0.525 mm body (backside coating included)

2 Package outline



wafer level chip-scale package; 9 bumps; 1.24 mm x 1.24 mm x 0.525 mm body (backside coating included)

3 Soldering



PCB DESIGN GUIDELINES - SOLDER MASK OPENING PATTERN

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MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
PRINT VERSION NOT TO SCALE	NON JEDEC		0	

Figure 2. Reflow soldering footprint part1 for WLCSP9 (SOT1384-5)

wafer level chip-scale package; 9 bumps; 1.24 mm x 1.24 mm x 0.525 mm body (backside coating included)

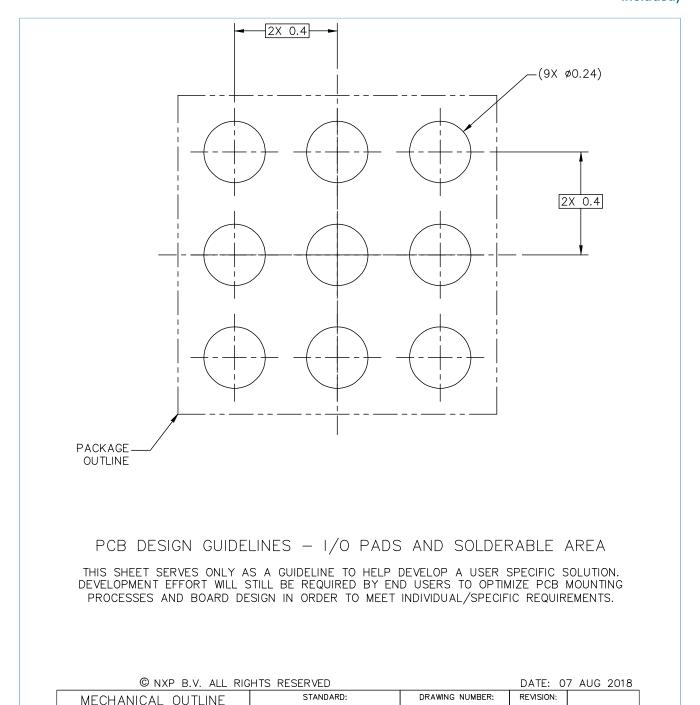


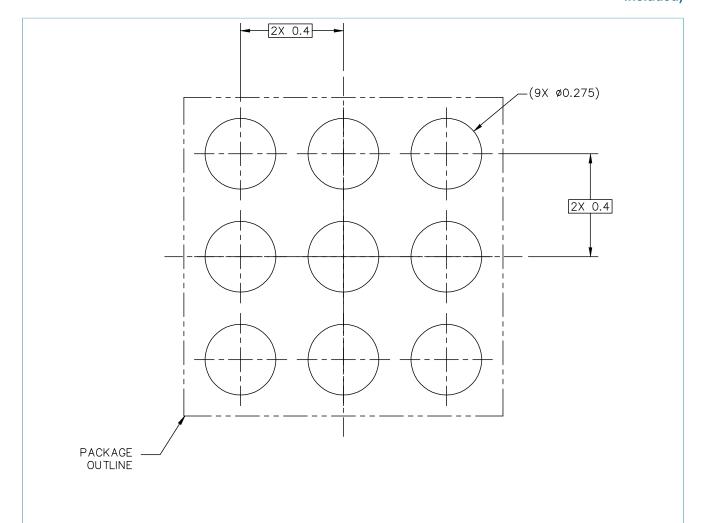
Figure 3. Reflow soldering footprint part2 for WLCSP9 (SOT1384-5)

PRINT VERSION NOT TO SCALE

NON JEDEC

0

wafer level chip-scale package; 9 bumps; 1.24 mm x 1.24 mm x 0.525 mm body (backside coating included)



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES - SOLDER PASTE STENCIL

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PRINT VERSION NOT TO SCALE	NON JEDEC		0	

Figure 4. Reflow soldering footprint part3 for WLCSP9 (SOT1384-5)

wafer level chip-scale package; 9 bumps; 1.24 mm x 1.24 mm x 0.525 mm body (backside coating included)

4 Legal information

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wafer level chip-scale package; 9 bumps; 1.24 mm x 1.24 mm x 0.525 mm body (backside coating included)

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