Document Number: MM912_637ER
Rev. 4.0, 14 Jan 2020

MM912_637, Silicon Mask Errata

Introduction

This mask set errata applies to the Analog mask M97W for these SMARTMOS products:

Device Revision Identification

Package	Part Number	Analog Mask ID	Analog Pass	MCU Mask ID
48 QFN-EP	MM912I637AM2EP	DA04M97W	2.4	DA01M96X
	MM912J637AM2EP	DA04M97W	2.4	DA01M96X
	MM912I637AV1EP	DA04M97W	2.4	DA01M96X
	MM912J637AV1EP	DA04M97W	2.4	DA01M96X
	MM912I637TM2EP	DA04M97W	2.4	DA01M96X
	MM912J637TM2EP	DA04M97W	2.4	DA01M96X
	MM912I637TV1EP	DA04M97W	2.4	DA01M96X
	MM912J637TV1EP	DA04M97W	2.4	DA01M96X
	SM912I637AM2EP	DA04M97W	2.4	DA01M96X
	SM912I637AM3EP	DA04M97W	2.4	DA01M96X
	SM912J637AM2EP	DA04M97W	2.4	DA01M96X
	SM912J637AM3EP	DA04M97W	2.4	DA01M96X
	SM912F637TM3EP	DA04M97W	2.4	DA01M96X
	SM912H637TM3EP	DA04M97W	2.4	DA01M96X
	SM912I637TM3EP	DA04M97W	2.4	DA01M96X
	SM912J637TM3EP	DA04M97W	2.4	DA01M96X

The device revision is indicated by a 1-character code after the device code. For instance the “A” in the “MM912J637AM2EP” indicates revision 2.4. All standard devices are marked with a device identification and build information code.

Device Build Information / Date Code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTZW1025”). The date is coded as four numerical digits, where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “1025” indicates the 25th week of the year 2010.

Device Part Number Prefixes

Some device samples are marked with a PM prefix. A PM prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MM prefix.

Silicon Revision Register - SRR

The analog die contains a silicon revision register to read the actual revision information. Mask M97W corresponds to silicon revision 2.4. The actual revision of the analog die is available in the SRR (Silicon Revision Register), accessible through the Die-to-Die interface.

Register Details

Offset [1] 0xFA

		7	6	5	4	3	2	1	0
R		0	0	MMREV			FMREV		
W									
Default Values	M97W	0	0	1	0	1	0	0	1

Notes

1. Offset related to 0x0200 for blocking access and 0x300 for non blocking access, within the global address space.

Field	Description
0-2 FMREV	MM912_637 analog die Silicon Revision Register Major Revision (all layers) - Those three bits represent the revision count of full mask change. Read only, writing will have no effect. The first Full Mask will have the count 00.
3-5 MMREV	MM912_637 analog die Silicon Revision Register Minor Revision (metal only) - Those two bits represent the number of metal changes applied to the full mask.Read only, writing will have no effect. The first Full Mask will have the count 00.

Analog Mask Errata

Excessive IIR Noise In Low Power Modes

General Description

IIR coefficients 1/64 and 1/128 are not usable in Low Power modes due to excessive noise generation.

Failure Mechanism

Due to the digital implementation, the enable signal for the programmable current measurement channel injects switching noise into the IIR filter due to repeated enable/disable sequences in Low Power mode.

Workaround/Solution

All IIR coefficients are usable in Normal mode. In addition, IIR coefficients of 1/8, 1/16, 1/32 are usable in Low Power modes. Recommendation is to use one of these coefficients in all modes. If this is not acceptable, an alternative recommendation is to switch to one of these coefficients (1/16, for example) before transitioning to Low Power mode.

HTF flag cannot be cleared after Thermal Shutdown

General Description

The Power, Clock and Reset (PCR) module sets the HTF (High Temperature Condition Flag) bit in the PCR Status register once a temperature warning is detected, or if the last reset was caused by a temperature shutdown event (TSDR). In the second case, writing HTF=1 does not clear the HTF flag, even if the high temperature shutdown condition is no longer present. See Table 74. PCR Status Register (PCR_SR (hi)) in the data sheet.

PCR Status Register (PCR_SR (hi))

Offset 0x02 Access: User read/write

	7	6	5	4	3	2	1	0
R	HTF	UVF	HWRF	WDRF	HVRF	LVRF	WULTCF	WLPMF
W	Write 1 will clear the flags							
Reset	0	0	0	0	0	0	0	0

Failure Mechanism

The cause of this issue is undetermined at this time. It is still under investigation.

Workaround/Solution

A system reset must be performed after Thermal Shutdown to clear the HTF flag.

Unwanted LIN Wake-up Behavior From Low Power Mode

General Description

If the LIN module is enabled (bit 2 =1, LIN_CTL register) before a transition from Normal Mode to Low Power mode, the LIN module will wake-up correctly if a valid LIN Wake-up event occurs.
However, if the LIN module is enabled and if the LIN bus is in a dominant state during the transition from Normal to Low Power mode, the LIN module will wake up on the next rising edge of the LIN bus, assuming that the duration between mode transition to rising edge is greater than the bus wake-up deglitcher (t_{PROPWL}, typical 80 µs). This scenario is depicted on the next graph.

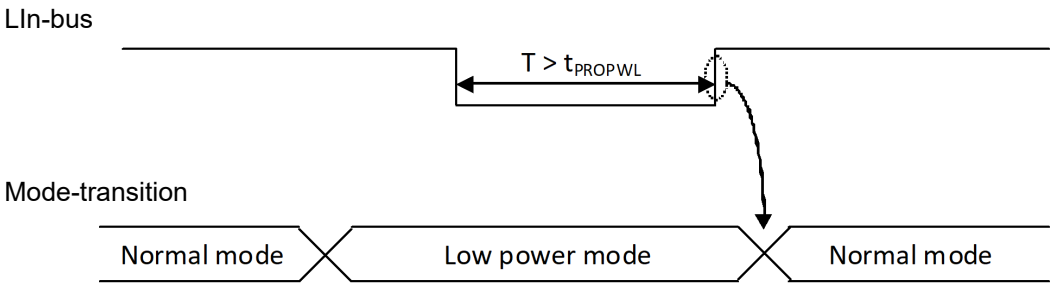

Figure 1. Usual Wake-up Scenario

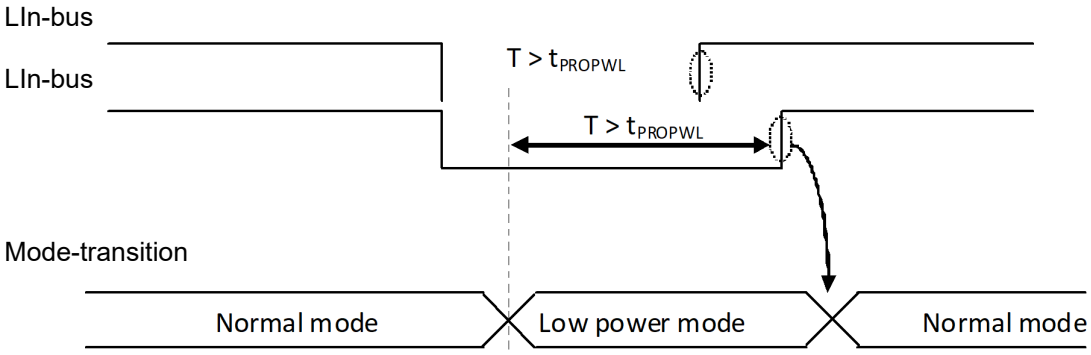

Figure 2. Unwanted LIN Wake-up Behavior from Low Power mOde

Failure Mechanism

When LIN is enabled before transition to Low Power mode, and if the LIN is in a dominant state, then due to a timing issue in the circuitry, the LIN switches to Low Power mode after the rest of the device. Under this condition, an unexpected falling edge on the RCV line occurs, leading to an unwanted wake-up condition.

Workaround/Solution

The LIN software must ensure that the LIN module is disabled before a transition to Low Power mode. In this case, the unwanted wake-up from low power is no longer present.

Non-Saturation of the Voltage Channel at High V_{SUP}

Description

The voltage channel is supposed to saturate at 0xFFFF whenever the voltage input is out of range (>35 V). When the voltage increases beyond 41 V, the code is no longer 0xFFFF and starts to decrease.

Failure Mechanism

The input stage of the sigma-delta converter is not biased correctly for voltages above 41 V.

Workaround/Solution

None required, since the anomalous behavior occurs above the operating voltage of the device, 1V below the absolute maximum rating.

V_{DDX} Overshoot on V_{SUP} Transients in Low Drop Out Conditions

Description

During a specific transient on V_{SUP}, V_{DDX} will generate an overshoot that will exceed the V_{DDX} Max Rating. The overshoot will only occur if the transient signal on V_{SUP} meets the conditions below:

1. V_{SUP} is initially at a level low enough to cause V_{DDX} to be in a low drop out condition (i.e. V_{SUP} below approximately 5.0 V and over LVRX)
2. From this level, V_{SUP} increases by approximately 10 V with a rise time faster than a few microseconds.

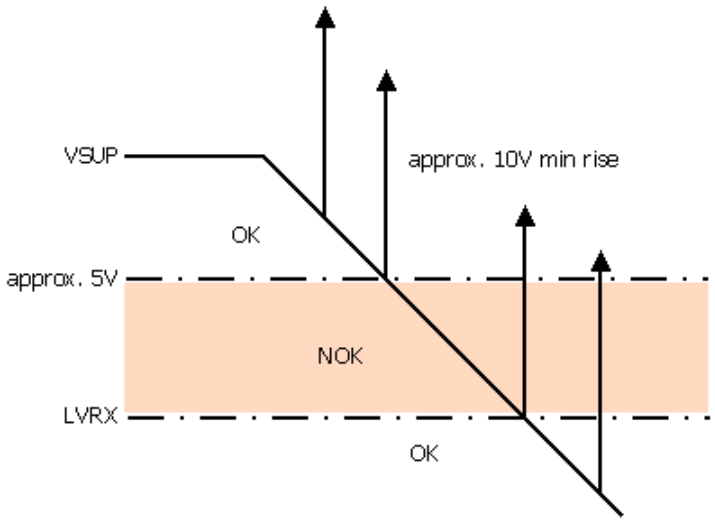

Figure 3. Transient Signal Shape

As shown in Figure 3, if the V_{SUP} transient occurs for levels of V_{SUP} > the V_{DDX} dropout voltage or V_{SUP} < V_{LVRX} (the Low Voltage Reset level), the V_{DDX} overshoot will not occur.

Failure Mechanism

While V_{SUP} rises according to above conditions, the V_{DDX} regulator will switch from low drop out mode to regulated mode. This transition will last several microseconds and may lead to an overshoot on V_{DDX}.

Workaround/Solution

To ensure V_{DDX} remains within its Max Ratings, it is recommended to add the following RC filter on VSUP (pin 21), as shown in Figure 4:

Minimum RC filter time constant = 47 µs
Recommended RC filter= 10 Ω and 4.7 µF (minimum value for the decoupling capacitor, according to datasheet)

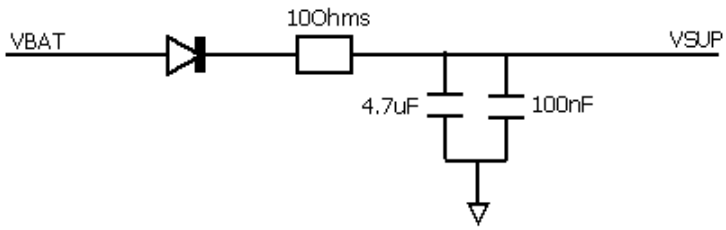

Figure 4. VSUP Recommended RC Filter Schematics

Note: Adding a resistor in the V_{SUP} path will reduce the device supply voltage and shift the device under- and over-voltage from a proportional drop, according to the resistor value and current consumption.

Revision History

Revision	Date	Description of Changes

4.0	1/2020	• Added the following part numbers:
		  • MM912I637TM2EP
		  • MM912J637TM2EP
		  • MM912I637TV1EP
		  • MM912J637TV1EP
		  • SM912F637TM3EP
		  • SM912H637TM3EP
		  • SM912I637TM3EP
		  • SM912J637TM3EP
		• Deleted the following part numbers:
		  • SM912I637AM2EPR2
		  • SM912I637AM3EPR2
		  • SM912J637AM2EPR2
		  • SM912J637AM3EPR2

3.0	3/2014	• Implemented Revision History page • Removed Xtrinsic logo. No other change to the document.

RoHS

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