MCXN23x_0P21K

Mask Set Errata

Mask Set Errata for Mask 0P21K

Revision History

This report applies to mask 0P21K for these products:

- MCXN236VDFT
- MCXN236VNLT
- MCXN235VNLT
- MCXN235VDFT

Table 1. Revision History

Revision	Date	Significant Changes
1.0	5/2024	Initial Revision

Errata and Information Summary

Table 2. Errata and Information Summary

Erratum ID	Erratum Title
ERR050875	CoreSight: AHB-AP can issue transactions where HADDR[1:0] is not aligned to HSIZE on the AHB
ERR051421	SAI: Synchronous mode with bypass is not supported
ERR051588	LPSPI:Reset transmit FIFO after FIFO underrun by LPSPI Slave.
ERR051617	I3C: In I2C compatibility mode read transaction not terminating correctly
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ERR052122	I3C : Data size limitation in Message mode DDR transfer
ERR052147	USB: ISO schedule issue in FS Host mode
ERR052241	CDOG: Restart command can't let timer count down

Known Errata

ERR050875: CoreSight: AHB-AP can issue transactions where HADDR[1:0] is not aligned to HSIZE on the AHB

Description

ARM errata 1624041

This erratum affects the following components:

• AHB Access Port.

The ARM Debug Interface v5 Architecture Specification specifies a TAR (Transfer Address Register) in the MEM-AP that holds the memory address to be accessed.

TAR[1:0] is used to drive HADDR[1:0] when accesses are made using the Data Read/Write register DRW.

When the AHB-AP is programmed to perform a word or half-word sized transaction the AHB-AP does not force HADDR[1:0] to be aligned to the access size. This can result in illegal AHB transactions that are not correctly aligned according to HSIZE if HADDR[1:0] is programmed with an unaligned value.

Conditions:

1) TAR[1:0] programmed with a value that is not aligned with the size programmed in the CSW register of the AHB-AP.

2) An access is initiated by an access to the Data Read/Write Register (DRW) in the AHB-AP.

Implications:

As a result of the programming conditions listed above, AHB-AP erroneously initiates an access on the AHB with HADDR[1:0] not aligned to the size on HSIZE. This might initiate an illegal AHB access.

Workaround

TAR[1:0] must be b00 for word accesses, TAR[0] must be b0 for half-word accesses.

Software program should program TAR with an address value that is aligned to transaction size being made.

ERR051421: SAI: Synchronous mode with bypass is not supported

Description

The SAI does not receive or transmit when:

Scenario 1. The transmitter is configured for synchronous mode (TCR2[SYNC] = 0b1), in the Transmit Configuration 2 register, and the receiver is in bypass (RCR2[BYP]=0b1), in the Receiver Configuration 2 register, then there will not be a bit clock as it is the source of the BCLK.

Scenario 2. The receiver is configured for synchronous mode (RCR2[SYNC] = 0b1) in the Receiver Configuration 2 register and the transmitter is in bypass (TCR2[BYP]=0b1), in the Transmit Configuration 2 register, then there will not be a bit clock as it is the source of the BCLK.

Workaround

If scenario 1, then set the TCR2[BCI] = 0b1, in the Transmit Configuration 2 register.

If scenario 2, then set the RCR2[BCI] = 0b1, in the Receiver Configuration 2 register.

ERR051588: LPSPI:Reset transmit FIFO after FIFO underrun by LPSPI Slave.

Description

Transmit FIFO pointers are corrupted when a transmit FIFO underrun occurs (SR[TEF]) in slave mode.

Workaround

When clearing the transmit error flag (SR[TEF] = 0b1) following a transmit FIFO underrun, reset the transmit FIFO (CR[RTF] = 0b1) before writing any new data to the transmit FIFO.

ERR051617: I3C: In I2C compatibility mode read transaction not terminating correctly

Description

The I3C module can operate in I2C compatibility mode to support I2C devices. However when operating in this mode, the end of any read transaction may terminate with a repeated START followed by the STOP instead of only a STOP.

Workaround

In I2C compatibility mode, the use of no skew should be avoided and must set to MCONFIG[SKEW] = 1.

ERR051629: LPUART:Transmit Complete bit (STAT[TC]) is not set.

Description

When the CTS pin is negated and the CTS feature is enabled (MODIR[TXCTSE] = 0b1) and the TX FIFO is flushed by software then, the Transmit Complete (STAT[TC]) flag is not set.

Workaround

Clear (MODIR[TXCTSE]) bit and reset the transmit FIFO (FIFO[TXFLUSH] = 0b1) when flushing the FIFO with CTS enabled(MODIR[TXCTSE] = 0b1).

ERR051704: DCDC: Failure changing to Low drive-strength mode

Description

The DCDC output may fail when transitioning from Normal to Low drive-strength, resulting in the DCDC output voltage dropping to the point it is not able to adequately power the VDD_CORE supply, or causes temporary brown-out conditions. This failure may occur when both of these conditions occur:

1) The transition from Normal drive strength (DCDC_VDD_DS = 10b) to Low drive-strength (DCDC_VDD_DS = 01b) occurs when the DCDC is actively switching the output.

2) The voltage level set in the bitfield SPC->LP_CFG[DCDC_VDD_LVL] is greater than or equal to the current output voltage of the DCDC.

Because this failure requires a specific timing to manifest, it may fail very infrequently in an application. The greater the load current of the DCDC, the more likely the failure will occur because the DCDC will spend more time in the active switching period. A higher rate of transitioning to Low drive-strength will also see a higher failure rate.

There are two scenarios when the DCDC drive-strength can transition from Normal to Low drive-strength, and this failure may occur:

1) While the MCU is in Active power mode, and the application changes the drive-strength setting by writing 01b to the bitfield SPC->ACTIVE_CFG[DCDC_VDD_DS]. Writing this bitfield will start the transition to Low drive-strength.

2) When the MCU enters a low-power mode (Deep Sleep, Power Down, or Deep Power Down), and Active mode uses Normal drive-strength with ACTIVE_CFG[DCDC_VDD_DS] = 10b, while the low-power mode uses Low drive-strength with LP_CFG[DCDC_VDD_DS] = 01b.

Workaround

This issue will always be avoided when the voltage level at the low-power low drive-strength is lower than the current output voltage of the DCDC. Before transitioning to Low drive-strength, ensure the voltage level in LP_CFG[DCDC_VDD_LVL] is lower than the voltage level in Normal drive-strength configured by ACTIVE_CFG[DCDC_VDD_LVL]. As part of this workaround, the voltage level used in Low drive-strength configured by LP_CFG[DCDC_VDD_LVL] must not be set to the maximum value 11b for 1.2 V at any time in an application.

If the desired voltage level in LP_CFG[DCDC_VDD_LVL] is the same as the level currently set in ACTIVE_CFG[DCDC_VDD_LVL], a workaround is to temporarily increase the voltage level in ACTIVE_CFG[DCDC_VDD_LVL], and then transition to Low drive-strength with the lower level in LP_CFG[DCDC_VDD_LVL]. Here is the sequence for this workaround:

1) Ensure LP_CFG is configured for Low drive-strength and the desired voltage level in Low drive-strength mode

2) Wait for the SPC bit SC[BUSY] to be clear.

3) Write ACTIVE_CFG[DCDC_VDD_LVL] with the value for the voltage level one step higher than the desired level in LP_CFG[DCDC_VDD_LVL].

4) Start the transition to Low drive-strength

If the workaround sequence above is used when the MCU enters a low-power mode, then when the MCU wakes the DCDC will return to Normal drive-strength with the output voltage level configured in SPC->ACTIVE_CFG[DCDC_VDD_LVL]. If a lower voltage level is preferred, the application can lower DCDC voltage by waiting for the bit SC[BUSY] to be clear and writing the new voltage level to SPC->ACTIVE_CFG[DCDC_VDD_LVL].

ERR051713: ADC: Extra conversion can occur when moving to low power mode

Description

When high-priority trigger exceptions are enabled (ADCx->CFG[HPT_EXDI] = 0x1) and the ADC command uses the "Repeat until true" compare option (ADCx->CMDHa[CMPEN] = 0x3), an extra conversion occurs at the end of the conversion cycle if a higher priority trigger is asserted when a low power request is also made. This can result in erroneous extra data in the result FIFO and/or prevent the ADC module from being disabled in the low power mode (even if the Doze enable bit is set - ADCx->CTRL[DOZEN] = 0x1).

Workaround

The ADC workaround is to do ONE of the following:

- Disable the ADC before entering low power mode (ADCx->CTRL[ADCEN] = 0)

- Disable high priority exceptions (ADCx->CFG[HPT_EXDI] = 0x1)

- If high priority exceptions are enabled (ADCx->CFG[HPT_EXDI] = 0x1) and "Repeat until true" compare option is used (ADCx->CMDHa[CMPEN] = 0x3), then the trigger command select (ADCx->TCTRLa[TCMD]) pointing to that command must be the highest priority (ADCx->TCTRLa[TPRI] = 0).

- User software waits for final conversion to be completed before entering low power mode.

ERR051874: I2C clock stretching mode is not supported

Description

I3C IP when working as I2C master mode it doesn't support Clock stretching feature.

Workaround

Application must not use I2C clock stretching feature. It will create clock contention on bus.

I2C Targets on the bus must keep Clock stretching feature disabled.

ERR051989: PWM: output may be abnormal when the value of phase delay register is reduced from a non-zero value to 0.

Description

When the value of the SMxPHASEDLY register is reduced from a non-zero value to 0 and the SMxCTRL2[RELOAD_SEL]=1, the submodule x may output an unexpected wide PWM pulse (x=1,2,3).

Workaround

The minimum value of the SMxPHASEDLY register should be set as 1 in this process. To realize no phase delay between the submodule 0 and submodule x in this process, set the SMxPHASEDLY=1, SMxINIT=SM0INIT–1, SMxVALy=SM0VALy–1 (x=1,2,3, y=0,1,2,3,4,5).

ERR051998: ROM: Command "get-property 12" not supported when using USB interface

Description

When using the USB interface to access the device in ISP mode, command "get-property 12" returns a fail result. This applies to both Full-Speed and High-Speed USB interfaces.

Workaround

There is no workaround for this issue. Customers should not use the "get-property 12" command when using USB as the ISP mode interface.

ERR052108: ROM: LDO_SYS VDD level not returned to Normal voltage range after programming fuses

Description

When programming any fuse using the ROM API, the voltage level of the LDO_SYS is not returned to Normal Voltage level (1.8V). That is, SPC0->ACTIVE_CFG[SYSLDO_VDD_LVL] = 1.

Workaround

User software should return the LDO_SYS voltage level to normal level immediately after programming fuses (SPC0->ACTIVE_CFG &= ~SPC_ACTIVE_CFG_SYSLDO_VDD_LVL_MASK;).

Note that the SDK functions which program fuses already account for this errata.

ERR052122: I3C : Data size limitation in Message mode DDR transfer

Description

The message length in DDR message(DMA) mode is defined in MWMSG_DDR_CONTROL2 [9:0].LEN field. The 2 MSBs [9:8] of this field has no effect on operation. Only [7:0] part of this field is taken as length in number of Half words. So, for max value of 3FF h in this field is taken as FF h (255) by hardware , consequently the maximum amount of actual data gets limited as per the operation type. For Read operation the actual data size will be (255 - 2) = 253 half-words (506 bytes) and for write operation it is (255 -1) = 254 halfword (508 bytes)

Workaround

Application need to limit the data size for Write and Read operation in message(DMA) mode of DDR transfer. Configure MWMSG_DDR_CONTROL2 [9:0].LEN = FF h, For Read frame data receive size will be 506 bytes and for Write frame data transmit size will be 508 bytes for a single frame.

ERR052147: USB: ISO schedule issue in FS Host mode

Description

When working in FS Host mode, for ISO communication, if the first ISO package is equal or greater than about 238 bytes, then the second ISO transaction could not be scheduled in the same 1 ms frame.

For example, a typical application case affected is audio bi-directional communication with 48 KHz sample rate, 24 bit per sample and 2 channels for both direction. In this case, we need one ISO IN 288 bytes (>238 bytes) + one ISO OUT 288 bytes (>238 bytes) in one 1 ms frame. But actually, only one ISO OUT 288 bytes or only one ISO IN 288 bytes is available in one 1 ms frame due to the IP limitation.

Workaround

No workaround.

ERR052241: CDOG: Restart command can't let timer count down

Description

Due to this errata, once RESTART command is written to RESTART register, the Instruction Timer is continually reloaded with the value in the RELOAD register and the counter will not count down (until subsequent accesses of CDOG registers).

Workaround

Replace RESTART register write instructions in all locations with a write to the STOP register immediately followed by a write to the RELOAD and START register. Both the STOP and START registers should be written with the same value in this situation..

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