MCXC_x43_x44_1N71K

Mask Set Errata

Mask Set Errata for Mask 1N71K

Revision History

This report applies to mask 1N71K for these products:

- MCXC444VLH
- MCXC143VFM
- MCXC143VFT
- MCXC243VFT
- MCXC443VMP
- MCXC443VLH
- MCXC144VFM
- MCXC244VFM
- MCXC144VFT
- MCXC244VFT
- MCXC444VMP

Table 1. Revision History

Revision	Date	Significant Changes
1.0	4/2024	The following errata were revised. • ERR009457
0.1	3/2024	Initial Revision

Errata and Information Summary

Table 2. Errata and Information Summary

Erratum ID	Erratum Title
ERR002580	UART: Start bit sampling not compliant with LIN 2.1 specification
ERR002581	Data bit sampling not compliant with LIN 2.1 specification
ERR006396	sLCD: LCD_GCR[RVTRIM] bits are in reverse order
ERR007822	USBReg: Some devices have VREG_OUT trim value incorrectly programmed
ERR007857	UART: WT timer in T=0 mode and CWT timer in T=1 mode can expire between 0.2 ETU to 0.8 ETU earlier than programmed.
ERR007914	PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.
ERR007950	LLWU: When exiting from Low Leakage Stop (LLS) mode using the comparator, the comparator ISR is serviced before the LLWU ISR
ERR007986	LPUART: The LPUART_TX pin is tri-stated when the transmitter is disabled
ERR008058	ROM: COP can't be re-enabled in application code due to being disabled by ROM boot code

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Table 2. Errata and Information Summary (continued)

Erratum ID	Erratum Title
ERR008060	ROM: Bytes sent from host over I2C and SPI interfaces may be lost
ERR008594	ROM: I2C0_A1 register does not contain the reset default value when MCU boots from ROM
ERR008595	ROM: ROM read memory command may read the incorrect data back from flash in some cases
ERR008777	I2C: Address match wake-up from low-power mode cannot receive data
ERR008992	AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode
ERR009308	I2C: I2C does not hold bus between byte transfers in receive and may result in lost data
ERR009380	FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang
ERR009457	Flashloader/ ROM Bootloader: The peripheral auto-detect code in bootloader can falsely detect presence of SPI host causing non-responsive bootloader
ERR010527	LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters

Known Errata

ERR002580: UART: Start bit sampling not compliant with LIN 2.1 specification

Description

The LIN 2.1 specification states that start bits should be checked at sample 7, 8, 9, and 10. The UART module checks the start bit at samples 3, 5, and 7 instead.

Workaround

Start bits longer than 5/16 of a bit time are guaranteed to be recognized. Start bits shorter than this should not be used with this version of the UART because they might not be recognized.

ERR002581: Data bit sampling not compliant with LIN 2.1 specification

Description

The LIN 2.1 specification requires equidistant sampling of the data bit, which means that the sample window is the same for all data bits and resynchronization of the sample point is done only on the start bit. The UART module performs resynchronization of the bit sampling on any falling edge. This can cause unpredictable sample results in the case of bit distortions.

Workaround

No workaround exists.

ERR006396: sLCD: LCD_GCR[RVTRIM] bits are in reverse order

Description

The four bits of LCD_GCR[RVTRIM] are in reverse order, in such a way that the LSB corresponds to bit 27 and the MSB corresponds to bit 24 of the LCD_GCR. The RVTRIM adjustment from lower voltage to higher voltage does not follow a linear increase in the LCD_GCR[RVTRIM] value. The RVTRIM adjustment should follow this sequence:

0,8,4,12,2,10,6,14,1,9,5,13,3,7,11,15

to achieve a linear increase from lower voltage to higher voltage.

The reset value of this field is still 8, which corresponds to a low voltage value of the VIREG.

Workaround

You can use a lookup table with the correct order of RVTRIM values for a linear change on the VIREG voltage (contrast). If planning to use a user-selectable contrast, a memory buffer is required to keep track of the logic value of the RVTRIM. When required to increase or decrease the contrast of the LCD, the buffer pointer should be increased or decreased accordingly and the corresponding value from the lookup table should be written to the LCD_GCR[RVTRIM].

To avoid a low voltage on VIREG after reset, LCD_GCR[RVTRIM] must be updated during the LCD initialization routine.

ERR007822: USBReg: Some devices have VREG_OUT trim value incorrectly programmed

Description

After exiting reset, the device loads its programmed VREG_OUT trim value. On devices that have an incorrect trim value, when asserting reset, VREG_OUT will be 3.3V and when reset is de-asserted VREG_OUT will be 3.02V.

Workaround

Program SIM_USBPHYCTL[USB3VOUTTRG]=0b110 to set VREG_OUT equal to 3.3V.

ERR007857: UART: WT timer in T=0 mode and CWT timer in T=1 mode can expire between 0.2 ETU to 0.8 ETU earlier than programmed.

Description

In ISO7816 receive mode, the wait timer (WT) used in T=0 mode and the character wait timer (CWT) used in T=1 mode can expire between 0.2 ETU to 0.8 ETU earlier than programmed. The early expiration of the timers can cause software to discard valid data during communication.

Workaround

To minimize the possibility of discarded data, in T=0 mode, program the WI counter field for the wait timer as WWT + D **480 ETUs for both receive and transmit.** ETUs for both receive and transmit.

To minimize the possibility of discarded data, in T=1 mode, program the CWI counter field for the character wait timer as CWT + 5 ETUs when receiving and CWT + 4 ETUs when transmitting.

ERR007914: PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.

Description

If a write to the PIT module enable bit (PIT_MCR[MDIS]) occurs within two bus clock cycles of enabling the PIT clock gate in the SIM_CG register, the write will be ignored and the PIT will fail to enable.

Workaround

Insert a read of the PIT_MCR register before writing to the PIT_MCR register. This guarantees a minimum delay of two bus clocks to guarantee the write is not ignored.

ERR007950: LLWU: When exiting from Low Leakage Stop (LLS) mode using the comparator, the comparator ISR is serviced before the LLWU ISR

Description

The comparator's interrupt service routine when exiting from LLS mode is serviced before the LLWU ISR. Clearing the comparator flag in CMPx_SCR clears the corresponding comparator flag in the LLWU_Fx register which may be used to determine wakeup source in the LLWU ISR.

Workaround

Code can implement a software flag in the CMP ISR to retain wakeup source if required by software.

ERR007986: LPUART: The LPUART_TX pin is tri-stated when the transmitter is disabled

Description

The LPUART transmitter is disabled when the MCU:

• Enters Stop, Wait, or VLPS with the DOZEN bit set

• Enters LLS or VLLS power mode.

The LPUART will tri-state the LPUART_TX pin when the transmitter is disabled, which may result in leakage current.

Workaround

Before the MCU enters Stop, Wait, or VLPS power mode with the DOZEN bit set or enters the LLS or VLLS power mode, enable the pullup resistor on the LPUART_TX pin to ensure the pin does not float. If the TXINV bit is set, enable the pulldown resistor on the LPUART_TX pin.

ERR008058: ROM: COP can't be re-enabled in application code due to being disabled by ROM boot code

Description

COP is disabled by ROM boot code,can't be re-enabled in application code. If the MCU boots up from ROM and then jumps into flash code, the flash code will fail to enable COP again.

Workaround

To use the COP watchdog in an application, write 00b to FOPT[BOOTSRC_SEL] bit to boot from flash out of reset.

ERR008060: ROM: Bytes sent from host over I2C and SPI interfaces may be lost

Description

Ping packet byte to the I2C and SPI loss occurs occasionally when the target is out of reset.

Workaround

1.Run the I2C/SPI interface at 48 MHz core clock.

2.Insert a delay of at least 1 ms between the two bytes of the initial ping packet sent from the host to the device

3.If no response from the device is received, the host should re-send the ping packet

ERR008594: ROM: I2C0_A1 register does not contain the reset default value when MCU boots from ROM

Description

When the MCU boots from ROM, then the I2C0_A1 register will not hold the reset default value (i.e. 0x00) from the ROM boot.

Workaround

Re-initialize the I2C0_A1 register when booting from ROM and when I2C0 is used by applications.

ERR008595: ROM: ROM read memory command may read the incorrect data back from flash in some cases

Description

When using the ROM Read Memory command to read the same flash address twice, if in the middle of the two consecutive reads, the flash address space content is changed by either a flash erasing or programming command, the second Read Memory command does not return the correct value in flash, and instead returns the same value as the first read. The root cause is that the flash cache is not disabled and retains the previous content of the flash.

Workaround

Use one of two options:

1) Avoid continuous read of the same flash address space twice

2) Invalidate flash cache before second read of the same flash address

ERR008777: I2C: Address match wake-up from low-power mode cannot receive data

Description

When the device is in a low-power mode that supports address match wake-up, receiving a matching address will wake up the MCU, however, the I2C will not respond correctly. I2C traffic after the wake-up address will not generate TCF interrupt events.

Workaround

Either one of the following sequences will enable the address match wake-up to operate correctly:

1) Send only the matching slave address followed by a repeated start and then resend the matching slave address including any subsequent data.

2) Send only the matching slave address followed by a stop condition and then resend the matching slave address including any subsequent data.

ERR008992: AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode

Description

Upon entry into VLPS from VLPR, if NMI is asserted before the VLPS entry completes, then the NMI does not generate a wakeup to the MCU. However, the NMI interrupt will occur after the MCU wakes up by another wake-up event.

Workaround

There are two workarounds:

1) First transition from VLPR mode to RUN mode, and then enter into VLPS mode from RUN mode.

2) Assert NMI signal for longer than 16 bus clock cycles.

ERR009308: I2C: I2C does not hold bus between byte transfers in receive and may result in lost data

Description

When the I2C module is in receive mode, the bus is typically held by simply not reading the I2C_D register. However, in devices with this errata, the bus is not held between byte transfers by this action. If the I2C_D register and the data buffer are full, incoming data from an I2C device will overwrite data in the data buffer.

Workaround

When configured to receive data, the delay in processing incoming bytes should be minimized. Delay can be minimized by the use of DMA or increased interrupt priority.

ERR009380: FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang

Description

Accessing a FlexIO register when the FlexIO functional clock is disabled (the clock source configured to 0 in PCC_FLEXIO0[PCS], or the selected clock source is disabled) will hang the bus and the access will stall forever.

Workaround

Always enable the FlexIO functional clock before accessing any FlexIO register.

ERR009457: Flashloader/ ROM Bootloader: The peripheral auto-detect code in bootloader can falsely detect presence of SPI host causing non-responsive bootloader

Description

During the active peripheral detection process, the bootloader can interpret spurious data on the SPI peripheral as valid data. The spurious data causes the bootloader to shutdown all peripherals except the "falsely detected" SPI and enter the command phase loop using the SPI. After the bootloader enters the command phase loop using the SPI, the other peripherals are ignored, so the desired peripheral is no longer active.

The bootloader will not falsely detect activity on the I2C, UART, or USB interfaces, so only the SPI interface is affected.

Workaround

Ensure that there is an external pull-up on the SPI chip-select pin or that the pin is driven high. This will prevent the bootloader from seeing spurious data due to activity on the SPI clock pin.

ERR010527: LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters

Description

When the LPUART transmitter is idle (LPUART_STAT[TC]=1), two break characters may be sent when using LPUART_CTRL[SBK] to send one break character. Even when LUART_CTRL[SBK] is set to 1 and cleared (set to 0) immediately.

Workaround

To queue a single break character via the transmit FIFO, set LPUART_DATA[FRETSC]=1 with data bits LPUART_DATA[T9:T0]=0.

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