Document Number: MCIMX31CE
Rev. 5.7, 1/2013

MCIMX31 and MCIMX31L Chip Errata

M91E, Rev. 2.0 and Rev. 2.0.1

This document contains errata information for:

MCIMX31 and MCIMX31L (i.MX31 and i.MX31L) for the silicon masks 2.0 and 2.0.1, shown in Table 1.

Table 1. Silicon Revision

Silicon Revision	Part Number
2.0	“C” at the end
2.0.1	“D” at the end

Table 2 provides silicon errata information for SoC/system-related issues, the ARM® Platform, and integrated peripherals.

Table 3 provides silicon errata information for the USB Host controller designed by TDI (formerly ARC) partners with ChipIdea.

Third-party errata for the ARM core (ARM Ltd.), Memory Stick® controller (Sony Corp.), MPEG-4 encoder (Hantro), and MBX graphic’s accelerator (ARM Ltd. and Imagination Technologies Ltd.) is provided when they exist by their corresponding companies. Refer to Table 4 for details on third-party errata and modules versions used.

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1 Errata

Table 2 provides silicon errata information for SoC/system-related issues, the ARM Platform, and integrated peripherals.

Table 2. Chip Errata for i.MX31

Errata ID	Summary	Details	Mask Rev.	
MSIls19340	**Module Affected:** Fusebox **Title:** Fusebox access from JTAG (SJC)—different frequency needed for read/write **Release Date:** 2/13/2006	**Description:** When attempting to write-to and read-from the fuse boxes through JTAG, using the same clock period of TCK, the following occurs: When using a clock period lower than 414 ns, the writing process does not execute as expected. This is because the epm_program signal of the fusebox is not stable for a sufficient period of time to be sampled (because of TCK). As a result, thus the epm_ready signal does not have sufficient time to activate (activate low in this case), and as a result of this, the program does not execute. To operate the program correctly, increase the period of TCK; however, when doing so, the reading process does not execute as expected. This is because the ready signal (in the fusebox_analog model) stays low for only 84 ns, so it cannot be captured when the clock period of TCK is very high. Minimal frequency limit for *Read* access is 11.9 MHz. This is due to a short ready signal from the analog part. The maximum frequency limit for write access is 2.4 MHz due to epm_program short assertion time (derived from TCK cycle). **Workaround:** Use different frequency for fuse write and read cycles. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhl23542	**Module Affected:** EMI **Title:** Writing in Null Memory locations overwrites the WEIM control registers **Release Date:** 2/13/2006	**Description:** When writing to 0xb802a230 (null memory location), the contents of the WEIM control registers are overwritten. Because of this, it is not possible to access the WEIM CS0, CS1, CS2, CS3, CS4, and CS5 locations. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhl22831	**Module Affected:** SDMA **Title:** debug_evt_chn_lines not generated on channel 0 start **Release Date:** 2/13/2006	**Description:** SDMA debug_evt_chn_line[0] is not asserted on channel start event. Operation does function correctly on a restart event. **Workaround:** Switch to another channel and back to restart channel 0 and cause the line to assert. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
DSPhl25117	**Module Affected:** RNGA **Title:** Osc_counter_cntrl register will not reset osc1/osc2 if in STOP_CLKS state. **Release Date:** 2/13/2006	**Description:** Writing to the Oscillator Counter Control register will not reset the oscillator counter 1 if the RNGA FSM is in STOP CLOCKS state. The same is true for Counter 2. The problem is caused by the logic to reset the counters, which requires a rising edge of shft_reg_clk_1. This signal is not active during the STOP_CLK state. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhl22960	**Module Affected:** CSPI **Title:** Negation of SS when FIFO empty and SSCTL=0 **Release Date:** 2/13/2006	**Description:** The CSPI negates SS when the FIFO becomes empty with SSCTL= 0. Software cannot guarantee that the FIFO will not drain because of higher priority interrupts and the non-realtime characteristics of the operating system. As a result, the SS will negate before all of the data has been transferred to/from the peripheral. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhl20719	**Module Affected:** PWM **Title:** ipp_do_pwmo behavior error when POUTC = 2'b01 **Release Date:** 2/13/2006	**Description:** Currently, ipp_do_pwmo remains 0 for POUTC = 2'b01 and the sample value being used is equal to 0. The correct behavior is that the value of ipp_do_pwmo is equal to 1. **Workaround:** Any waveform that is intended to be generated with POUTC = 2'b01, can be generated with POUTC = 2'b00, setting by suitably alternating sample values. This can be implemented in software. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	

DSPhl24788	**Module Affected:**
	SSI
	Title:
	dma rx requests not generated by SSI after receiver is disabled
	Release Date:
	2/13/2006
		Description:
		Given the scenario:
		1. An external driver is configured to transmit data to SSI2.
		2. After four words are received in Rx FIFO, then rx_en is disabled in SCR register.
		3. DMA is configured to transfer data from Rx FIFO to memory.
		In this situation, the SSI does not generate ipd_ssi_rx1_dmareq_b or ipd_ssi_rx0_dmareq_b. This is because the following logic flaw in ssi_irq.v:
		`assign ipd_ssi_rx1_dmareq_b = !(rx_dma_en & tch_en & rx_en & rx1_dma & ssi_en);`
		`assign ipd_ssi_rx0_dmareq_b = !(rx_dma_en & rx_en & rx0_dma & ssi_en);`
		Notice that rx_en is ANDed in this example logic to generate the requested signals. Therefore, when the receiver (rx_en) is disabled, the DMA Rx request is not generated at all.
		Fix Plan/Status:
		Not Fixed
			Rev. 2.0	Rev. 2.0.1

DSPhl20608	**Module Affected:** UART **Title:** When the UART is in Doze mode, Xfert of first character transmitted is not completed properly. **Release Date:** 2/13/2006	**Description:** The following test was carried out to pinpoint the errant behavior of the UART: • Set UART Doze bit to 1. Note, in this mode UART must complete any ongoing transmission, and must not begin any new transmission. • Begin transmitting the first character. • Enter into ARM Doze mode. • Continue first character Xfert. • Send second character. • Exit ARM Doze mode. • Transmit third character. • Check Rx FIFO. At the end of this test sequence, the UART Rx FIFO must contain only the first and the third character. *UART behavior description:* The UART performs this sequence correctly except for the read of the third character. The third character does not input properly into the Rx FIFO. After inspecting the vcd, it was found that the UART does not complete the Xfert of the first character properly. At the end of the Xfert of the first character, the rxd_from_decoder signal is maintained at 0 instead of 1. Because of this erroneous value, the start bit of the third character received is not detected properly, which is why an incorrect character value is read in the Rx FIFO. **Workaround:** No impact on performance. Ensure that the Rx FIFO is empty before entering Doze mode. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
DSPhI23796	**Module Affected:** UART **Title:** TXD does not mark 1s when transmitter is disabled in the middle of transmission **Release Date:** 2/13/2006	**Description:** In the UART, the TXD/TXD_MUX pin does not begin marking 1s when the transmitter is disabled during the middle of a transmission. This is not consistent with the UART module specifications within the reference manual. In the UART's submodule uart_txblock and its submodule uart_tx_ir, although the signal nrz_encoded becomes 1 two clock cycles after the UART is disabled, it is unable to pass the value to uart_txd_reg because the clock tx_m_clk is no longer available (clock tx_m_clk is gated). **Workaround:** Ensure that TX FIFO is empty before disabling the UART or its transmitter. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhI22781	**Module Affected:** UART **Title:** Transmitting a break condition results in a frame error in the current character transmitting **Release Date:** 2/13/2006	**Description:** For the specified version of IP UART, transmitting a break condition (assert SNDBRK UCR1[4]) results in a frame error in the current character transmission in progress. The reason is the stop bit of current character is destroyed (becomes a narrow pulse other than a valid one). This is not consistent with the UART specification (v1.5 and v1.7). **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhI22423	**Module Affected:** UART **Title:** UART does not send one stop bit when configured to send break before TXDC **Release Date:** 2/13/2006	**Description:** In the UART, the send break is enabled during the transmission of the first character. According to the specification, the current character must be transmitted and only then a break should be sent until the send break bit is cleared. This does not occur if breaks are sent after the TXDC bit is set. **Workaround:** Send break only after TXDC bit is set. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhI19968	**Module Affected:** ARM Platform **Title:** AIPS unaligned accesses to 16-bit peripheral **Release Date:** 2/13/2006	**Description:** Unaligned halfword and byte accesses to 16-bit peripherals are not terminated with an error response as stated in the specification, section 4.5. An IP transaction is initiated and incorrect behavior of the IP bus strobes (incorrect strobes assert) may occur. **Workaround:** Software must not attempt unaligned halfword and byte accesses because these accesses are not supported. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
DSPhI19969	**Module Affected:** ARM Platform **Title:** AIPS Unaligned (Without Byte Strobes) Accesses to 8-bit Peripheral **Release Date:** 2/13/2006	**Description:** If an unaligned byte accesses (without byte strobes) occurs for 8-bit peripherals a transaction is initiated. The AHB access is not terminated with an error response. It is not clear if the ARM11™ (or any other bus master) can generate this type of access. **Workaround:** Software must not attempt unaligned byte accesses because these accesses are not supported. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhI20940	**Module Affected:** ARM Platform **Title:** Status Register in ROMPatch **Release Date:** 2/13/2006	**Description:** The status register (ROMPatchSR) in the ROMPatch module always reads zero. The read enable logic is incorrect. **Workaround:** Do not use the ROMPatch Status Register. Use the ETM trace function instead, however, typically this register is not used often. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhI24192	**Module Affected:** ARM Platform **Title:** Non-Word Writes to EVTMON **Release Date:** 2/13/2006	**Description:** Non-word size writes to EVTMON registers can affect the contents of the registers even though they are properly flagged as a bus error. **Workaround:** Only use word writes to the EVTMON registers. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
DSPhI19594	**Module Affected:** ARM Platform **Title:** L2CC Error on All bits of a Burst **Release Date:** 2/13/2006	**Description:** At present, the Level 2 Cache only recognizes errors on the last beat of a burst. Errors on earlier beats are ignored. Note that while this is not ideal for memory spaces or undefined spaces, entire rows are defined the same way. There will either be all good accesses or all error accesses when a burst occurs. This cannot be assumed for peripheral spaces, but those are typically not cached. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo65953	**Module Affected:** ARM Platform **Title:** FIQ or IRQ behavior causing aberrant behavior on ARM1136 core when exiting WFI mode resulting in cache corruption **Release Date:** 2/13/2006	**Description:** The behavior of the FIQ signal to the ARM11 core has been shown to cause a problem when exiting WFI mode. The FIQ signal will toggle after being initially asserted, which is unexpected behavior to the ARM11 core. This particular behavior occurs when core clocks continue to run and, along with particular caching and alignment schemes, can result in a corrupted cache line following a prefetch, and thus unexpected behavior in code. It was also discovered that the core could execute an instruction immediately following the WFI instruction before servicing the FIQ. This errata supersedes and replaces the errata previously reported as TLSbo64855. **Workaround:** There are two work arounds for this issue. The first is recommended when using DVFS load tracking hardware while the second may be used if DVFS load tracking hardware is not used. ***Work Around 1:*** The first work around requires locating the WFI code in a non-cacheable region. The sequence is as follows: • Make the WFI a non-cacheable sub-routine to eliminate interaction of the WFI and the L1 Instruction cache. • Disable and invalidate the L1 and branch target caches in WFI routine, prior to executing WFI instruction. • Add 7 NOPs after WFI command (this is only needed in cases where interrupts are enabled upon executing WFI). • Re-enable L1 caches *Continued on next page*	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	

TLSbo65953 *Continued*	**Module Affected:** ARM Platform
	Title: FIQ or IRQ behavior causing aberrant behavior on ARM1136 core when exiting WFI mode resulting in cache corruption
	Release Date: 2/13/2006
		The word around software sequence is shown below:
		mrc p15, 0, r0, c1, c0, 0 ; Read system control reg
		bic r0, r0, #ARM_CTRL_ICACHE ; Disable I-cache
		bic r0, r0, #ARM_CTRL_DCACHE ; Disable D-cache
		mcr p15, 0, r0, c1, c0, 0 ; Update system control reg
		mov r0, #0 ; Invalidate entire I-cache (also
		mcr p15, 0, r0, c7, c5, 0 ; flushes branch target cache)
		mov r0, #0 ; Clean and invalidate entire
		mcr p15, 0, r0, c7, c14, 0 ; D-cache
		mov r0, #0
		mcr p15, 0, r0, c7, c0, 4 ; Enter WFI
		<< NOP instructions may be added here if interrupts are enabled prior to entering WFI.
		The NOP instructions are used to prevent premature execution of the instruction following the WFI. >>
		mrc p15, 0, r0, c1, c0, 0 ; Read system control reg
		orr r0, r0, #ARM_CTRL_ICACHE ; Enable I-cache
		orr r0, r0, #ARM_CTRL_DCACHE ; Enable D-cache
		mcr p15, 0, r0, c1, c0, 0 ; Update system control reg
		Continued on next page
			Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	

TLSbo65953
Continued
	Module Affected:
	ARM Platform
		Work Around 2:
		The second work around is recommend for systems not using DVFS load tracking hardware. In this work around, the WFI routine must change the clocking mode to 1:1 (ARM:AHB) ratio.
		After writing to the post-divider register, enough delay must be introduced to ensure that 1:1 mode has been achieved, which can be done by performing a series of “dummy” reads. To determine the delay needed (the number of dummy reads to be performed), one must look at the divide ratios (from HCLK) in the PODFs (post dividers) and then find the LCM (Least Common Multiple) of these to arrive at the worst-case time for the posedges of the clocks to line up. This is required for the CCM to complete the switch to 1:1 mode. After finding the LCM, convert that to IPG cycles based on the IPG divide ratio (generally the IPG bus clock is one-half HCLK). Once the number of IPG cycles have been calculated, add 1 to that number to get the number of reads required to the IP bus (CCM).
		For example, if the CCM HCLK post dividers have divide ratios of 1, 2, and 7, then the LCM is 14 HCLKs. This equals 7 IPG clocks. Thus, 8 reads are required before entering WFI.
		On wakeup, the clocks can then be changed back to the original ratio.
		This completely prevents the toggle on the interrupt line, and this code can now be located in a cacheable region.
		EXAMPLE:
		mov r0, #0
		ldr r1, =<clock_control_BASE>
		ldr r2, [r1, #OFFSET]
		orr r3, r2, #1TO1MODE
		str r3, [r1, #OFFSET]
		..... // delay while switch to 1:1 occurs
		// In the example stated above, 8 reads are needed
		ldr r3, [r1, #OFFSET] //dummy read 1
		ldr r3, [r1, #OFFSET] //dummy read 2
		...
		ldr r3, [r1, #OFFSET] //dummy read 8
		mcr p15, 0, r0, c7, c0, 4 //WFI
		str r2, [r1, #OFFSET]
		bx lr
		Fix Plan/Status:
		Not Fixed
			Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo51015	**Module Affected:** ATA **Title:** Access to drive register when ATA is in reset state hangs the bus **Release Date:** 2/13/2006	**Description:** When ATA is in reset, reads and writes to the ATA drive registers causes the bus to hang. This has no impact on properly written code. **Workaround:** Not needed—use module properly—that is, never attempt Drive when interface is in reset. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo52620	**Module Affected:** SSI **Title:** SSI AC97 variable mode bug **Release Date:** 2/13/2006	**Description:** According to AC97 protocol, the AC97 controller (SSI) sends data based on the SLOTREQ bits. When the CODEC sends 0 in SLOTREQ bits, it can mean that the CODEC is requesting data or that a particular channel is powered-down/unimplemented. Within SSI, if SSI receives 0 in SLOTREQ, it means that the CODEC is requesting data; 1 implies that the CODEC does not require data for that slot. Therefore, the SSI has no ability to identify whether the channel is powered down. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
MSIls19391	**Module Affected:** CCM/DVFS **Title:** Some DVFS load tracking signals cannot be sampled with div_3_clk **Release Date:** 2/13/2006	**Description:** The load tracking signals of DVFS are intended to stay asserted longer than div_3_clk; however, several signals cannot be used properly for load tracking. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo54572	**Module Affected:** EMI **Title:** Running code that uses SDRAM (16-bit) with data cache off causes the system to hang **Release Date:** 2/13/2006	**Description:** Running Redboot and turning off the data caches causes the system to hang. The RVD or IcePick are unable to communicate to the ARM core. The system must go through reset to recover. This erratum does not apply to DDR. **Workaround:** Programming the SDRAM and SDRAM Controller to Full page mode corrects this behavior. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo61195	**Module Affected:** IPU **Title:** Cursor gets corrupted before reaching the end of the visible screen buffer. **Release Date:** 2/13/2006	**Description:** The IPU cursor gets corrupted before reaching the end of the visible screen buffer. After that, increasing the column number causes the cursor to cover the entire width of the display. The desired behavior is to be able to move the cursor to the edge of the screen (up to coordinate 240 without any issues.) There are no issues with the cursor blinking or cursor size options. **Workaround:** SW workaround exists. The latest specification includes clarification for correct IPU programming. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo50929	**Module Affected:** EMI/DDR, DVFS **Title:** Limited support for DVFS functionality in a system using DDR memories **Release Date:** 2/13/2006	**Description:** *Two problems exist:* 1. The DVFS function within a system with DDR memory is limited to the same AHB frequency—that is, the external memory interface frequency is the same across all DVFS voltage and frequency points. A DVFS frequency change between frequency and voltage points is not supported because DDR memory does not allow a frequency change during the middle of a transaction. 2. The ESDCTL (SDRAM Controller) delay line measurement unit is not robust enough to handle changes in core voltage (QVCC), which is needed for DVFS functionality. **Workaround:** For problem 1, in all revisions of silicon, the AHB frequency must be maintained when using DDR memory. However, SDR SDRAM memory is not affected by this limitation. For problem 2, a fix will be made for Rev2.0 silicon to allow changing the core voltage (QVCC) without adverse affects to the DDR operation. For silicon revisions 1.2 and below, this errata does not affect SDR SDRAM memories. **Fix Plan/Status:** Changing core voltage (QVCC) while using DDR: Fixed in silicon Rev. 2.0	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo61214	**Module Affected:** SSI **Title:** Defect in I^2S slave mode, causing left/right channel switches **Release Date:** 2/13/2006	**Description:** A defect in I^2S slave mode causes the left and right channels to switch randomly. The SSI begins transmitting and receiving data in I^2S slave mode (async/sync) on the posedge of the frame sync instead of waiting for the negedge of the frame sync when the posedge of the frame sync is encountered first. This scenario occurs when tx_en/rx_en of SSI in the SCR register is disabled in between the frame and enabled after the frame is completed. All other register settings of SSI remain unchanged. **Workaround:** SW Workaround exists. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo61142	**Module Affected:** CCM/Low Power Mode **Title:** GPIO1_5 pin used as both Power Management IC (PMIC) interrupt and POWERRDY inputs, but must be driven 1 in exit from DSM/SR modes **Release Date:** 2/13/2006	**Description:** Although not explicitly indicated within the specification, GPIO1_5 is a dedicated pad for handshaking with the Power Management IC (PMIC) to exit from State Retention (SR) and Deep Sleep Mode (DSM). CCM input ipp_pmic_int, which is driven by GPIO1_5 pin, must be 1 on exit from SR/DSM modes. This means that the pad must be in its functional mode and not in an alternate GPIO mode. Otherwise, the core will not recover from SR/DSM low-power modes and hang. This is caused by a default value of pmic_int when the non-functional mode is 0. **Workaround:** APP board design and SW must guarantee the following: • GPIO1_5 is in its functional muxing mode when entering LPM mode. • GPIO1_5 is driven to 1 when the core exits LPM mode. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo72155	**Module Affected:** ESDCTL: SDR only **Title:** SDR SDRAM exit self refresh timing is too short for some devices requiring tRC + 1. **Release Date:** 9/7/2006	**Description:** When using external SDR SDRAM with tSREX (also called tXSR, and means self refresh exit to next valid command delay) of more then tRC + 1, the controller may issue auto refresh after exiting manual self refresh too soon, and that may result in errors. The setting of tSREX is not direct, but derived from the tRC value. Relation is as follows: tSREX = (tRC reg value + 1) × Tcycle (AHB cycle time). In timing, tSREX = tRC + 7.5 ns (for 133 MHz AHB frequency). tRC (Active to Active timing) if set to higher number than minimal value supported by the memory, will have negligible impact on the performance. This does not affect DDR operation. For DDR, tXSR is hard-wired to 27 clock cycles. At 133 MHz, this yields 7.5ns × 27 = 202.5 ns. **Workaround:** Set tRC to max possible, to meet tSREX timing (Max yields 157.5 ns value). This implies tRC = 150 ns. Any memories, which support lower tRC value, the impact to performance is negligible. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo74193	**Module Affected:** EMI: WEIM and NFC **Title:** WEIM and NAND Flash Controller bus sharing may stall if WEIM access starts at the beginning of a NAND Flash Read **Release Date:** 9/7/2006	**Description:** The WEIM and the NAND Flash controller have a special handshake logic that allows them to share the data bus. This logic can stall, prohibiting both of them from using the data bus, if the WEIM access starts at a particular state of the NAND Flash Controller Read State machine. **Impact:** The bus stall may lead to a core hang requiring a chip reset to recover. **Workaround:** Do not use WEIM and NAND Flash accesses at the same time. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo72918	**Module Affected:** ESDCTL: SDR **Title:** Cannot use SDR on both chip selects. **Release Date:** 9/7/2006	**Description:** An issue with internal logic causes both CKE0 and CKE1 to go low even though only one chip-select is being accessed. The result is that the SDR SDRAM on the alternate chip-select views CKE as going low which may be mistaken for a power-down operation, therefore the timing for the power-down may not be met (especially as this power-down operation is unintentional). Hence, the chip-selects (CSD0 and CSD1) cannot be used together for SDR memories. This errata does not affect DDR memories. **Workaround:** None **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo72912	**Module Affected:** Watchdog **Title:** Watchdog (WDOG) timer resets pre-maturely during low power mode. **Release Date:** 9/7/2006	**Description:** After any service sequence of the WDOG Timeout Field (in the Watchdog Control Register, see Reference Manual), it requires two CKIL clocks to reload the WDOG Counter. If the WDZST bit is set (which suspends the WDOG Timer in low power mode) and the system enters low power mode before these two CKIL clocks, the service request is lost. **Workaround:** S/W must ensure that after the WDOG service request, it does not enter low power mode for at least 2 CKIL periods (~61 us). **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo72605	**Module Affected:** WEIM **Title:** WEIM cannot operate with WEIM BCLK equal to AHB clock. **Release Date:** 9/7/2006	**Description:** When enabling the SYNC bit of the WEIM, the burst clock (BCLK) frequency cannot be equal to the AHB (system) clock. This means that for a maximum AHB frequency of 133 MHz, BCLK can be no greater than 66 MHz. **Workaround:** When enabling the synchronous interface of the WEIM, the Burst Clock Divider (BCD) bits must be set to one (divide-by-2) or greater. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo71120	**Module Affected:** EPIT **Title:** The EPIT Counter may not be updated if the EPITLR is written to multiple times. **Release Date:** 9/7/2006	**Description:** When IOVW = 1 and there are multiple writes of differing values to the EPIT Load Register (EPITLR) within one EPIT counter clock and the last write is 1 ipg_clk before the next rising edge of the counter clock, the last write will not update the EPIT Counter Register (EPITCNT), however, the EPITLR will be loaded with the correct value. This means that the counter will not start counting down from the last value written to the EPITLR. **Workaround:** There are two software work arounds for this bug: 1. Write to the EPITLR with the desired value twice. This ensures that the counter will be updated with the desired value programmed into the EPITLR. 2. For two consecutive (differing) writes to the EPITLR, ensure that the second write is performed at least one counter clock after the first write. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo71157	**Module Affected:** IIM **Title:** Fusebox Digital Race condition causing the IIM busy status bit to lock. **Release Date:** 9/7/2006	**Description:** A race condition exists in the Fusebox Digital module causing a lock of the IIM busy status bit which prevents further fusing operations unless a reset is performed. **Workaround:** S/W must introduce a delay of at least one CKIL clock cycle (~31 us) between consecutive fuse programming operations. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo67266	**Module Affected:** IPU **Title:** R/W signal error for byte enable accesses for asynchronous 68K mode. **Release Date:** 9/7/2006	**Description:** A read/write signal error occurs when the interface type is async sys68k type 1 or type 2 and a read of the upper byte is performed in byte enable mode. When the IPU is setup in this mode, R/W (IPU_WR) should indicate the correct state for both lower and upper byte accesses, however, the observed function is that IPU_WR (R/W) does not indicate correct level for upper byte accesses. No problem occurs for any operations with the sys80 interface, for writing the upper and lower bytes with the sys68k interface, or for reading the full word or the lower byte with the sys68k interface. **Workaround:** There are three possible workarounds for the problem: 1. Use the sys80 interface. No SW limitations are required. 2. If the sys68k interface is used, perform only full 16-bit reads (SW limitation). The desired byte can be extracted from a word by SW. 3. For the sys68k interface, perform ORing of two IPU outputs: DISPB_WR and DISPB_DATA[16]. The OR output should be used as read/write control in sys68k mode with byte enable. This new signal should be used instead of DISPB_WR for this interface. The ORing can be performed on the board or inside the GPU (if possible). The OR function corresponds to the case when the DISPB_WR polarity is 1 for read. No SW limitations are required for this HW workaround. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSb063573	**Module Affected:** SIM **Title:** Glitch on Reset of ICM register in the SIM module. **Release Date:** 9/7/2006	**Description:** The ICM register in the SIM module contains Reset and Set signals. The Set signal connects to system reset and the reset value of the register should be “1”. At the Gate-Level when de-asserting the Set signal, a glitch on the Reset is created, because of the race condition in reset logic. This causes the reset value of the ICM register to be “0” instead of “1” as stated in the specification. **Workaround:** SW Workaround Available: The software should not rely on the reset value of this bit, but instead, write the desired value during initialization. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo55829	**Module Affected:** GPT **Title:** Missing CKIH source to GPT. **Release Date:** 9/7/2006	**Description:** The CKIH source in not available as a source to the GPT. This means that selecting “011” for the clock source bits in the GPT Control Register is not allowed. **Workaround:** Do not use CKIH (setting of “011” for the clock source select) as source clock for the GPT. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo78667	**Module Affected:** SDHC **Title:** SDHC Multiple-Block Write issues. **Release Date:** 9/7/2006	**Description:** During a multi-block write, when the STOP_TRANSMISSION command (CMD12) is sent, the SDHC does not have a hardware mechanism to wait until the card busy signaling period is over to determine if it is safe to send the next write command. As a work around, the SDHC software driver should configure the IOMUX to switch the SDHC DAT0 IO pin as a GPIO input. In the case of SHDC1, SD1_DAT0 is multiplexed with a GPIO, however, SD2_DAT0 (SDHC2) does not have a GPIO multiplexed with SD2_DAT0. **Workaround:** As SD2_DAT0 does not have a GPIO multiplexed on the same IO, it is recommended that after each multi-block write command (CMD25+CMD12) SW continuously sends CMD13 to read the card status register to determine whether the card busy period is over. This adds overhead to the driver affecting write performance. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo81932	**Module Affected:** ESD **Title:** MX31 M45G Absolute Maximum Human Body Model (HBM) ESD is 1.5 KV. **Release Date:** 10/30/2006	**Description:** M45G and M91E mask set does not meet the 2 KV Human Body Model (HBM) ESD and was qualified at 1.5 KV. Other mask sets meet the 2 KV HBM ESD. **Workaround:** None **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo82066	**Module Affected:** ARM Platform **Title:** Masking FIQ in the CPU **Release Date:** 11/8/2006	**Description:** The interrupt controller design is such that, whenever FIQ is asserted, the IRQ signal is forced negated. If FIQ is masked inside the CPU (via the CPSR), this can cause the following issues: 1) FIQ can be asserted, but not recognized by the CPU. This forces IRQ to remain negated, so the CPU can never recognize or service the IRQ. 2) IRQ could be asserted, then randomly negated at the moment a masked FIQ is asserted. This could result in unpredictable behavior by the CPU. **Workaround:** Never mask FIQ (inside the CPU via the CPSR) unless IRQ is also masked. If this functionality is needed, FIQ can be masked in the interrupt controller via the FIDIS bit in the INTCNTL register. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo81670	**Module Affected:** IPU **Title:** Hanging IPU slave AHB bus for MCU direct access to different chip selects **Release Date:** 1/4/2007	**Description:** For certain applications using an external graphics processing unit (GPU), the MCU should directly access an external GPU via the IPU slave AHB interface using different IPU chip select outputs (display numbers). If the MCU reads from and writes to the different IPU chip selects in interleaved manner, the IPU slave AHB may hang on read operation. Hanging occurs when two chip selects are accessed in different directions (for example, the first one for write and the second one for read) and an address for the first chip select is sequentially incemented after switching. An example scenario follows: 1. Write to CS0. The last address of the write is “A” (byte resolution). 2. Switch to read from CS1. 3. Switch back to write to CS0. The first write address after switching is “A+2”. The root of the problem is that the write template is not involved after switching at step #3 because the addresses are sequential. The IPU’s ADC state machine expects that each change of access direction will involve the template. Because this does not occur, the IPU hangs. **Workaround:** A possible SW workaround is to force template execution before step #3. This can be done by performing dummy read from CS0 before resuming writes from CS0. A dummy read address must be different from the first write address. It is recommended that the dummy read use a large address offset in the GPU memory to guarantee this condition. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo84378	**Module Affected:** EMI and Internal RAM **Title:** Internal RAM and EMI access issue **Release Date:** 1/4/2007	**Description:** Symptom: The EMI (External Memory Interface, specifically the ESDRAM Controller) may occasionally miss an access depending on the MMU configuration. This occurs when there is an internal *slave switch* on the L2CC bus during the SDRAM auto *refresh cycle*. **Reasons:** *Two EMI specific reasons:* 1. The EMI assumes it is the only slave on the bus and hence does not use the internal *hready_in* signal from the ARM core. 2. No decoding of the incoming address occurs in the EMI when deciding to deactivate the internal hready_out signal. So each access reflected on the internal AHB bus will cause EMI to think it is being accessed. *One architectural reason:* • The ARM busses to EMI are L2CC0 and L2CC2, which reflect any access on other ARM AHB busses which were not configured as Not Shared in MMU. *Continued on next page*	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo84378 *Continued*	**Module Affected:** EMI and Internal RAM **Title:** Internal RAM and EMI access issue **Release Date:** 1/4/2007	**Scenario:** The problem occurs when there is a Slave Switch on the L2CC (L2 Cache Controller) bus between internal RAM and the EMI, where the EMI cannot service the access due to a *Refresh Cycle* occurring to the external SDRAM memory. The first access to the internal RAM makes the EMI deactivate its internal hready_out signal. Then, the second access is completely ignored by EMI, although it is a legal access. **Note:** Because the internal ROM cannot be mapped to the P-AHB (due to the fact that code is executed from ROM), any accesses to ROM (when not in boot sequence), must take special precautions to avoid the failure conditions. **Impact:** An external access may be missed (may not occur) following an access to the internal RAM. **Workaround:** A work around in software exists, such that accesses to the internal RAM should be made via the “P-AHB” bus from the ARM core as defined in the MMU set up. This can be accomplished by setting up the internal RAM region as a non-shard device in the MMU page table (via the type extension field bits, TEX[2:0], C bit and B bit as defined in the ARM11 page table format). However, a restriction occurs as the ARM core cannot execute code via the P-AHB bus. This work around is applicable given the code is being executed from the external SDRAM (or internal cache) and data is stored and accessed in the internal RAM. Code cannot be executed from both internal RAM and external SDRAM. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo84397	**Module Affected:** Bootstrap ROM **Title:** CPU hangs if BOOT[4:0] set to 00000 (bootstrap) and a USB ULPI is not present. **Release Date:** 1/4/2007	**Description:** When setting boot mode BOOT[4:0] to 00000 (bootstrap mode), and a ULPI transceiver is not present or is disabled at reset, the CPU will hang. This is because the USB module requires an external clock from the external ULPI transceiver during bootstrap mode. **Workaround:** Three work arounds exist to avoid this issue during bootstrap mode (BOOT[4:0] = 00000): 1. If using a board design with a ULPI transceiver, enable the transceiver at power on. 2. If using a board design without a ULPI transceiver, connect a clock to the USB_OTG pin. This can be a low frequency clock (for example, same clock source as CKIL). The clock source to this pin can be turned off later. 3. For debug purposes only, use boot mode BOOT[4:0] 00110 (but can only perform bootstrap through UART or USB Full speed interface). Note, the MX31 ADS board has two possible serial full speed transceivers, the ISP1301BS and the MC13783, but only the ISP1301BS works in BOOT[4:0] 00110 mode. In BOOT[4:0] 00000 mode, both the IPS1301BS and the MC13783 serial transceivers work, however, one of the previous two work arounds should be used. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo88060	**Module Affected:** EMI: ESDCTL **Title:** Software reset in ESDCTL causes loss of information on the external memory's precharge status **Release Date:** 1/18/2007	**Description:** When issuing a software reset in the ESDCTL via the RST bit in the ESDMISC register, the logic that stores the precharge status of the external memory's banks is reset. Thus, if a bank in the external memory was closed at the time this soft reset is initiated, the ESDCTL incorrectly assumes this bank is open and issues a read or write command when instead, it should first issue an active command. However, in normal use cases, soft reset of the ESDCTL is not necessary. **Workaround:** None **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo88353	**Module Affected:** SIM **Title:** SIM RCV_EN bit must be set (SIM receiver enabled) for the SIM transmitter (enabled via the XMT_EN bit) to work properly **Release Date:** 1/18/2007	**Description:** It is found that for the SIM transmit logic to function properly, the SIM receive must be enabled (via the RCV_EN bit in the SIM's ENABLE register). **Workaround:** The SIM receiver must be enabled (via the RCV_EN bit) before enabling the SIM transmitter (enabled via the XMT_EN bit). **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo91748	**Module Affected:** SDHC (SDIO Controller) **Title:** SDHC multi-block write problem to SDIO cards that do not send a busy signal between each block in a multi-block write **Release Date:** 2/26/2007	**Description:** When the SDHC writes multi-block data to an SDIO card, it will monitor the busy signal (low value of DAT0 driving by the SDIO card) from the card after each block of data is sent to the card. The SDHC will then wait until the card is ready for the SDHC to write the next block of data. No other data transfer operations are affected. **Impact:** If no busy signal is detected after the multi-block write, the SDHC will stall waiting for the busy signal causing the write operation to timeout and a failure to proceed with the next write operation. Therefore, the SDHC can only support cards that provide a busy signal between each block in a multi-block write. **Workaround:** As a workaround, multi-block write can be replaced by single-block write, however this will degrade the efficiency of the data transfer. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo91750	**Module Affected:** IOQVDD Voltage Rail **Title:** Power up sequence causes a slight current drain increase on IOQVDD rail **Release Date:** 8/27/2007	**Description:** This only applies to M91E. The defined power up sequence results in a slight increase in current drain (3 to 5 mA) when IOQVDD is raised prior to the NVCC2, NVCC21, and NVCC22 (NVCC2x) rails, specifically NVCC21. The current drain increase is observed during the time IOQVDD is raised prior to NVCC21 being raised. Once NVCC21 is raised to its appropriate voltage, the extra current drain disappears. However, this drain neither poses a risk to the silicon nor causes any damages. Therefore, this is technically not an errata, but it is documented here to inform the user of this scenario. **Workaround:** Since the slight current drain does not pose a risk to the silicon, no work around is necessary. However, another power up sequencing option is available (please refer to the *MCIMX31 and MCIMX31L Multimedia Applications Processor Data Sheet*), which allows the user to power the NVCC2x rails with IOQVDD, NVCC1, and NVCC3-10, in which case, no current increase will occur. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo86232	**Module Affected:** SDMA **Title:** SDMA causes wrong accesses when running CH0 a second time **Release Date:** 8/27/2007	**Description:** When the SDMA Channel 0 (CH0) is ran a second time with Dynamic Context Switching mode, it can generate invalid accesses on the BurstDMA port. In most applications, SDMA CH0 is run a second time only when downloading RAM scripts from external memory into the SDMA RAM. No issue is seen when running the SDMA CH0 for the first, initial time. **Workaround:** Since the issue is mainly seen when downloading RAM scripts into the SDMA RAM, it is recommended to use Static Context Switching for CH0 during the script download. When the download process is completed, the user may switch back to Dynamic Context Switching mode. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo94952	**Module Affected:** IPU **Title:** LCD clock temporarily stops while performing DVFS PLL switching **Release Date:** 8/27/2007	**Description:** When performing a DVFS PLL switch, flicker is seen on the LCD display for about 200 µs, which is proportional to the VSCNT value in the CCM module. The flicker occurs due to the DVFS handshake with the IPU. Specifically, when the CCM sends an internal clock rate change request to the IPU, the IPU stops the pixel clock to the display until the VSCNT time has expired. This problem is not seen when using a smart (asynchronous) display. Note that this only applies to mask set M91E since previous versions did not support DVFS PLL switching. **Workaround:** Performing a DVFS switch from one PLL to another should be performed in two stages: 1. Perform voltage change by software through programming the power management IC (PMIC) via SPI or I2C for example. 2. Once the voltage has changed (after counting the appropriate CKIL cycles), perform the DVFS operation through CCM but without changing the voltage (so this will actually perform a DFS stage only). This can be done by programming the dvs0/1 of CCM to match the new value programmed by software in the first stage (the voltage change only stage), and to set VSCNT to a low number (even 0), so that the state machine will not wait for PMIC to change voltage (PMIC is already at the aimed voltage in this stage). **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo93426	**Module Affected:** Bootstrap ROM **Title:** USB is not recognized by the PC during bootstrap mode **Release Date:** 8/27/2007	**Description:** When configuring the BootMode[4:0] pins for bootstrap mode, the bootstrap ROM configures the USB and UART modules for serial download. However, deficiencies in the bootstrap ROM code result in unreliable USB connectivity with the PC such that the PC reports that it does not recognize the USB device. Note that this is not a problem with the USB module, just the implementation in the bootstrap ROM. **Workaround:** Use the UART port for serial communication during bootstrap mode. **Fix Plan/Status:** Not Fixed	Rev. 2.0	—

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
TLSbo93469	**Module Affected:** SDHC **Title:** Buffer corruption can occur when SW enables the SDHC clock for a read **Release Date:** 8/27/2007	**Description:** When the SDHC bus clock is stopped by SW, on writing a read command to the CMD_DAT_CONT register, the clock will be re-activated by the SDHC module itself. If the SW starts the clock, as it does in legacy drivers, the clock will be forced active, corrupting the data buffer. **Workaround:** The SW driver should not manually re-start the SDHC clock during reads as the SDHC module re-activates this clock automatically **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo86219	**Module Affected:** IPU **Title:** IPU restriction on HSP=AHB clock when accessing an external GPU **Release Date:** 8/27/2007	**Description:** Internal synchronization issues in the IPU limits accesses to an external graphics processor (GPU) such that the maximum HSP clock frequency is the frequency of the AHB clock. In other words, the HSP clock cannot be set higher than the AHB clock when using an external GPU. This applies to the IPU version used in mask set M91E only. **Workaround:** None **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo95266	**Module Affected:** UART **Title:** UART module asserts TRDY interrupt even if the transmitter is disabled **Release Date:** 8/27/2007	**Description:** The UART transmitter ready interrupt (TRDY) will generate an interrupt when TRDYEN (transmitter ready interrupt enable) is set, even though the transmitter is disabled (TXEN=0). **Workaround:** Enable the interrupt after enabling the transmitter in software. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
TLSbo96321	**Module Affected:** IPU **Title:** When using the 3-clock-cycle-per-pixel mode, the first pixel in a line presents incorrectly **Release Date:** 10/05/2007	**Description:** When using a 3-clock-cycle-per-pixel synchronous LCD panel, a problem occurs where the first pixel of each line does not sample correctly; therefore, incorrect data is sent out to the display. This incorrect data is the last pixel of the previous line. **Workaround:** None. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
ENGcm02610	**Module Affected:** USB OTG **Title:** Data corruption occurs in the USB OTG module at low core voltage **Release Date:** 01/11/2008	**Description:** At low core voltages, the USB OTG core will transfer corrupted data (single bit errors) in both Host and Device mode, without being caught by the CRC, as the data corruption occurs inside core by which the CRC is calculated on that erroneous data. Preliminary testing shows that this problem occurs at core voltages < 1.38 V. The problem was identified to be an issue with the internal memory of the USB OTG core. **Workaround:** There are two work around solutions: 1. During USB OTG transfers, elevate the core voltage greater than Vmin (preliminary testing shows this to be 1.38V, however more thorough testing and characterization is being performed). 2. Use an alternate Host core (if not needing the OTG functionality). **Fix Plan/Status:** Not fixed.	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
ENGcm11424	**Module Affected:** WEIM **Title:** WEIM can not correctly sample data **Release Date:** 07/2010	**Description:** The active-low input signal End Current Burst (ECB) is asserted by external burst capable devices. It is serviced in synchronous mode only (SYNC=1).This signal can be used in two different modes depending on the EW bit in the Chip Select Control Register. In the ECB mode (EW=0), ECB indicates the end of the current (continuous) burst sequence. Following assertion, the WEIM terminates the current burst sequence and initiates a new one. In the WAIT mode (EW=1), the memory device asserts this signal to insert wait states during refresh collisions or during a row boundary crossing. Following assertion, the WEIM does not terminate the current burst sequence and continues it once WAIT is negated. FCE is one parameter in the register CSCRxA that is used to enable/disable feedback clock. • If FCE=0, WEIM will sample the data by internal AHB bus clock. • If FCE=1, WEIM will sample the data by BCLK_FB singal that is from PAD. The issue is found that, if FCE is configued to 1 and there is ECB assertion during access, WEIM will not sample the correct data. **Workaround:** Use FCE=0 mode instead of FCE=1 mode, if external device will assert ECB_B singal during burst access in FCE=1 mode. **Fix Plan/Status:** Not fixed.	Rev. 2.0	Rev. 2.0.1

Table 2. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
ENGcm09282	**Module Affected:** IPU **Title:** Cannot receive IPU ACK if CSI is still working when the OS goes into low power mode **Release Date:** 12/2012	**Description:** For the data flow [input_data—>camera interface (CSI)—>pre-processor (PRP)—>LCD], when the OS goes into suspend mode (low-power mode), IPU handshakes with the CCM to acknowledge a stop request if the IPU source clock HSP_CLK is not disabled (CCM CGR1 register CG9[19:18] does not equal 2'b00/2'b01/2'b10). When the CSI is busy dealing with data from a sensor, the IPU does not send an ACK back, and this causes an IPU handshake failure and low-power mode failure. Only after detecting CSI_EOF, which indicates that the CSI has finished processing the current frame and is not busy at this moment, the IPU can successfully send an ACK to CCM and low-power mode can work. Projected Impact: This increases power consumption. **Workaround:** Before going into low-power mode, disable the IPU source clock (HSP_CLK) by configuring CG9[19:18] to 2'b01 or 2'b10 in the CCM CGR1 register, so the IPU does not do the handshake. This enables the OS to successfully enter low-power mode. **Fix Plan/Status:** No fix scheduled.		

2 USB2 Host Controller Errata

Table 3 lists the errata for the USB host controller by TDI (formerly ARC) partners with ChipIdea.

Table 3. Chip Errata for the USB2 Host Controller of i.MX31

Errata ID	Summary	Details	Mask Rev.	
Nashua CR571	**Module Affected:** USB2.0 **Title:** Incorrect write enables are used for bytes 2 and 3 write accesses to the ULPI Viewport register **Release Date:** 2/13/2006	**Description:** The incorrect write enables are used for bytes 2 and 3 write accesses to the ULPI Viewport register. This problem does not occur with 32-bit accesses. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR574	**Module Affected:** USB2.0 **Title:** When device disconnects in full-speed, the xcvr_select transitions through HS **Release Date:** 2/13/2006	**Description:** In Host mode when the device disconnects during full speed, the xcvr_select transitions through high speed. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR583	**Module Affected:** USB2.0 **Title:** Data pulsing lasts for 8 ms when SRP is enabled regardless of the state of the bus **Release Date:** 2/13/2006	**Description:** When the SRP accelerator is enabled, data pulsing lasts for 8 ms regardless of the state of the bus, as opposed to ceasing when the core detects that a_vbus_vld is asserted. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR584	**Module Affected:** USB2.0 **Title:** Host missing interrupt on a resume after suspend **Release Date:** 2/13/2006	**Description:** The host does not detect an interrupt on a resume after suspend, and the port-change-control interrupt does not go active, and no port-change-toggle occurs. **Workaround:** Software: Monitor the SOFs. If SOFs are generated then the port is resumed. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 3. Chip Errata for the USB2 Host Controller of i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
Nashua CR585	**Module Affected:** USB2.0 **Title:** Disconnect bit is not visible, when host is running in Test_Force_Enable mode **Release Date:** 2/13/2006	**Description:** When host is running in Test_Force_Enable mode, the disconnect bit is not visible. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR591	**Module Affected:** USB2.0 **Title:** Core sends packet traffic (SOF's) when in TEST_MODE_SE0 **Release Date:** 2/13/2006	**Description:** The host UTMI+ core sends packet traffic (SOF's) when in TEST_MODE_SE0. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR609	**Module Affected:** USB2.0 **Title:** The host core sends an extra byte of data after the Keep Alive for directly attached low speed devices **Release Date:** 2/13/2006	**Description:** The host core sends an extra byte of data after the Keep Alive for directly attached low speed devices. **Impact:** Does not cause any interoperability problems. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 3. Chip Errata for the USB2 Host Controller of i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
Nashua CR590	**Module Affected:** USB2.0 **Title:** The ULPI TX state machine locks-up if the peripheral disconnects immediately prior to a packet transmit **Release Date:** 2/13/2006	**Description:** Host, FS/LS Only: The ULPI TX state machine lock-ups when the peripheral disconnects immediately prior to a packet transmit. The ULPI sends an RXCMD to indicate that there is an SE0 on line state instead of an ACK as the target did not respond. The core must wait 2.5 ms to ensure that this is really a disconnect before recognizing it as such. Meanwhile, the transmit state machine re-tries the previous transaction—that is, the combination of the events where the SE0 was registered and the first transition on the bus caused an erroneous EOP to be detected and the transmit state machine locked up. The core issues the port change detect interrupt which shows that a disconnect has occurred, however, there is no indication that the ULPI transmit state machine is locked up. **Impact:** Critical, must use SW workaround. **Workaround:** Software: Reset the core in SPH and OTG after an FS peripheral disconnect, in an MPH wait until the transfers on all other ports has completed, then reset the core. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR597	**Module Affected:** USB2.0 **Title:** A pre-empted tx packet causes the ulpi_tx state-machine to lock-up **Release Date:** 2/13/2006	**Description:** A pre-empted tx packet causes the ulpi_tx state machine to lock-up. In this context tx means that the process of putting the data out onto the bus is in progress, not that a packet is queued for later transmission. If working as host, the USB will not begin transmitting the next packet until the results of the previously received packet are known. It is possible, however, that a malfunctioning device is transmitting. If working as a device, the USB will only begin to transmit in response to a receive packet (a host must never send another packet in the interpacket interval). This anomaly only shows up in testing because the link is taken out of test packet mode without resetting the core as required by the USB2.0 specification. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 3. Chip Errata for the USB2 Host Controller of i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
Nashua CR610	**Module Affected:** USB2.0 **Title:** Previous LS_THRU_HUB packet causes next FS packet to be sent as LS_THRU_HUB. **Release Date:** 2/13/2006	**Description:** Previous LS_THRU_HUB packet causes the next FS packet to be sent as LS_THRU_HUB. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR566	**Module Affected:** USB2.0 **Title:** Missing reset on register iface_ser_sel_r in the ULPI block. **Release Date:** 2/13/2006	**Description:** Missing reset on register iface_ser_sel_r in the ULPI block. This errata was released in the 4.1.2 version of the ULPI product. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR570	**Module Affected:** USB2.0 **Title:** ULPI logic generates a register write request without register access to j or k traffic when the test mode is set to either test_j or test_k. **Release Date:** 2/13/2006	**Description:** Setting the test mode to either test_j or test_k causes the ULPI logic to generate a register write request (to disable bit stuffing) and to generate either the j or k traffic. However, there is a register in the logic path for the register access request and not one for the j/k traffic. This anomaly causes the j or k access to the ULPI port and lock-out the register write. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR572	**Module Affected:** USB2.0 **Title:** ULPI—set/clear on IFACE and OTG registers always clears bits that are controlled by SW **Release Date:** 2/13/2006	**Description:** ULPI—set/clear on IFACE and OTG registers always clears bits that are controlled by SW. The values for the registers clear access for these bits are inverted. The HW will clear any bit set by SW when an autonomous HW register access is executed. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR577	**Module Affected:** USB2.0 **Title:** Count of inter-packet gap differs from the ULPI specification **Release Date:** 2/13/2006	**Description:** The ULPI specification allows between 15–24 clocks for Host Transmit to Transmit inter-packet gap, however this time starts with the assertion of stp in HS, in full speed the time starts from the receipt of the RX CMD packet that indicates SE0-J transition. The ULPI code begins timing from the FS condition instead of the assertion of STP. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

Table 3. Chip Errata for the USB2 Host Controller of i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.	
Nashua CR579	**Module Affected:** USB2.0 **Title:** ULPI interface does not detect the end of a receive packet on the deassertion of dir only **Release Date:** 2/13/2006	**Description:** The ULPI interface does not detect the end of a receive packet on the deassertion of dir only. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
ARC DDTS not available 17U	**Module Affected:** USB2.0 **Title:** Transmit state machine locks up when FS port is disconnected during back-to-back transmission **Release Date:** 2/13/2006	**Description:** When an FS port is disconnected during back-to-back transmit transactions—for example, OUT token followed by DATA—the transmit state machine can lock up, depending on precisely when the port was disconnected. The only recovery option is a hard or soft reset of the USB block. This bug effects FS, ULPI, host only operation. **Workaround:** There are some possible software workarounds. These involve issuing a soft reset when a Disconnect event occurs. The reset can be further qualified to only be issued when ULPI mode is operating at FS. This should work fine for OTG, SPH and the MPH when only one port is active. However, when multiple ports of the MPH are active, then the reset can cause data to be lost on the ports that remain connected. This is because the soft reset is not port independent. So, if there is activity on the other port, the reset will cause the data on that port to be lost. To prevent this, the software can possibly, wait for or create, a window of inactivity to reset the controller. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1
Nashua CR579	**Module Affected:** USB2.0 **Title:** A remote wakeup can be interpreted as a disconnect in ULPI mode of USBOTG **Release Date:** 2/13/2006	**Description:** A remote wakeup could be interpreted as a disconnect in ULPI mode of USBOTG. This issue involves the latency in asserting synchronous mode. In some instances, the host does not properly latch the K state. The core then determines that it woke-up in a J state. Eventually the host does not takeover the resume, and will later interpret an SE0 and presume a disconnect occurred. The latency in asserting synchronous mode is fixed, so this is no longer an issue. **Fix Plan/Status:** Not Fixed	Rev. 2.0	Rev. 2.0.1

3 Embedded Third-Party Module Errata

The i.MX31 uses embedded third-party modules for which there are separate errata documentation as relevant. This information is provided in Table 4.

Table 4. Third Party Errata

Module Name	Third-Party Source	Module Version (Used by i.MX31)	Errata Source
MSHC (Memory Stick Host Controller)	Sony Corp.	1.3	No Known Errata
USB (Universal Serial Bus Controller)	TDI	4.0.2 [1]	See Table 3.
MBX (Graphics Accelerator, aka GPU)	ARM Ltd.	Lite 1_2_0	MBX ERRATA 1.0.155a External Issue MBXLITE1_2_0. 30Mar2005
MPEG-4 Encoder	Hantro	1_3	No Known Errata
ARM11™ Core	ARM Ltd.	ARM1136JF-S™ r0p2 (mask L38W), and r0p4 (masks 2L38W, 3L38W, M45G, and M91E)	ARM1136J-S/ARM1136JF-S (AT310/AT260) Rev. 10.0, 27Jan2005
L2 Cache Controller	ARM Ltd.	ARM1136JF-S r0p2_01 (L38W), r0p2_02 (2L38W, 3L38W, M45G, and M91E)	ARML210 Errata List AS006-PRDC-003350 6.1

Note:

[1] This includes the critical bug fix that relates to ULPI High Speed support (Ver. 4.2), as follows:
[Host/OTG/Multi-Host; ULPI Only] The ULPI logic was not properly decoding RxActive when it was encoded in its immediate form (**dir** and **nxt** simultaneously asserted with **dir** previously low). If there was no intervening RxCMD to indicate RxActive before the receive data, the link will fail the next receive packets as if a BTO had occurred while waiting for the data phase of the transfer. (Nashua CR569)

4 Revision History

Table 5 lists the document changes since the last revision.

Table 5. Document Revision History

Revision	Sections Affected	Substantive Change(s)
5.7	Table 2	• 12/2012: Added the erratum ENGcm09282.
5.6	Table 2	• Added the erratum ENGcm11424.
5.5	Table 1 and Table 2	• Added Table 1, “Silicon Revision.” • In Table 2, “Chip Errata for i.MX31,” updated Erratum “TLSbo84397.” • Removed TLSbo39790 • Changed 1.35 V to 1.38 V in the description for ENGcm02610

Table 5. Document Revision History (continued)

Revision	Sections Affected	Substantive Change(s)
5.4	Section 1, "Errata," Table 2 and Table 3	Changed the title to "MCIMX31 and MCIMX31L: M91E, Rev. 2.0 and Rev. 2.0.1." Removed all instances of 2L38W, 3L38W, M45G, and M91E. Added new column to both tables. Updated ENGcm02610. Removed the following errata: • MSIIs20595 • DSPhl19588 • TLSbo53656 • TLSbo54060 • TLSbo54564 • TLSb058791 • TLSbo56802 • TLSbo56803 • TLSb061191 • TLSbo61193 • TLSbo61196 • TLSbo58425 • TLSbo59308 • TLSb061175 • TLSbo60029 • TLSb061213 • TLSbo66289 • TLSbo55792 • TLSbo66305 • TLSbo66295 • TLSbo66303 • TLSbo68334 • TLSbo70912 • DSPhl26819 • TLSbo69244 • TLSbo63646 • TLSbo62569 • TLSbo63224 • TLSbo66891 • TLSbo84389
5.3	Table 2	Added the following errata: ENGcm02610 Updated errata: • TLSbo93426 • TLSbo84389 • TLSbo84397
5.2	Document	"Fix/Plan Status" description verbiage was updated throughout for "Fixed" errata.
5.1	Table 2	This revision includes the following: • TLSbo91748: Updated • TLSbo96321: Added

Table 5. Document Revision History (continued)

Revision	Sections Affected	Substantive Change(s)
5	Throughout	This revision includes the following: • TLSbo78667: Updated • TLSbo84397: Updated • TLSbo86232: Added • TLSbo94952: Added • TLSbo93426: Added • TLSbo93469: Added • TLSbo86219: Added • TLSbo95266: Added • TLSbo91750: Added
4.2	Throughout	Release for NDA Customers only. This revision includes the following: • TLSbo91796: New TLSbo91748, added this new errata. • TLSbo91795: Update to TLSbo74193, added new impact information. • TLSbo92176: Update to TLSbo65953, major change to Workaround 1 and 2. • TLSbo92184: Update to Table 3, additional masks added to ARM1136JF-S version.
4.1	Table 2	Release for NDA Customers only. This revision includes the following: • Fix status updated and added silicon Rev. 2.0 mask, M91E, as shown within document. • Added silicon Rev. 2.0, M91E, to errata as shown within document. • Fixed in silicon Rev. 2.0 as shown within document. • Added the following new errata: – TLSbo81670 – TLSbo84378 – TLSbo66891 – TLSbo84389 – TLSbo84397

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