Advance Information

MC68340CE/D
Rev. 1, 12/2001

MC68340 Integrated Processor with DMA Chip Errata

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Contents of this document are intended only for the internal use of Motorola customers designing with this product.

This errata list applies to the following 68340 mask set:

Mask	Processing Geometry	Part Number Suffix
G67F	0.65u	“E”
H37T	0.65u	“E”

The mask set for each part is encoded into the device topside markings - for example, the following markings would indicate a device from the 1F77J mask, manufactured in the 2nd week of 1995:

MC68340FE16C
1F77J
QEAQ9502

1.1 SIM: Loss of Crystal without Limp Mode

If a loss of crystal occurs while the VCO is set to a low operating frequency (131 KHz), the part may lock up and not enter limp mode.

1.2 CPU: System Clock Minimum Frequency

The minimum operating frequency for all clock modes is 100kHz.

1.3 DMA: DONEx Input

If DONEx is recognized asserted before or after the DACKx signal has been asserted or negated, respectively, the channel will block further recognition of DREQx, but will not clear the STR bit in the DMACCR register or set any of the channel termination status bits in the DMACSR register. This specific device functionality is not guaranteed, and may change on future mask sets.

Workaround:

1. Assert DONEx after DACKx has been asserted and before DACKx is negated.

2. Since DONEx as an input is used to signal that the current DMA transfer is the last, peripheral devices that signal a done termination when there are no more DMA transfers required can either initiate a dummy DMA transfer with DONEx asserted, or generate an interrupt directly to the CPU. For the direct interrupt, the interrupt service routine can then clear the DMA channel and initialize it for the next transfer.

1.4 Clock skew for external clock with PLL mode

The MC68340 electrical specifications list a maximum 5ns skew between EXTAL and CLKOUT for external clock with PLL mode. Skew between these 2 edges may exceed +/-5ns. For operating frequencies >= 10MHz, the EXTAL to CLKOUT skew is +9/-5ns maximum (CLKOUT falling edge may occur between 5ns before and 9ns after the corresponding EXTAL falling edge). For frequencies less than 10MHz, the maximum skew is +/-10ns. Note that the PLL locks falling edges (not rising) of the EXTAL clock input and CLKOUT.

1.5 JTAG: TCK Input Low Voltage

Input voltage low level does not meet maximum specification(0.8V) at the operating temperature range for pin tck ONLY. This pin will meet maximum VIL spec of 0.25V over the specified operating temperature. The minimum spec for VIL remains unchanged.

1.6 Notes

These notes describe silicon operation which is different from the original documented operation of the 68340. These are permanent features - future documentation revisions will reflect this operation.

1. JTAG, DONEx — The JTAG dma.ctl scan bit (bit #83) documented in the original User's Manual and implemented in silicon revisions through D75M is extraneous and IEEE 1149.1 non-compliant. Silicon revisions after xD75M do not support this bit and all subsequent bits are shifted forward one position. Rev. 1 of the User's Manual documents the revised (D97R and later) JTAG scan chain.
2. PIT, Background Mode — If Background Debug Mode is entered and exited while the PIT is running and the FRZ1 bit in the SIM MCR is set, the PIT value may decrement by an extra count, shortening the timeout period. This will typically only affect emulation.
3. VCCSYN Power — VCCSYN provides power to the VCC pin when the part is powered down. Power VCCSYN from the same supply as VCC, with appropriate filtering as shown in the manual.
4. Serial: RTS operation — In the hardware flow-control mode of operation, the first assertion of RTSx* after enabling the RxRTS bit (MR1 register bit 7) does not have to be done manually. If a FIFO position is available, RTSx* is enabled immediately when the RxRTS bit is set.
5. Serial Transmitter Disabling: The character in the temporary holding register will be lost if the transmitter is disabled. Wait for TxRDY before disabling the transmitter.
6. Recognition of DONEx* as an input during single address transfers has been modified to cause channel termination after the current transfer. Previous silicon would typically run another transfer, but could also stop after the current transfer if the channel was forced off the bus by interrupt activity or other bus masters (2nd DMA channel or external bus request). Effective mask: F77J (rev C).

7. The tDICL (min.) specification #27 has been changed from 5ns (min.) to 8ns (min.) on the MC68340FE16VC, MC68340RP16VC, and MC68340PV16VC only. Effective mask: F77J (rev C).
8. The PLL lock counter has been modified for external clock with VCO mode to increase the clock delay to lock from 328 to 1864 clocks. This delay applies to PLL locking for both power-on reset and exit from LPSTOP (if the VCO was turned off). This means that power-up reset will be slightly longer, and that the SLOCK bit in the SYNCR register will be set slightly later following a reset. Effective mask: F77J (rev C).
9. The appearance of CLKOUT following RESET has been changed if the VCO was turned off during LPSTOP. If CLKOUT was turned off during LPSTOP, it will not resume toggling upon exiting LPSTOP until the PLL has achieved lock. If CLKOUT was selected to be the EXTAL input during LPSTOP, it will not switch back to the VCO output upon exiting LPSTOP until the PLL has achieved lock. These changes affect both crystal and direct-drive mode. All clock switches will still be clean (no short duration highs/lows). Effective mask: F77J (rev C).
10. JTAG I/O control change. Following JTAG test reset (not functional reset), all I/O and output pins will be set to input or high-impedance states. This was not previously true for some pins. Note that most automated vector generators (and most programmers) don't rely on the reset to determine their direction anyway. Effective mask: F77J (rev C).
11. CPU minimum frequency requirements for using the serial module baudrate generator have been relaxed. This means that customers can run the device below 8MHz for baud rates below 76.8K baud. Please refer to the attached description for more detailed information. Effective mask: F77J (rev C).
12. When the MC68340 is powered up after a long downtime period, the processor sets the "System Reset" bit in the reset status register (RSR) instead of the "Power up" bit. However, if the power is turned off and on quickly, the Power up bit is set as it should be. Effective mask set: G67F and H37T (rev. E).

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