MC33978ER

MC33978 mask N11P errata

Rev. 3.0 — 13 December 2017 Errata sheet

Document information

Information	Content
Keywords	MC33978EK, MC34978EK, PC33978ES, MC33978AEK, MC33978AES, MC34978AEK, MC34978AES
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

1 Revision history

Table 1. Revision history

Rev	Date	Description
1.0	6/2015	• Initial release
	8/2016	• Updated to NXP document form and style
2.0	1/2017	• Updated document format • Added ER02 as per CIN # 201612010I
3.0	12/2017	• Added ER03 as per CIN 201711022I

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2 Product identification

This errata document applies to the following SMARTMOS devices:

Table 2. Orderable part number identification

Part number	Version	Mask ID	Package	Chip marking
MC33978EK	P2.1	N11P	32-pin SOICW-EP	MC33978EK
MC34978EK	P2.1	N11P	32-pin SOICW-EP	MC34978EK
PC33978ES[1]	P2.1	N11P	32-pin QFN (WF-type)	PC33978
MC33978AEK	P2.2	N11P	32-pin SOICW-EP	MC33978AEK
MC33978AES	P2.2	N11P	32-pin QFN (WF-TYPE)	M33978A
MC34978AEK	P2.2	N11P	32-pin SOICW-EP	MC34978AEK
MC34978AES	P2.2	N11P	32-pin QFN (WF-TYPE)	M34978A

[1] For the QFN version (suffix ES), ER01 applies to pre-production (PC) samples only.

2.1 Device part number prefixes

Some device samples are marked with a PC prefix. A PC prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices are marked with the MC prefix.

2.2 Device build information / date code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTZW1025”). The date is coded as four numerical digits, where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “1025” indicates the 25th week of the year 2010.

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3 Errata overview

Table 3. Functional problems table

Functional problems	Short description	Severity level [1][2][3][4]	Solution	Detailed description
ER01	WAKE_B fails to pull-down in Normal mode without V_{DDQ}	Medium	Fix in silicon revision P2.2	Section 4.1
ER02	AMUX output voltage deviates when there are negative inputs on SGx or SPx	Low	None	Section 4.2
ER03	The "Comp Only Comparator" may loose the ability to detect a high/low signal in the corresponding SP/SG input at the extreme corner condition of VBATP < 5.0 V and T_A < −37 °C	Low	Select AMUX output via SPI	Section 4.3

[1] High: Failure mode that severely inhibits the use of the device for all or a majority of intended applications
[2] Medium: Failure mode that might restrict or limit the use of the device for all or a majority of intended applications
[3] Low: Unexpected behavior that does not cause significant problems for the intended applications of the device
[4] Enhancement: Improvement made to the device due to previously found issues on the design

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4 Functional problems description

4.1 ER01—WAKE_B fails to pull-down in Normal mode without V_{DDQ}

4.1.1 Severity level

Medium

4.1.2 Introduction

When operating as an OUTPUT, WAKE_B may exhibit erratic behavior under the following circumstances:

- The MC33978 is in LPM, WAKE_B is released and is expected to be pulled up externally to V_{BATP} to assert the ENABLE_B of the external V_{DDQ} regulator HIGH, which turns the V_{DDQ} rail OFF.
- A switch change is detected. The device wakes up from LPM but WAKE_B is unable to be pulled down to 0 V and fails to enable the V_{DDQ} regulator. Hence no complete system wake-up is possible.

4.1.3 Problem

The WAKE_B internal block is currently powered by V_{DDQ}. When V_{DDQ} is lost, there is no signal to drive the gate of the open drain FET and pull the WAKE_B pin low.

This issue is present solely at the system level and only impacts applications implementing the WAKE_B as the control signal for the V_{DDQ} voltage rail. For those applications in which V_{DDQ} is always ON, this issue should not be a problem.

4.1.4 Work-around

No work-around

4.1.5 Fix plan

Will be fixed in silicon 2.2

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4.2 ER02—AMUX output voltage deviates when there are negative inputs on SGx or SPx

4.2.1 Severity level

Low

4.2.2 Introduction

AMUX output voltage deviates when there are negative inputs on other SGx or SPx channels.

By design, the multiplexer for AMUX operates only in the positive 0 V to 5.0 V range and does not take into account negative inputs. From that perspective, it works as designed. However, in customer applications that exclude the AMUX channel, the other SGx and SPx pins are allowed a minimum –1.0 V negative input. The SGx or SPx negative inputs may cause the AMUX output to deviate from its input.

4.2.3 Problem

Negative voltages are turning on parasitic devices on SGx/SPx channels, causing AMUX input voltage error.

This issue is present at the system level and only impacts applications in which the MCU reads the AMUX when there is negative input on other SGx or SPx channels. This issue is not a problem for those applications in which AMUX is not used or negative inputs are not present on SGx or SPx.

4.2.4 Work-around

The MCU should read the AMUX only when no negative offset is present on any of the SGx/SPx input pins

4.2.5 Fix plan

None

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4.3 ER03—Comp Only Comparator may loose the ability to detect a high/low signal in the corresponding SP/SG input at the extreme corner condition of VBATP < 5.0 V and T_A < −37 °C

4.3.1 Severity level

Low

4.3.2 Introduction

The “Comp Only” comparator (also referred as “Comparator only”), is an alternative to the default comparators on SG/SP pins used to detect changes in switch states during low-power mode (LPM). It has no wetting current and a fixed 2.5 V threshold compatible with standard CMOS outputs. It is selectable via SPI configuration (LPM comparator only register). When the SGx/SPx bit on the LPM Comparator Only register is set to 1, the corresponding channel uses this 2.5 V threshold during the Sleep mode (only) and a detection from high-to-low or low-to-high in the SGx/SPx pin causes the device to wake up and return to normal operation.

A secondary function of the Comp Only comparator, is to serve as the high/low detection threshold in hardwired mode allowing a selection of the AMUX input via 2 or 3 of the SG pins. When the aconfig0 and aconfig1 on the Device Configuration registers are set to 10 or 11, the AMUX uses the pin SG1, SG2 and SG3, to pick which channel will be routed out to the AMUX pin.

The device is defined and designed to meet parametric specifications in the operating voltage range of 6.0 V to 28 V and fully functional from 4.5 V to 38 V. Under these premises, the issue described above does not meet the functional requirement at the corner condition presented.

However, from a system perspective, the functional operating range (4.5 V to 38 V) is intended to provide a functional support on transitory conditions such as a crank profile, load dump. In these conditions, the system is not expected to remain in low-power mode for an indefinite time and expect to be woken up by a system I/O (which is the use case for the Comparator only threshold).

In the case of the hardwire AMUX selection, the system is not expected to perform critical parametric reading in the operating range below 5.0 V. In this range, the system cannot guarantee the parametric values and therefore it is not expected that the AMUX to be read outside of the parametric operating range.

4.3.3 Problem

In certain corner conditions, the Comp Only comparators may loose the ability to detect a high or a low signal in the corresponding SG/SP input. Such conditions are well identified as listed below:

1. Device temperature is below −37 °C
2. VBATP input voltage is below 5.0 V

All other scenarios within the device operating range work as described in the device specification sheet.

1. When any of the SG/SP inputs uses the Comp Only threshold (LPM comparator only bit set to 1), if the part is in the LPM and the system meets the condition mentioned

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above, the system may loose the ability to wake up when the corresponding channel using the Comp Only threshold changes state from low-to-high or may falsely detect a change in state of a pin that is normally high.

2. In systems using the SG1, SG2 and SG3 pins in hardwired mode to select the input source to be routed to the AMUX pin, for the conditions listed above, any or all of the dedicated SG pins can change state from “1” to “0” redirecting the input of AMUX from the intended input source. For lower voltages and temperatures, SG1, SG2 and SG3 will be read as “0”. The IC resumes proper operation when either temperature or supply voltage increase.

4.3.4 Work-around

1. In the specific use case that the system is intended to operate at voltages lower than 5.0 V for extended periods of time and it requires to be able to come in and out of the low-power mode, the regular 4.0 V detection threshold with or without wetting current is still available and it will perfectly wake up the device from low-power mode if the state change comes from a regular switch connected at the input.
2. In the scenario that user requires to perform any AMUX reading in the non-parametric operational range (VBATP < 5.0 V) for informative purposes, the AMUX output can be selected via SPI command and the MC33978 provides proper reading with the corresponding specification degradation due to the VBATP voltage level.

4.3.5 Fix plan

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