Mask Set Errata for Mask 3N40J

This report applies to mask 3N40J for these products:

- KEA8

Errata ID	Errata Title
6946	Core: A debugger write to the I/O port might be corrupted during a processor write
6945	Core: Processor executing at HardFault priority might enter Lockup state if an NMI occurs during a waited debugger transaction
6749	I2C: The I2C_C1[MST] bit is not automatically cleared when arbitration is lost
7331	IO: High current drive pins not in high-Z state during power up
7914	PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.

e6946: Core: A debugger write to the I/O port might be corrupted during a processor write

Errata type: Errata

Description: A debugger can perform memory accesses through the Cortex-M0+ processor bus matrix while the processor is running.

Because of this erratum, a debugger write to the I/O port might be corrupted if it occurs while the processor is executing a write. The processor write completes successfully. However, under specific timing conditions, the matrix might incorrectly replace the debugger write data with the value zero.

This erratum does not affect debugger writes outside the I/O port region of the memory map, or debugger reads.

Conditions:

The following timing-specific conditions must all be met:

- The processor is running (not halted in Debug state).

- The debugger performs a write within the I/O port region of the memory map.

- The processor performs a write.

Implications:

The debugger might corrupt the targeted memory or configure the targeted device incorrectly.

Workaround: The debugger can work around this erratum by halting the processor in Debug state before performing writes to the I/O port region of the memory map.

e6945: Core: Processor executing at HardFault priority might enter Lockup state if an NMI occurs during a waited debugger transaction

Errata type: Errata

Description: A debugger can perform memory accesses through the Cortex-M0+ processor bus matrix while the processor is running.

Because of this erratum, the processor might erroneously enter Lockup state if a debugger-initiated access on the AHB-Lite master port is subject to wait states while the processor is running, executing at HardFault priority and taking a Non Maskable Interrupt (NMI). Under very specific timing conditions, the processor might incorrectly stack a ReturnAddress of 0xFFFFFFFE on NMI entry. On NMI return, the processor unstacks the incorrectly stacked ReturnAddress and enters Lockup state at HardFault priority.

Conditions:

The following timing-specific conditions must all be met:

- The processor is running (not halted in Debug state) and is executing at HardFault priority.

- The processor executes a single-cycle instruction at a word-aligned address.

- The debugger performs an access through the AHB-Lite master port that is subject to wait states.

- An NMI becomes pending.

Implications:

The processor stops executing the code in the HardFault handler and enters Lockup state at HardFault priority as if a fault had occurred.

Workaround: The debugger can work around this erratum by halting the processor in Debug state before performing accesses outside the Private Peripheral Bus (PPB) region of the memory map.

e6749: I2C: The I2C_C1[MST] bit is not automatically cleared when arbitration is lost

Errata type: Errata

Description: When the I2C module is used as a master device and loses bus arbitration, it correctly switches to be a slave device. The I2C_C1[MST] bit is not automatically cleared when this occurs but it does correctly operate as a slave.

Workaround: When the I2C module has been configured as a master device and the I2C_S[ARB] bit is set, indicating arbitration has been lost, the I2C_C1[MST] bit must be cleared by software before the I2C_S[ARB] bit is cleared.

e7331: IO: High current drive pins not in high-Z state during power up

Errata type: Errata

Description: The high current drive pins on the chip are unexpectedly driven low for a short period during power up. All other I/O pins are high impedance. The issue happens only before VDD reaches the power-on reset voltage. After power up the normal I/O functions on the high current drive pins are not impacted.

Workaround: Use one or more combination of the following methods to avoid possible issues:

- Use high current drive pins as current source for LED connection, but keep total IDD < 120mA (refer to device data sheet for IDD)
- Configure the corresponding Flextimer channel output polarity as active high which are muxed with high current drive pins
- Use high current drive pins with NPN transistor (active high) to drive relays
- Keep VDD ramp-up time greater than or equal to 1KV/s and less than or equal to 10KVs to disable LED and/or driver action during power up

e7914: PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.

Errata type: Errata

Description: If a write to the PIT module enable bit (PIT_MCR[MDIS]) occurs within two bus clock cycles of enabling the PIT clock gate in the SIM_CG register, the write will be ignored and the PIT will fail to enable.

Workaround: Insert a read of the PIT_MCR register before writing to the PIT_MCR register. This guarantees a minimum delay of two bus clocks to guarantee the write is not ignored.

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