TN00042

NTAG I²C *plus* - FAQs

Rev. 1.0 — 10 July 2018
491610

Revision history

Rev	Date	Description
v. 1.0	20180710	First version

1   Introduction

This technical note shall be used as a set of guidelines for integrating NTAG I²C *plus*.

Hints are given to accelerate overall integration process and recommendations are listed to ensure a working prototype. It contains a collection of the answers to the most common questions from customers, integrating NTAG I²C *plus* into applications.

This is a living document which will be updated regularly.

2 Abbreviations

Following abbreviations are used within this technical report

Table 1. Abbreviations

Abbreviation	Meaning
EEPROM	Electrically Erasable Programmable Read-Only Memory (non-volatile memory)
FD	Field Detection
I²C	Inter-Integrated Circuit
kbps	kilo bits per second
kHz	kilo Hertz
NDA	Non-Disclosure Agreement
NFC	Near Field Communication
PMU	Power Management Unit
POR	Power On Reset
SRAM	Static Random Access Memory (volatile memory)

3 General

3.1 NFC devices

3.1.1 NFC field of the reader is switched off automatically - workaround

There are basically only two options:

1. Either to reconfigure the reader, that NFC field is constant on,
2. Use of a different reader

3.1.2 How can I find out if a reader supports FAST READ and FAST WRITE command?

Both, FAST READ and FAST WRITE commands are NXP proprietary. So called "transparent" or "transceive" commands need to be used to be able to send proprietary commands. On modern readers, which have ISO/IEC 14443 Type A communication support, it is expected to have transparent command support.

3.2 EEPROM

3.2.1 Accessing EEPROM from I²C while RF_LOCKED = 1b

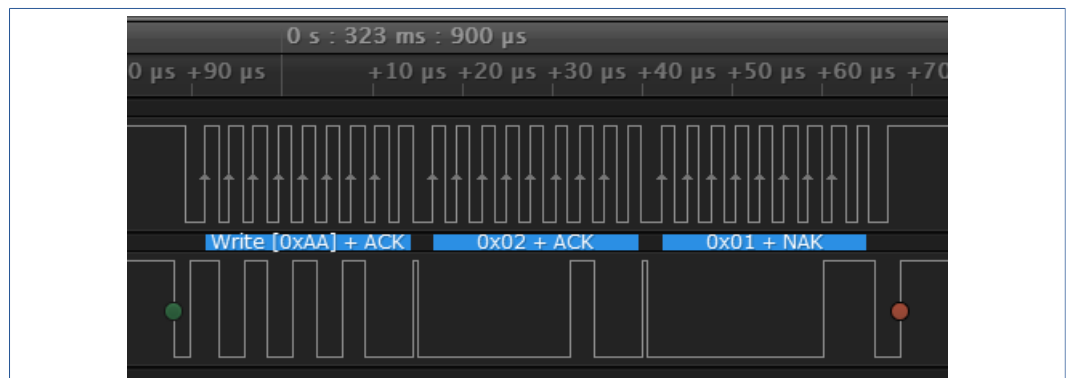Access to EEPROM from I²C side will be NAK-ed at following timestamps:
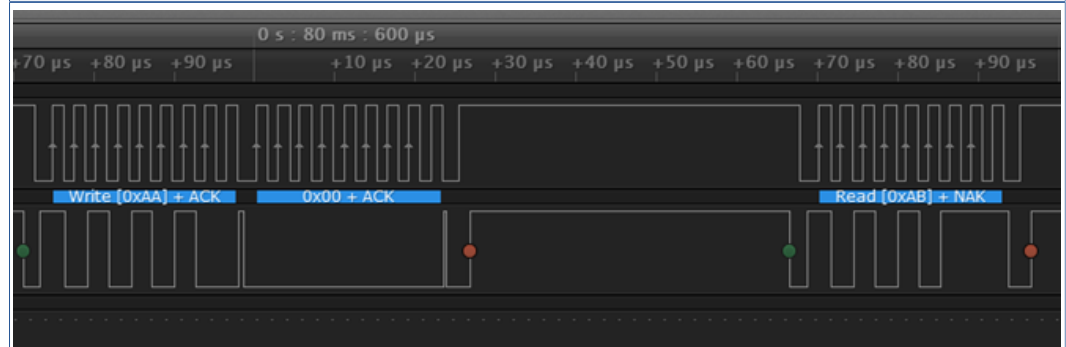

Figure 1. WRITING operation – after D0

Figure 2. READING operation – after 7bit + Read addressing

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3.2.2 Why it is mandatory to wait after programming the tag from I²C perspective

The ACK of last byte of the write command triggers the write cycle. If there comes another command too early, this programming cycle will be interrupted and leads to corrupted data.

After each write to EEPROM from I²C perpective, you shall wait 4.5 ms.

After each write to SRAM from I²C perspective, you shall wait 0.4 ms.

From RF perspective, there is no need to wait, as the response is sent, after programming the tag.
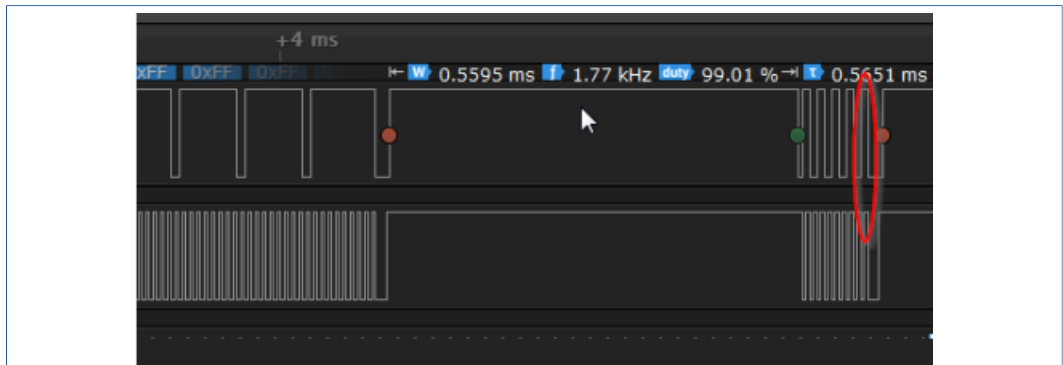

Figure 3. NAK if NTAG is addressed to early after EEPROM WRITE

3.2.3 How is the memory of the NTAG I^{2}C *plus* distributed?

With NTAG I2C plus, we changed the memory map compared to old NTAG I2C to improve interoperability and simplify usage of the two offered memory versions.

The very first sector looks totally the same now for both memory version. The 2K version (1912 byte) offers on top complete second sector as user memory.

We moved the mapping of Session Registers and SRAM to the very first sector, but kept the session registers mapped in Sector 2 for backward compatibility reasons. However it is recommended to access all features on sector 0.

3.2.4 Why is it not possible to write a NDEF message with TagWriter?

We decided to keep full flexibility on tag configuration from RF perspective. Therefore the tag is NOT formatted according to NFC Forum. When Capability Container and an empty NDEF message are programmed to the tag, TagWrite can write new NDEF messages to the tag. Example of NFC Forum-compliant formatting - Capability Container (CC) is in data sheet [1]. Also refer to NFC Forum Type 2 Tag specification [3].

3.2.5 Is it possible to configure memory from the RF side to be inaccessible to unintended viewers?

On NTAG I^{2}C *plus*, 2K access to second sector can be blocked from RF perspective. If NFC_DIS_SEC1 is set to 1b, second sector can only be accessed from I^{2}C perspective.

When setting NFCS_I2C_RST_ON_OFF to 1b, complete tag is invisible from RF perspective. If using this feature, also take a look to [Section 3.5.1].

3.3 Session Registers

Session registers can be used to monitor an ongoing communication session. From
I^{2}C perspective, some bits can be modified to change the behavior of NTAG I^{2}C *plus* in
current session, not from RF perspective.

3.3.1 What is the difference between Configuration and Session Registers?

Configuration registers are stored and accessible in the user EEPROM (NFC address
on sector 0: E8h and E9h; I^{2}C address: 3Ah). These bytes define the default behavior of
NTAG I^{2}C *plus* after start-up.

Session registers are mapped and accessible in the user EEPROM area (NFC address
on sector 0: ECh and EDh; I^{2}C address: FEh). The configuration register gets copied
to these session registers during start-up. From I2C perspective, some values may
be changed to modify the tag behavior for the current session. On next POR (power-
on reset), these session registers get overwritten again with the default values from
configuration registers.

3.3.2 When get session registers initialized?

After POR Configuration bytes get copied into session registers, however there are three
conditions to be considered:

- tag is already powered via VCC and RF field comes
  - if RF has access to session registers, registers will be initialized again
  - if I²C has exclusive access to session registers, initialization is not possible
- when tag is already powered via RF and VCC comes, session registers will not be
  initialized again

3.4 SRAM

For frequently changing data, e.g. when updating the firmware of the host, a volatile
memory of 64 bytes with unlimited endurance is built in. SRAM can only be accessed,
when NTAG I^{2}C *plus* is powered via VCC.

3.4.1 What is the proper reaction on a NACK when accessing SRAM via I^{2}C?

The arbiter, which internally takes care of communication flow, is designed and tested
in the way, that there are no side effects expected if NACK happens before the end of
process. It is recommended to simply retry access to SRAM.

3.4.2 What is the proper reaction on a NACK when accessing SRAM via NFC

A NACK on NFC interface causes a state machine change. The tag falls out of ACTIVE
state and enters IDLE/HALT state. It strongly depends on the reader design whether or
not current session gets lost. When the RF reader resets the field, current session is lost
and needs to be re-initilized, if not current session can be continued.

3.5 NFC Silence

NFC Silence maybe used to disable the NFC interface to avoid unintended access
via RF interface. Note, that this feature is multiplexed with I^{2}C soft reset. This means,

when NFC Silence is enabled, also I²C soft reset is enabled and the tag will reset if on a repeated start condition.

3.5.1 Can NFC Silence feature be used to recover a stuck reader?

Well designed reader shall not stick at all. Anyway it is hard to distinguish from host side between "reader is stuck" and "bad positioning of the tag in the RF field". It is not recommended to use this feature for this purpose. However, if used, enabling NFC silence for 1000 ms should be sufficient.

3.6 I^{2}C

3.6.1 What is the default I^{2}C device address?

On default NTAG I^{2}C *plus* reacts, when addressed with its 7-bit device address 55h.

3.6.2 How can I change the I²C device address?

NTAG I^{2}C *plus* has configurable I^{2}C address. However, it can only be modified via I^{2}C interface. The I^{2}C device address can be modified by writing the I^{2}C write address (most significant 7-bits contain the I^{2}C device address followed by 0b as least significant bit) to byte 0 of block 0.

NOTE: When reading this byte NTAG I^{2}C *plus* returns 04h, which is UID0 of the unique serial number (manufacturer code for NXP). Therefore, if possible, it is recommended to use 04h as I²C write address (02h device address). To keep default device address of 55h, byte 0 of block 0 needs to be set to AAh.

3.6.3 How can I read the I^{2}C address?

Unfortunately, it is not possible to read the I²C address. In both cases, reading from RF and I^{2}C side, this byte always contains 04h, which is UID0 of the unique serial number (manufacturer code for NXP).

3.6.4 I have overwritten my I^{2}C address unintentionally. How can I recover my tag?

As it might happen, during configuration of the Capability Container, and or static lock bytes, which are also located on block 0. When you first have read block 0 and then just modified related bytes, I^{2}C address might be 04h, as this is returned as first byte of the memory.

If not, try "brute force" and access the tag from I^{2}C device address 00h to 7Fh, like it is done in Peek and Poke.

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4 Hardware

4.1 Delivery Forms

NXP offers different packages to fulfill customer needs. E.g., if wave soldering process is used, SO8 package can be used.

4.1.1 What IC markings designate the different versions of NXP connected tag chips?

Table 2. Marking codes for NTAG 21xF

Type number	Package	Memory	Marking code		
		[Bytes]	Line 1	Line 2	Line 3
NT2H1311F0DTL	HXSON4	144	N3F	YWW	-
NT2H1611F0DTL	HXSON4	888	N2F	YWW	-

Table 3. Marking codes for NTAG I²C

Type number	Package	Memory	Marking code		
		[Bytes]	Line 1	Line 2	Line 3
NT3H1101W0FHK	XQFN8	888	N11	-	-
NT3H1201W0FHK	XQFN8	1908	N12	-	-
NT3H1101W0FFT	TSSOP8	888	31101	DBSN ASID	YWW
NT3H1201W0FFT	TSSOP8	1908	31201	DBSN ASID	YWW

Table 4. Marking codes for NTAG I²C *plus*

Type number	Package	Memory	Marking code		
		[Bytes]	Line 1	Line 2	Line 3
NT3H2111W0FHK	XQFN8	888	211	-	-
NT3H2211W0FHK	XQFN8	1912	221	-	-
NT3H2111W0FTT	TSSOP8	888	32111	DBSN ASID	YWW
NT3H2211W0FTT	TSSOP8	1912	32211	DBSN ASID	YWW
NT3H2111W0FT1	SO8	888	NT32111	DBSN ASID	nDYWW
NT3H2211W0FT1	SO8	1912	NT32211	DBSN ASID	nDYWW

Used abbreviations:

DBSN: Diffusion Batch Sequence Number

ASID: Assembly Sequence ID

n: Assembly Centre Code

D: RHF-2006 indicator

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Y: year

WW: week

NTAG I^{2}C *plus* is pin to pin compatible to NTAG I^{2}C. NXP recommends using NTAG I^{2}C *plus* for new designs and for recent designs. When using NTAG I^{2}C 888 byte version, NTAG I^{2}C *plus* is also compatible from memory layout. Only if you use NTAG I^{2}C 1908 byte version, you might need small software modifications when moving to new improved NTAG I^{2}C *plus*.

4.1.2 XQFN8

4.1.2.1 Should the center pad of the I^{2}C chip be connected?

The center pad of the chip does not connect to anything internally. We recommended leaving this pad unconnected.

4.1.3 Gold bumped die

4.1.3.1 Where do I get the Wafer specification?

Wafer specification is available on DocStore, after signing an NDA.

4.2 Antenna

4.2.1 What tools are available for simple antenna board layouts?

One free option is Eagle PCB software, which may be downloaded at the following link:http://www.cadsoftusa.com/download-eagle/

It is limited to 2 schematic sheets, 2 signal layers, and 80 cm^2 board area.

4.2.2 Can I place my antenna on metal?

When you place an antenna directly on a metal plate, e.g., ground plane, no communication is possible. Some distance and/or ferrite is needed to isolate the antenna from the metal.

4.3 Field detection pin

The filed detection pin can be used as trigger for the host system. As it is an open-drain implementation, an external pull-up resistor (> 5kΩ) connected to VCC (1.2 V to 3.6 V) is needed to pull the line high, when Field Detect is not asserted. NTAG I^{2}C *plus* will assert the signal to low, when a field detector condition is met (e.g. tag enters the RF field).

4.3.1 When is FD pin pulled low, when configured to indicate tag selection?

"Tag selection" trigger is initiated when the tag goes to ACTIVE state i.e. after doing ANTI-COLLISION. When a reader does anti-collision every now and then, you see the trigger on FD pin. E.g., after a HALT command the reader has to do full anti-collision again.

Recommended configuration for FD_ON 10b - "FD pin is pulled low by selection of the tag" and recommended configuration for FD_OFF is 01b - "FD pin is released, if the field is switched off or the tag is set to the HALT state".

4.3.2 Is there any configuration, that FD pin indicates NFC write operation?

No, unfortunately not on this generation of IC. It will be implemented in next generation of connected tags.

4.3.3 Do you recommend RC filtering on the FD signal for the NTAG I^{2}C *plus*?

RC filtering is not required on the FD signal.

4.3.4 Is the FD on the NTAG I^{2}C *plus* the same as on the NTAG203F, the NTAG 213F, or NTAG 216F series of products?

The NTAG I^{2}C *plus* FD is similar to the NTAG 213F and NTAG 216F with an open-drain, asserted low. The NTAG 203F was able to source and sync and was asserted high.

4.3.5 Can the FD source current for an interrupt signal?

No, the output is an open-drain and can only sink current. It cannot source the signal.

4.4 Energy Harvesting

NTAG I^{2}C *plus* provides the capability to supply external low-power devices with up to 15 mW of energy, harvested from the RF field of an NFC device.

The voltage and current from the energy harvesting depend on various parameters, such as the strength of the RF field, tag antenna size, and distance from the NFC device.

If higher values of energy harvested are needed, it can be done via external components.
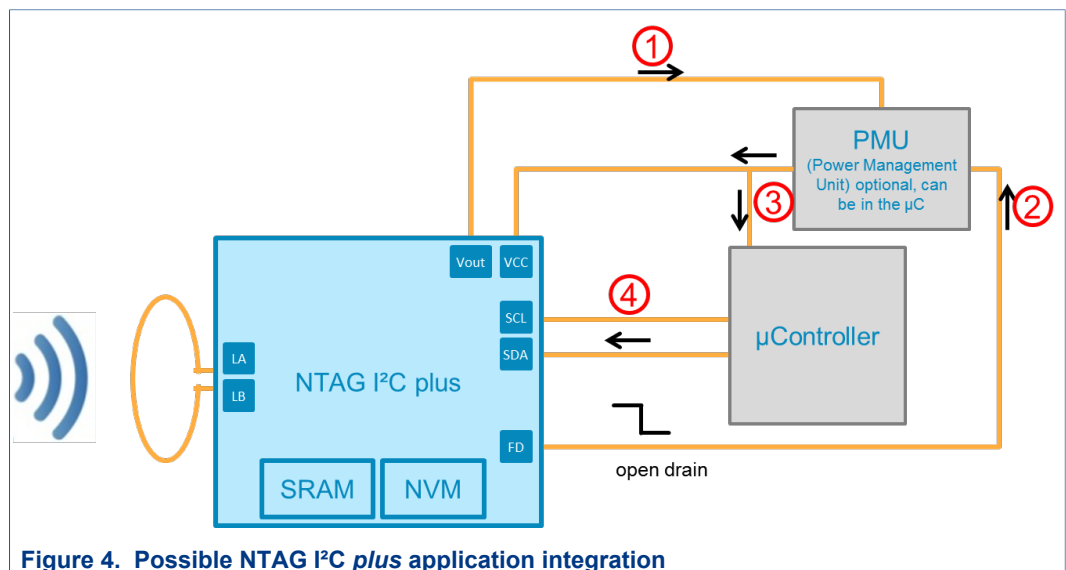
Figure 4. Possible NTAG I²C *plus* application integration

4.4.1 What shall be considered when using energy harvesting?

- NXP recommends a storage capacitor (105 nF to 220 nF) between VOUT and GND close to the IC terminals.
- To charge storage capacitor, NFC device needs to respect 5 ms start-up time as defined in ISO/IEC 14443.
- Direct connection to VCC is needed to supply NTAG I^{2}C *plus* pads.
- Pull-up resistors (> 5kΩ) on SCL, SDA and FD pin are needed.

4.5 General Power Considerations

4.5.1 How much leakage current would be expected if the VCC pin of the NTAG I^{2}C *plus* were connected to an external source and pull-up resistors were connected to FD, SCL and SDA?

When inactive, the pull-up resistors, which would be connected to the SCL, SDA and FD lines, would essentially be floating as the resistors would be connected to an open-drain FET, so the leakage would be minuscule—in the pico amp range. If external power is continuously provided to the VCC pin, the consumption may be up to 150 uA. If desired, one method of reducing this current might include use of a Power Management Unit (PMU) to source power to the NTAG I^{2}C *plus* only after an FD trigger or when needed by the I^{2}C bus.

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5 Software

5.1 Host

5.1.1 Pass through mode

When using pass through mode to, e.g., transfer sensor log data or update host firmware, it depends on the overall use case which approach fits best your needs.

5.1.1.1 When is it recommended to poll for RF_LOCKED session bit instead of using FD pin?

As polling for a session register bit takes time and hence reduces pass through performance, it is recommended to use FD pin to synchronize the data transfer. Only in case FD pin cannot be used as interrupt, polling RF_LOCKED bit needs to be used.

5.1.1.2 Is it possible to pre-load SRAM, before starting pass through transfer?

Yes, it is possible to first write data to be transferred to the SRAM and then enable pass through mode, of course VCC power must be there already at that point of time.

5.1.2 Bluetooth LE pairing information NDEF

To create the BTSSP LE (Low Energy) NDEF message, you need to fill in the following OOB (Out Of Band) data types:

1. LE Bluetooth Device Address data type, which consists of 6 bytes of device address and address type. The address type may be a Public Device Address (0x00) or a Random Device Address (0x01).
2. LE Role data type, which value is defined to four specific roles: PeripheralOnly (0x00), CentralOnly (0x01), PeripheralPrefered (0x02), CentralPrefered (0x03).

```
uint8_t BTSSP_LE_pairing_NDEF_msg[] = {
    /*1*/    0xD2,    // NDEF record header: MB=1b ME=1b
 CF=0b SR=1b IL=0b TNF=010b
    /*1*/    0x20,    // Record Type Length
    /*1*/    0x0c,    // Payload Length
    /*32*/
 'a','p','p','l','i','c','a','t','i','o','n','/','v','n','d','.',
 'b','l','u','e','t','o','o','t','h','.','l','e','.','o','o','b',
    // Record Type Name
    /*1*/    0x08,    // LE Bluetooth Device Address length:
 8 bytes
    /*1*/    0x1B,    // LE Bluetooth Device Address data
 type
    /*6*/    0xc6, 0xc5, 0xc4, 0xc3, 0xc2, 0xc1, // Bluetooth
 Device Address: 6 bytes + 1 (next byte)
    /*1*/    0x00,    // added at the end of the Device
 Address
    /*1*/    0x02,    // LE Role Length: 2 bytes
    /*1*/    0x1c,    // LE Role data type
    /*1*/    0x02,    // LE Role:  PeripheralPrefered
    };
```

An example how to define the BTSSP LE NDEF message.

LE Device address is: (MSB) C1:C2:C3:C4:C5:C6

Address type is: Public Device

LE Role is: Peripheral Preferred

For more details on this topic, see reference document [13].

5.2 NFC Reader

5.2.1 Pass through mode

5.2.1.1 When is it recommended to poll for RF_LOCKED session bit instead of using proper timeout value?

As polling for a session register bit takes time and hence reduces pass through performance, it is recommended to use proper timeout value, dependent, and different on every system. RF_LOCKED session bit should only be used at the beginning to detect the start of the transfer. When using (recommended) FAST_WRITE command, the complete SRAM is written with one command and polling for RF_LOCKED is not needed at all.

5.2.2 Is there a multi page transfer option available?

NFC Forum defines only a READ command (read 4 pages = 16 bytes) and a WRITE command (write one page = 4 bytes).

NTAG I2C *plus* offers on top a FAST READ command to read more than 4 pages of EEPROM or SRAM at once to increase overall transaction time. The implemented FAST WRITE command can be used to write complete 64 bytes of SRAM in one shot.

NOTE: FAST WRITE command can only access SRAM.

5.3 Arbitration

If both interfaces are powered by their corresponding source, only one interface has access to the EEPROM and SRAM according to the "first-come, first-serve" principle. Access to session registers is always possible.

5.4 Are there any additional support tools?

There are several useful apps available on Google Play.

- **NFC TagInfo** by NXP
  NFC TagInfo is the "Swiss Army Knife" for NFC tags. It is a value checker, memory content viewer, and analysis tool.
  NOTE: This app is also available for iOS11 devices like iPhone 7, 8 or X.
- **NFC TagWriter** by NXP
  NXP TagWriter for NFC applications allows you to store contacts, URLs, and SMS, as well as text messages and generic URIs to any NFC-enabled tags and to NFC enabled posters, business cards, watches, etc.
- **NTAG I²C Demoboard**

This is the android app needed to operate the NTAG I^{2}C *plus* Explorer Kit

- **Originality Checker**
  Does Originality Signature check

Java tool:

- **TagXplorer**
  Available on http://www.nxp.com

6 Performance

6.1 What is the data transfer speed between the RF interface and the I²C interface?

ISO/IEC 14443 and NFC Forum define the air interface speed of 106 kbps. The I²C interface operates up to 400 kHz. For both interfaces, there is some protocol overhead, EEPROM programming time and latency time which reduces overall transaction speed. With an optimized closed system, pass through data rate of approximately 40 kbps can be achieved. With good mobile phones, still 30 kbps are possible.

6.2 What read ranges can be expected with common mobile phones?

Achieved read ranges are strongly dependent on the used antenna sizes (coupling) and field strength. As a thumb rule you can expect a read range of approximately the diameter of the antenna, when the tag antenna and NFC antenna have similar size. With phones 2.5 cm to 5 cm (1 to 2 inches) are typical values for NTAG I²C *plus*.

7   References

1. NTAG I^{2}C *plus* data sheet
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   Technical Specification
4. NFC Forum - Activity 2.0
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7. AN11276 NTAG Antenna Design Guide
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