Freescale Semiconductor
Engineering Bulletin

Document Number: EB694
Rev. 0, 05/2008

MPC5517G (RevA) vs MPC5516G (Rev0) Differences Document

by: David McMenamin
MSG Applications Engineering, EKB

1 Introduction

Freescale has introduced the prototype MPC5517G (Rev. A) device as part of its ongoing roadmap for the MPC5510 family of products.The MPC5517G is an enhancement of the current MPC5516G (Rev. 0) device, providing more Flash and RAM and several new features.

This document describes the new features on the MPC5517G and explains the differences between the two devices. This information should help you if you are planning to migrate from the MPC5516G to the MPC5517G.

Future MPC5510 family derivatives will be compatible with the features available on the MPC5517G.

You should use this document along with the latest revision of the reference manual and errata sheet to aid your migration from the MPC5516G to the MPC5517G.

Contents

2 Overview

The differences between the MPC5516G and MPC5517G are listed below.

- Memory enhancements
  - Flash increased from 1 MB to 1.5 MB
  - RAM increased from 64 KB to 80 KB
  - 80 KB RAM selection included in Sleep mode
- Media Local Bus (MLB) added
  - Integrated SoftMLB interface logic
  - MLB signals added to Port E and Port F (alternative positions)
  - Pad type changed on Port E and Port F to support the additional features.
- Debug
  - Retention of JTAG and Nexus communication upon exit from Sleep and Stop low-power modes added
- ADC
  - eQADC supports for three additional external multiplexers added
  - Reference bypass capacitor can be connected or disconnected in software
- EBI
  - ALE signal added to port F12
  - Support of non-multiplexed address[8:15] added on port F[2:9]
  - Chip selects increased from two to four
- Real Time Clock (RTC) / Autonomous Periodic Interrupt (API)
  - RTC runs through system reset on MPC5517G
  - 16 MHz IRC/512 bypass to API option added
- Miscellaneous
  - Number of DSPIs increased from three to four
  - FM function added to PLL
  - I^2C module updated — supports BIIE Interrupt
  - SIU test lock bit added

3 Memory

The MPC5517G has 16 KB of RAM and 512 KB of Flash memory more than the MPC5516G. This memory is available for use in the user application. The memory address ranges and sizes for the Flash and SRAM for the two devices are compared in Table 1.

Table 1. Memory Comparison Table

	Flash			RAM		
	Start Addr	**End Addr**	**Size**	**Start Addr**	**End Addr**	**Size**
MPC5516G	0x00000000	0x000FFFFF	1MB	0x40000000	0x4000FFFF	64KB
MPC5517G	0x00000000	0x0017FFFF	1.5MB	0x40000000	0x40013FFF	80KB

The Flash memory has four additional 128 KB blocks. The Flash memory segmentation is compared in Figure 1.

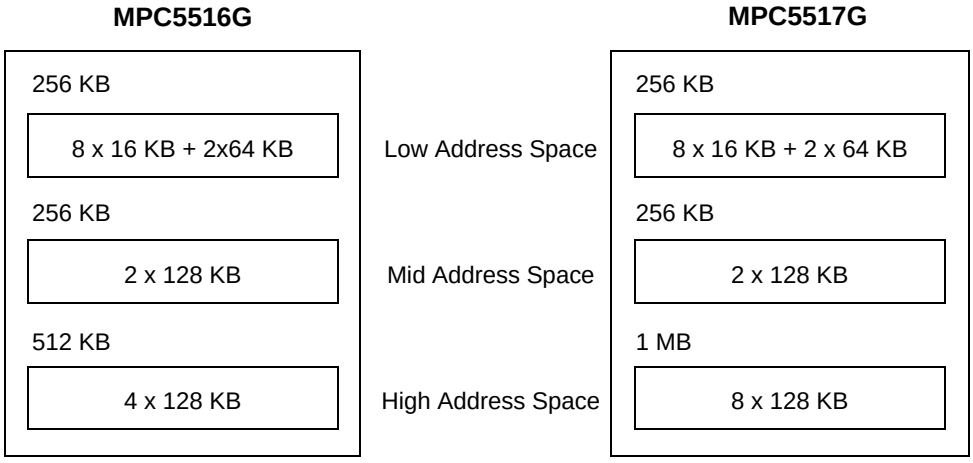

Figure 1. Flash Memory Segmentation

To support the extended memory range of the newer device, a number of registers in the Flash and CRP modules of the MPC5517G device have been changed.

- The Flash module has been extended to provide support for programming and erasing the extra 512 KB of Flash memory. The Flash module configuration register has also been updated to indicate correctly the size of the increased Flash array. The size field in the MPC5517G MCR reads 0x0101 as apposed to 0x0011 for the 1MB array in the MPC5516G.
- The High-Address Space Block Lock (HLOCK) field in the High-Address Space Block Locking Register (HBL) has been increased from four bits to eight bits to support the additional Flash blocks. The High-Address Space Block Select field in the High-Address Space Block Select Register has been increased form four bits to eight bits to allow from zero to eight of the high address space blocks to be selected for erase.
- In the CRP module, the RAMSEL field in the Power Status and Control Register has been updated to allow up to the entire 80 KB of RAM to retain power when in Sleep mode.

4 Media Local Bus (MLB)

Some of the Rev. A devices in the MPC5510 family, including the MPC5517G, feature SoftMLB interface logic to allow the MPC5510 device to join a MOST communications network.

The MPC551xE/G devices implement a software emulated MLB solution (SoftMLB) that is based on the e200Z0 core (IOP) but also uses system RAM, two DSPIs, and the eDMA module. In addition, SoftMLB interface logic to detect the FRAMESYNC pattern and generate the appropriate triggers to the IOP, eDMA, and DSPIs has been integrated. The MLB signals are routed out on Port E and Port F, which are on the VDDE1 and VDDE3 power domains, respectively. The MLB signals on Port E must be level-shifted externally to be compatible with the 2.5 V MLB bus. The VDDE3 domain is a smaller domain that is shared with Nexus, JTAG, and some EBI signals.

Port E and Port F have been changed to support the selection of this new feature as a pin assignment.

The MLB interface is located at 0xFFF8_4000 in the memory map. A Freescale software API for the MLB will be made available (date of release to be advised).

5 Debug

A new feature implemented on the MPC5517G is the ability to retain Nexus and JTAG debug communications as the device enters and exits the Sleep and Stop low-power modes of operation. This is an enhancement over Rev 0 devices, which lost debug communications when entering low-power modes as the pins used for debug were disabled to save power.

Although the pins are still disabled in the MPC5517G (under the control of the pad keeper hardware), when in low-power modes, the debug hardware on the MCU now has the ability to handshake with the debugger before entering and before fully exiting low-power modes. This allows the debug software to retain the status of the device before entering low-power modes, and to re-establish communications before low-power mode is exited.

Please speak to your tools vendor to establish if their hardware and software supports this feature.

6 ADC

The eQADC on the MPC5517G supports three additional external channel multiplexers. Therefore, support for the number of external channel multiplexers is increased from four to seven. The new ANR, ANS, and ANT channels are added to the AN16, AN17, and AN18 channels, respectively, and correspond to the channel numbers of 224-231, 232-239, and 240-247.

The external reference bypass capacitor on the MPC5517G can be connected and disconnected in software. This allows the ADC to be used without having to wait for the external reference bypass capacitor to fully recharge. The recovery time when waiting for the capacitor to recharge is 10 ms. This new feature allows the ADC to be used immediately after exit from low-power modes. It can also help to reduce overall power consumption as the 10 ms ADC recovery time is eliminated. However, without the bypass capacitor, the accuracy of the ADC is reduced.

The capacitor is connected and disconnected from within the CRP Status and Control Register (SOCSC). Setting the BYPDIS field disables the bypass capacitor, which is enabled by default from reset.

7 EBI

Several enhancements have been made to the external bus interface (EBI) on the MPC5517G.

To make interfacing to external memories feasible, an address latch enable signal (ALE) has been added to pin PF12. This provides the signal needed to control the address latches, to latch the address information on the bus at the correct time.

In 16-bit data port mode, non-multiplexed address signals are also present on the MPC5517G. The non-multiplexed address signals are address[8:15]. These address signals do not change state while the EBI access is in progress. Address[8:15] are multiplexed on the PF[2:9] pins.

The non-multiplexed range means that these address lines do not have to be latched by external hardware, thereby saving an additional address latch when addressing more than 16 (actually 17) address lines (128K)with 16-bit data port..

The EBI on the MPC5517G supports two additional chip selects, taking the total number of available chip selects to four. The additional chip selects are available on Port H: PH3 - CS[2] and PH2 - CS[3].

8 Real Time Clock (RTC) / Autonomous Periodic Interrupt (API)

The RTC on the MPC5517G will continue to run through reset, allowing a real time clock to be maintained through resets.

The RTC clock on the MPC5517G can be driven directly from the 16 MHz IRC. A 16 MHz IRC/512 bypass to RTC option has been added.

9 Number of DSPIs Increased from 3 to 4

Up to four DSPI modules are available on the MPC5517G.

DSPI D is present on selected Rev A devices, including the MPC5517, located at address 0xFFF9_C000. DSPI D supports all six chip selects, as well as serialization of eMIOS channels 0–15. (Note that no deserialization is supported on this DSPI.)

The pins used by DSPI D are listed below.

PC10 and PJ13 — SCK_D
PC11 and PJ14 — SOUT_D
PC12 and PJ15 — SIN_D
PC13 and PJ12 — PCS_D[0]
PC14 and PJ11 — PCS_D[1]
PC15 and PJ10 — PCS_D[2]
PD0 and PJ9 — PCS_D[3]
PD1 and PJ8 — PCS_D[4]
PD2 and PH12 — PCS_D[5]

The DMA multiplexer (DMA MUX) and Interrupt Controller have been updated to support the additional requests.

Interrupt Vectors:	279	DSPI_D.DSPI_ISR[TFUF] and DSPI_D.DSPI_ISR[RFOF] DSPI_D combined overrun interrupt request of the Transmit FIFO Underflow and Receive FIFO Overflow interrupt requests
	280	DSPI_D.DSPI_ISR[EOQF] DSPI_D transmit FIFO End Of Queue flag
	281	DSPI_D.DSPI_ISR[TFFF] DSPI_D Transmit FIFO Fill flag
	282	DSPI_D.DSPI_ISR[TCF] DSPI_D Transfer Complete flag
	283	DSPI_D.DSPI_ISR[RFDF] DSPI_D Receive FIFO Drain flag
DMA MUX:	0x17	DSPI_D.DSPI_SR[TFFF] DSPI_D transmit FIFO fill flag
	0x18	DSPI_D.DSPI_SR[RFDF] DSPI_D receive FIFO drain flag

10 Addition of FM Function to PLL

The PLL on the MPC5517G supports frequency modulation, and is hereafter known as the FMPLL. A frequency modulated PLL can help to reduce EMI emissions.

Modulation is applied as a triangular waveform and is programmable. Peak-to-peak register programmable modulation depths of 0.5%, 1%, 1.5%, and 2% of the system frequency are supported, along with modulation rates of $F_{extal}/80$, $F_{extal}/40$, and $F_{extal}/20$.

To use the FM feature, it must be enabled by configuring the modulation rate (ERATE) and depth (EDEPTH) fields in the FMPLL ESYNCR2 register. These fields are new on the MPC5517G to support the FM functionality.

11 Updated I^2C Module — Supports BIIE Interrupt

The updated I^2C module that is integrated into MPC5510 family Rev A devices support the Bus Idle Interrupt Enable function. On previous MPC5510 family devices, writing to the BIIE bit in the IBIC register has no effect and reading always returns 0.

12 Addition of SIU Test Lock Bit

Safety applications must prevent the occurrence of situations where the device may be locked up or unintentionally configured incorrectly. There are Freescale internal test features; the Test Lock bit ensures that they cannot be enabled unintentionally. Initialization code should set this bit. Once set, the Test Lock bit remains set until the next reset.

SIU_CCR[TESTLOCK] - Test Lock

0 - Internal test features can be enabled

1 - Internal test features cannot be enabled

The default reset state is 0 (reset with normal reset).

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: EB694
Rev. 0
05/2008

freescale™
semiconductor