Freescale Semiconductor
Engineering Bulletin

EB655
Rev. 1.00, 08/2005

MC3PHAC enable.asm Fault Modification

Problem

A customer has reported that in some instances when the fault input is asserted, the PWM outputs will be reactivated after the programmed restart timeout interval, even though the fault input is still asserted. This is a potentially serious condition that is in direct violation of the MC3PHAC spec, which indicates that the PWMs must remain off at all times while the fault input is asserted. The restart timeout interval should not be allowed to commence until the fault input is negated.

This change has been implemented on MC3PHAC devices with date codes of September 2005 and later. Please refer to product bulletin MC3PHACPB (on the MC3PHAC product page) from the Freescale Semiconductor website, http://freescale.com.

Code Analysis

The MC3PHAC code was inspected to determine whether a software explanation could be found for the aberrant behavior. A timing window bug was found in the enable.asm routine, and a scenario was identified that could reproduce the problem when noise exists on the fault input. The reporting customer claims there is no observable noise on their supplied fault signal, but stated that the incidence of occurrence of the problem was reduced significantly by filtering the fault input pin. The scenario is recreated in Figure 1.

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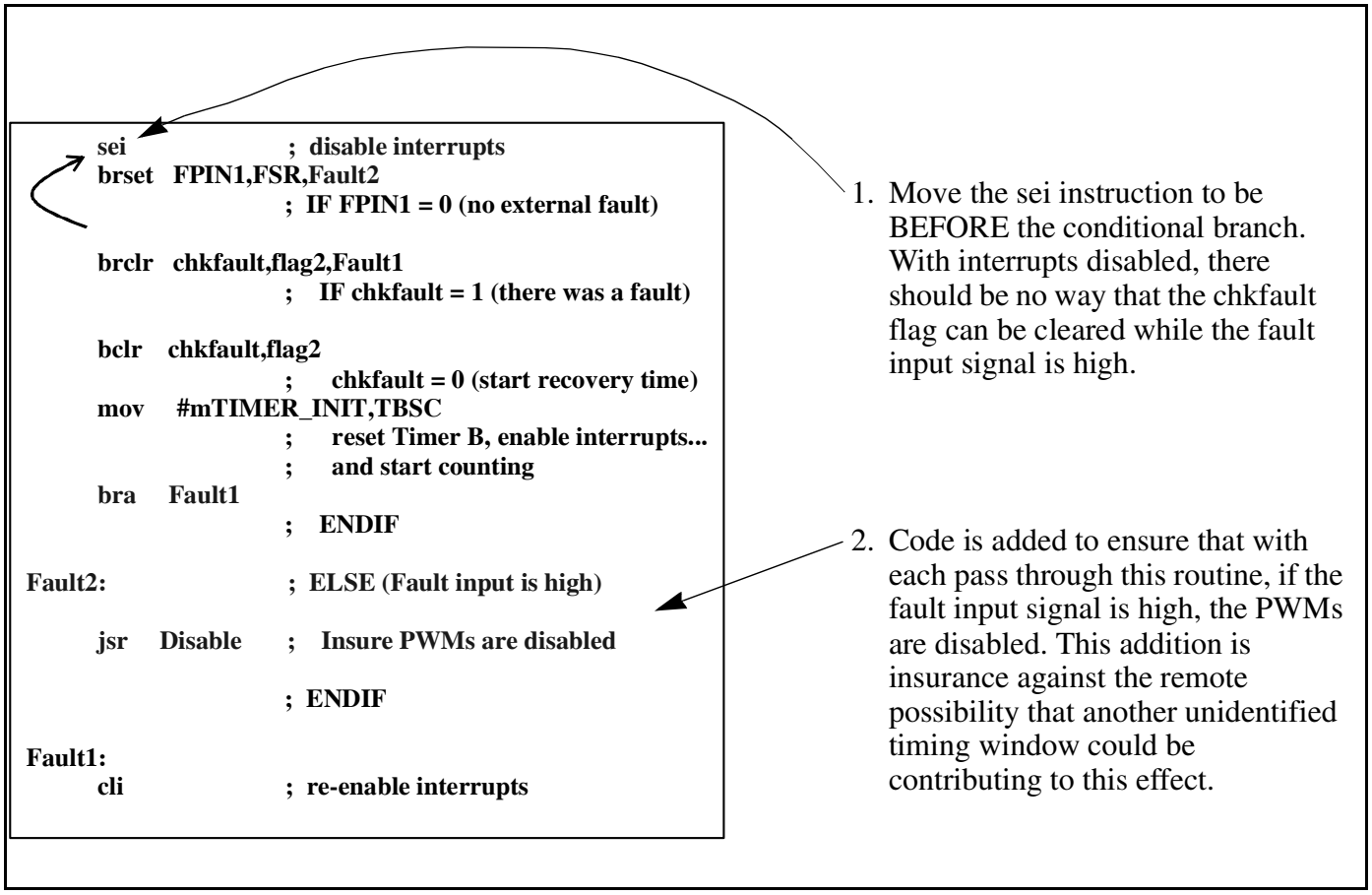
1. This is a segment of code from enable.asm, which is a background routine, with interrupts enabled. Assume that the fault pin was recently high (asserted), but now is low, indicating that the timeout interval may commence, inevitably resulting in the PWMs being reasserted.

```
      brset   FPIN1,FSR,Fault1
                        ;  IF FPIN1 = 0 (no external fault)
                  *** I N T E R R U P T ***
      sei               ;    disable interrupts
      brclr   chkfault,flag2,Fault1
                        ;    IF chkfault = 1 (there was a fault)

      bclr    chkfault,flag2
                        ;      chkfault = 0 (start recovery time)
      mov     #mTIMER_INIT,TBSC
                        ;      reset Timer B, enable interrupts...
                        ;      and start counting
                        ;    ENDIF
                        ;  ENDIF


Fault1:
      cli               ;  re-enable interrupts
```

2. Assume an interrupt occurs here (e.g., a PWM module interrupt, which occurs every 189 µs.)
3. During the time that the interrupt is being serviced, the fault input again goes high, and stays high. This generates a pending fault interrupt. When the fault ISR is executed, it sets the chkfault flag, indicating that a fault shutdown is in effect.
4. When execution is returned here, the routine shown will proceed to clear the chkfault flag (thinking that the fault input is low), which allows a timeout interval to commence, and eventually turn the PWMs back on.

Figure 1. Illustration of Timing Window Bug

Proposed Solution



Other Code Changes

The following changes were also made as part of the revision 1.1 upgrade:

- The header information associated with each file was modified to reflect the correct Freescale copyright declaration. The previous header information indicating that this code is “freeware” was removed.
- In the motor.s file, the revision text was changed from “ 1.0” to “ 1.1”.
- All changes associated with this revision were documented in the “readme.txt” file.

Software Testing

An MC3PHAC was programmed with revision 1.1 code and limited functional verification was performed. A motor was controlled using PC Master, and no problems were encountered. The fault pin was repeatedly asserted and negated and no problems were encountered.

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