NXP Semiconductors
Engineering Bulletin

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S32G3 NoC Recommendations

1. Introduction

Network-on-Chip (NoC) is an interconnect matrix that supports communication between various initiators and targets. In NoC interconnects, quality of service (QoS) is the statistical allocation of throughput and delay. It is defined in terms of bandwidth and latency to the transactions carried between the initiators and the targets.

This document provides the information about the mandatory NoC configuration to be applied over the chip default configurations for the S32G3 family of controllers. These configurations are based on the device validation, and are targeted to ensure bandwidth availability for all transactions on the NoC.

NOTE

This configuration is not applicable for S32G2 as it uses the default configuration.

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2. Programming new QoS settings

The default NoC setting is done in the NoC hardware design and is applied automatically from device reset. NXP mandates to overwrite these settings with the attached settings. These settings have gone through exhaustive testing during the validation of the device and have proven to be optimal for the part's intended target applications. Changes to these settings may result in degradation of system performance.

The attached settings should be written once after every reset and should be one of the first thing that the software needs to perform before there is any significant traffic on the NoC. Any of the available application cores (Cortex-A53® or M7®) can initiate these writes. Dynamic configuration of these parameters can cause system instabilities therefore these configuration parameters should not be altered after they are initially set.

Prerequisites for programming the updated QoS settings:

Software Resettable Domains RD1 and RD2 both should be out of reset, to write these settings to the desired register spaces. Failing to do so results in Hard-Fault because of the register inaccessibility.

Steps to program updated QoS settings:

1. Partition RD1 should be enabled for writing QoS configs for Cortex-A53 and partition RD2 should be enabled for writing QoS configs for Cortex-M7.

```
if (A53_0 == coreType)
{
    /*enable partition 1 in order to make all A53 flexNoc registers accessible */
    u8Status =  Bl_EnablePartition(PARTITION_1);
}

if (M7_0 == coreType)
{
    /* Keep track of the time needed to start domain control register */
    timeout  =  TIMEOUT_CNT_INIT_VALUE;

    /* Test to see if reset domain control register RD2 interface was not already enabled */
    regValue = ((IP_RDC->RD2_CTRL_REG) & RESET_RD2_CTRL_REG_RD2_INTERCONNECT_INTERFACE_DISABLE_MASK);

    if (regValue) /* not already enabled */
    {
        /* Unlock software reset domain control register RD2 for writing */
        IP_RDC->RD2_CTRL_REG = (IP_RDC->RD2_CTRL_REG | RESET_RD2_CTRL_REG_RD2_CTRL_UNLOCK_MASK);
```

2. These settings should be part of the Bootloader to make sure the settings are in effect before application starts using the NoC. Customers can use NXP's Example Bootloader from *Integration_Reference_Examples_S32G3_2022_12* release available on Flexera, for reference.

The config files *FlexNOC_Init.c* and *FlexNOC_Init.h* can be found in the folder: *<Installation_Directory>\Integration_Reference_Examples_S32G3_2022_12\code\framework\realtime\swc\bootloader\platforms\S32G3XX\src*

In addition, this document has the files attached for reference.

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