



# SC18IM704

UART to I<sup>2</sup>C-bus bridge

Rev. 1.0 — 22 September 2021

Product data sheet

## 1 General description

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SC18IM704 is designed to serve as an interface between the standard UART port of a microcontroller or microprocessor and the serial I<sup>2</sup>C-bus; this allows the microcontroller or microprocessor to communicate directly with other I<sup>2</sup>C-bus devices. SC18IM704 can operate as an I<sup>2</sup>C-bus controller. SC18IM704 controls all the I<sup>2</sup>C-bus specific sequences, protocol, arbitration and timing. The host communicates with SC18IM704 with ASCII messages protocol; this makes the control sequences from the host to SC18IM704 become very simple.

SC18IM704 is a functional replacement for SC18IM700 with exception of:

- New pinout
- GPIO no longer has quasi bidirectional mode
- Lower operating supply voltage level (1.71 V vs 2.4 V)
- Temperature range of -40 to +105 °C vs -40 to +85 °C
- Device is rotated 180 degrees in the tape pocket; pin 1 is now in Quadrant 1

## 2 Features and benefits

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- UART host interface
- I<sup>2</sup>C-bus controller
- Eight programmable I/O pins
- High-speed UART: baud rate up to 460.8 kbit/s
- Fast-mode I<sup>2</sup>C-bus: 375 kHz
- 256-byte TX FIFO
- 256-byte RX FIFO
- Programmable baud rate generator
- 1.71 V and 3.6 V operation
- Sleep mode (power-down)
- UART message format resembles I<sup>2</sup>C-bus transaction format
- I<sup>2</sup>C-bus controller functions
- Multi-controller capability
- 5 V tolerance on the input pins
- 8 N 1 UART format (8 data bits, no parity bit, 1 stop bit)
- ESD protection exceeds 2000 V HBM per JESD22-A114
- Latch-up testing is done to JEDEC Standard JESD78 that exceeds 100 mA
- Available in TSSOP16 package



### 3 Applications

- Enable I<sup>2</sup>C-bus controller support in a system
- I<sup>2</sup>C-bus instrumentation and control
- Industrial control
- Medical equipment
- Cellular telephones
- Handheld computers

### 4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
SC18IM704PW	18IM704	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm with 0.65 mm pitch	SOT403-1

#### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SC18IM704PW	SC18IM704PWJ	TSSOP16	REEL 13" Q1 *STANDARD MARK SMD NON DRY PACK <sup>[1]</sup>	2500	T <sub>amb</sub> = -40 °C to +105 °C

[1] Find packing information at [www.nxp.com/docs/en/packing/SOT403-1\\_118.pdf](http://www.nxp.com/docs/en/packing/SOT403-1_118.pdf)

### 5 Block diagram

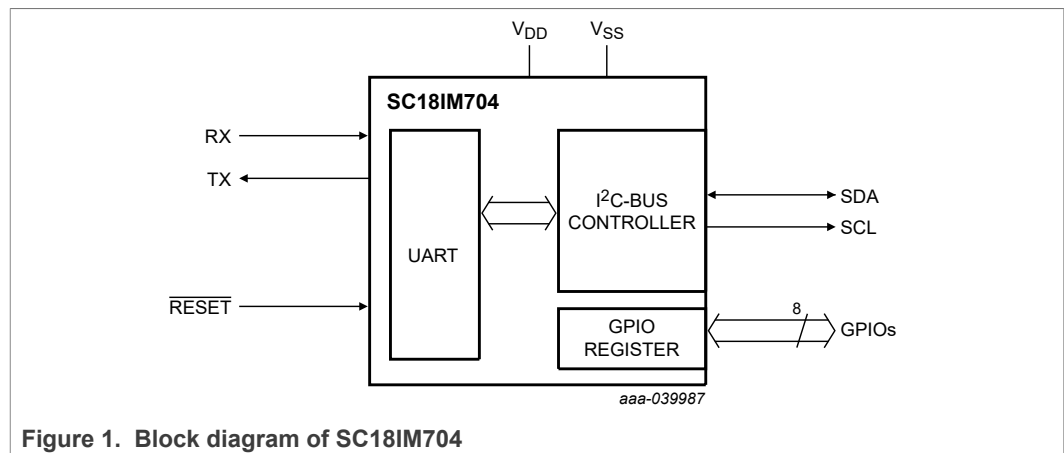


Figure 1. Block diagram of SC18IM704

## 6 Pinning information

### 6.1 Pinning

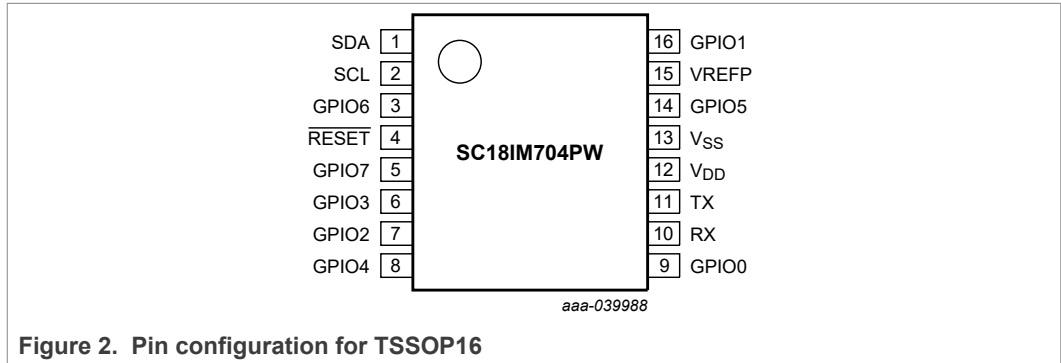


Figure 2. Pin configuration for TSSOP16

### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
GPIO0	9	I/O	programmable I/O pin
GPIO1	16	I/O	programmable I/O pin
RESET	4	I	hardware reset input
V <sub>SS</sub>	13	-	ground
GPIO2	7	I/O	programmable I/O pin
GPIO3	6	I/O	programmable I/O pin
SDA	1	I/O	I <sup>2</sup> C-bus data pin
SCL	2	O	I <sup>2</sup> C-bus clock output
RX	10	I	RS-232 receive input/Wake up. Device goes to Deep Power-down mode via the command 0x5A 0xA5 and exits the Deep Power-down mode when RX pin is driven LOW. A resistor must be connected between V <sub>DD</sub> and RX pin or the RX pin driven HIGH to remain in Deep Power-down mode.
TX	11	O	RS-232 transmit input
GPIO6	3	I/O	programmable I/O pin which must be pulled HIGH with resistor and must not be held LOW at power on or reset.
V <sub>DD</sub>	12	-	power supply
GPIO7	5	I/O	programmable I/O pin
GPIO5	14	I/O	programmable I/O pin
GPIO4	8	I/O	programmable I/O pin
VREFP	15	I	connect to V <sub>DD</sub>

## 7 Functional description

SC18IM704 is a bridge between a UART port and I<sup>2</sup>C-bus. The UART interface consists of a full-functional advanced UART. The UART communicates with the host through the TX and RX pins. The serial data format is fixed: one start bit, 8 data bits, and one stop bit. After reset the baud rate defaults to 9600 bit/s, and can be changed through the Baud Rate Generator (BRG) registers.

After a power-up sequence or a hardware reset, SC18IM704 will send two continuous bytes to the host to indicate a start-up condition. These two bytes are 0x4F and 0x4B; 'OK' in ASCII.

### 7.1 UART message format

The host initiates an I<sup>2</sup>C-bus data transfer, reads from and writes to SC18IM704 internal registers through a series of ASCII commands. [Table 4](#) lists the ASCII commands supported by SC18IM704, and also their hexadecimal value representation. Unrecognized commands are ignored by the device.

To prevent the host from handing SC18IM704 due to an unfinished command sequence, SC18IM704 has a time-out feature. The delay between any two bytes of data coming from the host should be less than 655 ms. If this condition is not met, SC18IM704 will time-out and clear the receive buffer. SC18IM704 then starts to wait for the next command from the host.

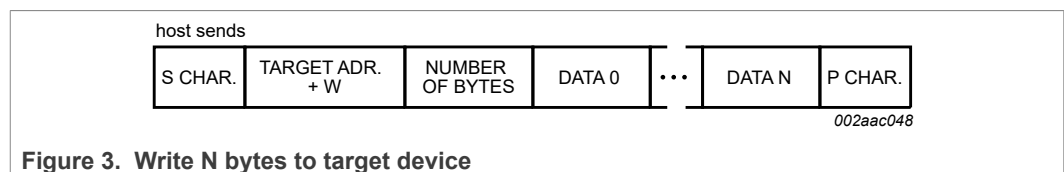
**Table 4. ASCII commands supported by SC18IM704**

ASCII command	Hex value	Command function
S	0x53	I <sup>2</sup> C-bus START
P	0x50	I <sup>2</sup> C-bus STOP
R	0x52	read SC18IM704 internal register
W	0x57	write to SC18IM704 internal register
I	0x49	read GPIO port
O	0x4F	write to GPIO port
Z	0x5A	power down

#### 7.1.1 Write N bytes to target device

The host issues the write command by sending an S character followed by an I<sup>2</sup>C-bus target device address, the total number of bytes to be sent, and I<sup>2</sup>C-bus data which begins with the first byte (DATA 0) and ends with the last byte (DATA N). The frame is then terminated with a P character. Once the host issues this command, SC18IM704 will access the I<sup>2</sup>C-bus target device and start sending the I<sup>2</sup>C-bus data bytes.

Note that the second byte sent is the I<sup>2</sup>C-bus device target address. The least significant bit (W) of this byte must be set to 0 to indicate this is an I<sup>2</sup>C-bus write command.



**Figure 3. Write N bytes to target device**

7.1.2 Read N byte from target device

The host issues the read command by sending an S character followed by an I<sup>2</sup>C-bus target device address, and the total number of bytes to be read from the addressed I<sup>2</sup>C-bus target. The frame is then terminated with a P character. Once the host issues this command, SC18IM704 will access the I<sup>2</sup>C-bus target device, get the correct number of bytes from the addressed I<sup>2</sup>C-bus target, and then return the data to the host.

Note that the second byte sent is the I<sup>2</sup>C-bus device target address. The least significant bit (R) of this byte must be set to 1 to indicate this is an I<sup>2</sup>C-bus write command.

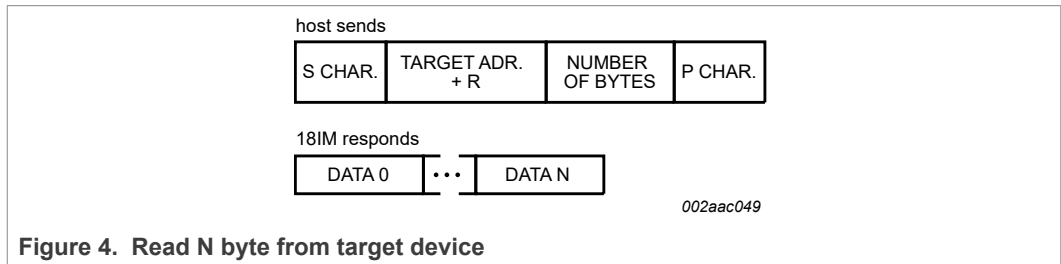


Figure 4. Read N byte from target device

7.1.3 Write to 18IM internal register

The host issues the internal register write command by sending a W character followed by the register and data pair. Each register to be written must be followed by the data byte. The frame is then terminated with a P character.

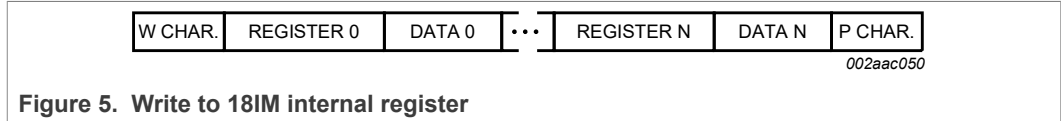


Figure 5. Write to 18IM internal register

**Remark:** Write and read from the internal 18IM register is processed immediately as soon as the intended register is determined by 18IM.

7.1.4 Read from 18IM internal register

The host issues the internal register read command by sending an R character followed by the registers to be read. The frame is then terminated with a P character.

Once the command is issued, SC18IM704 will access its internal registers and returns the contents of these registers to the host.

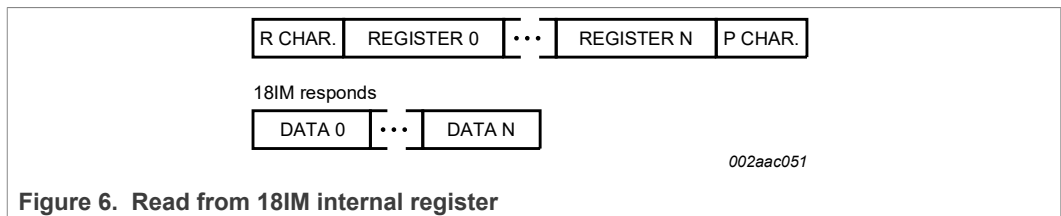


Figure 6. Read from 18IM internal register

7.1.5 Write to GPIO port

The host issues the output port write command by sending an O character followed by the data to be written to the output port. This command enables the host to quickly set

any GPIO pins programmed as output without having to write to SC18IM704 internal IOState register.

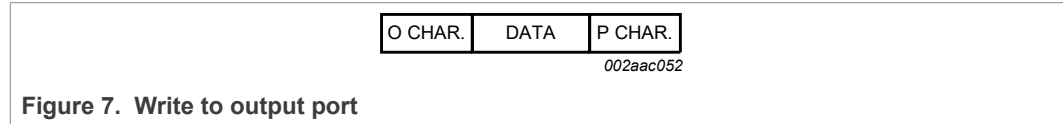


Figure 7. Write to output port

7.1.6 Read from GPIO port

The host issues the input port read command by sending an I character. This command enables the host to quickly read any GPIO pins programmed as input without having to read SC18IM704 internal IOState register.

Once the command is issued, SC18IM704 will read its internal IOState register and returns its content to the host.

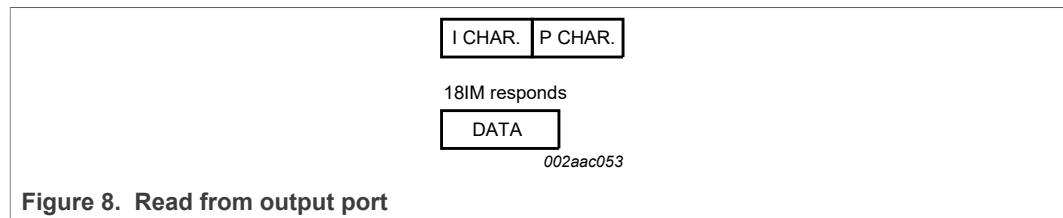


Figure 8. Read from output port

7.1.7 Repeated START: read after write

SC18IM704 also supports 'read after write' command as specified in the NXP Semiconductors I<sup>2</sup>C-bus specification. This allows a read command to be sent after a write command without having to issue a STOP condition between the two commands.

The host issues a write command as normal, then immediately issues a read command without sending a STOP (P) character after the write command.

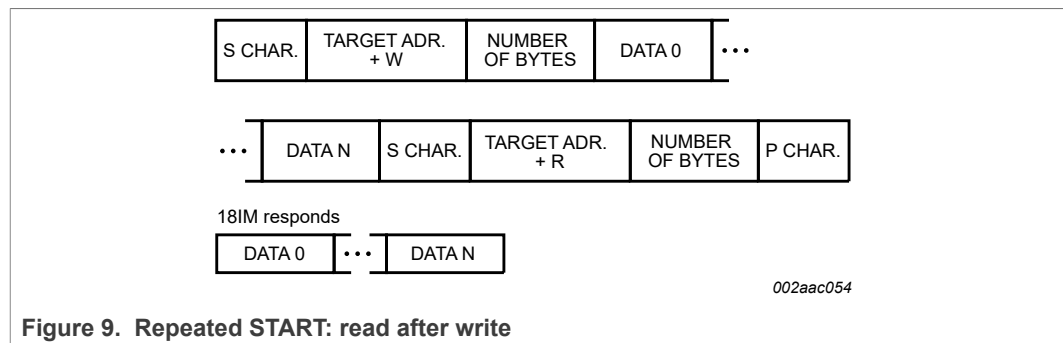


Figure 9. Repeated START: read after write

7.1.8 Repeated START: write after write

SC18IM704 also supports 'write after write' command as specified in the NXP Semiconductors I<sup>2</sup>C-bus specification. This allows a write command to be sent after a write command without having to issue a STOP condition between the two commands.

The host issues a write command as normal, then immediately issues a second write command without sending a STOP (P) character after the first write command.

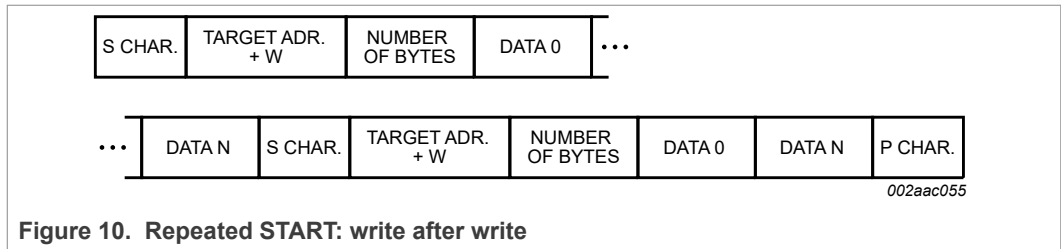


Figure 10. Repeated START: write after write

7.1.9 Power-down mode

SC18IM704 can be placed in a low-power mode. In this mode the internal oscillator is stopped and SC18IM704 will no longer respond to the host messages. Enter the Power-down mode by sending the power-down character Z (0x5A) followed by the two defined bytes, which are 0x5A and followed by 0xA5. If the exact message is not received, the device will not enter the power-down state.

Upon entering the power-down state, UART Rx pin is used to exit Deep Power-down mode. The bridge remains in the Deep Power-down mode as long as the Rx pin remains HIGH. Any character sent brings the bridge out of Deep Power-down mode but ignores the character.

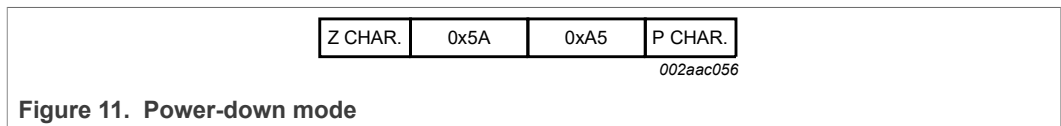


Figure 11. Power-down mode

7.1.10 Read version function ID

A read version command was included with SC18IM704 as a diagnostic tool when bringing up the bridge to verify communication. To retrieve the version, the host must send a ASCII 'V' followed by an ASCII 'P' character. The '704 will respond with a null terminated version string. An example response:

- 0x53 0x43 0x31 0x38 0x49 0x4D 0x37 0x30 0x34 0x20 0x31 0x2E0 0x30 0x2E 0x31 0x00

Which corresponds with the ascii string "SC18IM704 1.0.1".

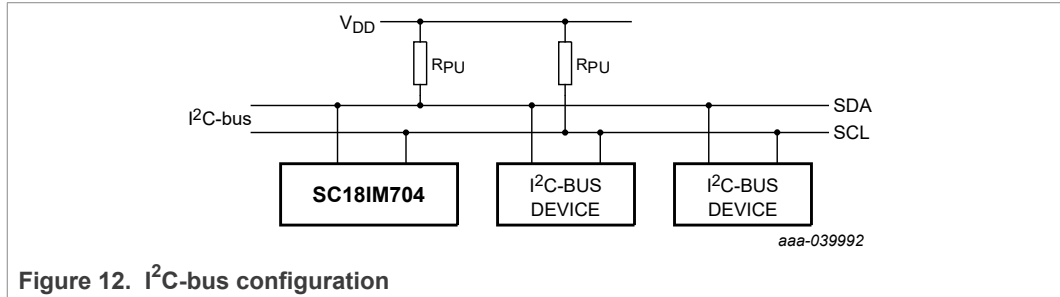
The response will always be 16 characters with the last character being a 0x00 null terminator.

8 I<sup>2</sup>C-bus serial interface

The I<sup>2</sup>C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between controllers and targets
- Multi-controller bus (no central controller)
- Arbitration between simultaneously transmitting controllers without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

A typical I<sup>2</sup>C-bus configuration is shown in [Figure 12](#). SC18IM704 device provides a byte-oriented I<sup>2</sup>C-bus interface that supports data transfers up to 400 kHz.



**Figure 12.** I<sup>2</sup>C-bus configuration



## 9 Internal registers available

### 9.1 Register summary

Table 5. Internal registers summary

Register address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Default value
General register set											
0x00	BRG0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	0xF0
0x01	BRG1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	0x02
0x02	PortConf1	GPIO3.1	GPIO3.0	GPIO2.1	GPIO2.0	GPIO1.1	GPIO1.0	GPIO0.1	GPIO0.0	R/W	0x55
0x03	PortConf2	GPIO7.1	GPIO7.0	GPIO6.1	GPIO6.0	GPIO5.1	GPIO5.0	GPIO4.1	GPIO4.0	R/W	0x55
0x04	IOState	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	R/W	- [1]
0x05	reserved	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	-	0x00
0x06	I2CAdr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	0x26
0x07	I2CClkL	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	0x13
0x08	I2CClkH	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	0x00
0x09	I2CTO	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TE	R/W	0x66
0x0A	I2CStat	1	1	1	1	I2CStat[3]	I2CStat[2]	I2CStat[1]	I2CStat[0]	R	0xF0

[1] Since the GPIO pins are configured as inputs after reset, the default value of this register depends on the states of the GPIO pins.

### 9.2 Register descriptions

#### 9.2.1 Baud Rate Generator (BRG)

The baud rate generator is an 8-bit counter that generates the data rate for the transmitter and the receiver. The rate is programmed through the BRG register and the baud rate can be calculated as follows:

$$Baudrate = \frac{7.3728 \times 10^6}{16 + (BRG1, BRG0)}$$

**Remark:** To calculate the baud rate the values in the BRG registers must first be converted from hex to decimal.

**Remark:** For the new baud rate to take effect, both BRG0 and BRG1 must be written in sequence (BRG0, BRG1) with new values. The new baud rate will be in effect once BRG1 is written.

#### 9.2.2 Programmable port configuration (PortConf1 and PortConf2)

GPIO port 0 to port 7 may be configured by software to one of three types. These are: push-pull, open-drain, and input-only. Two bits are used to select the desired configuration for each port pin. PortConf1 is used to select the configuration for GPIO3 to GPIO0, and PortConf2 is used to select the configuration for GPIO7 to GPIO4. A port pin has Schmitt triggered input that also has a glitch suppression circuit.

Table 6. Port configurations

GPIOn.1	GPIOn.0	Port configuration
0	0	input-only configuration
0	1	input-only configuration
1	0	push-pull output configuration
1	1	open-drain output configuration

9.2.2.1 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

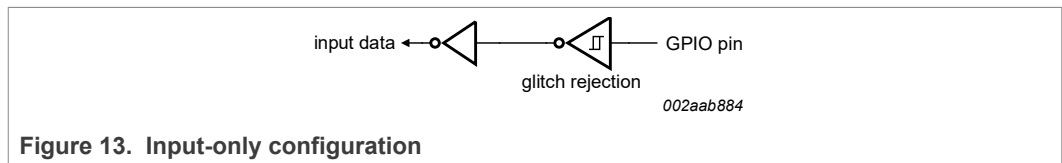


Figure 13. Input-only configuration

9.2.2.2 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

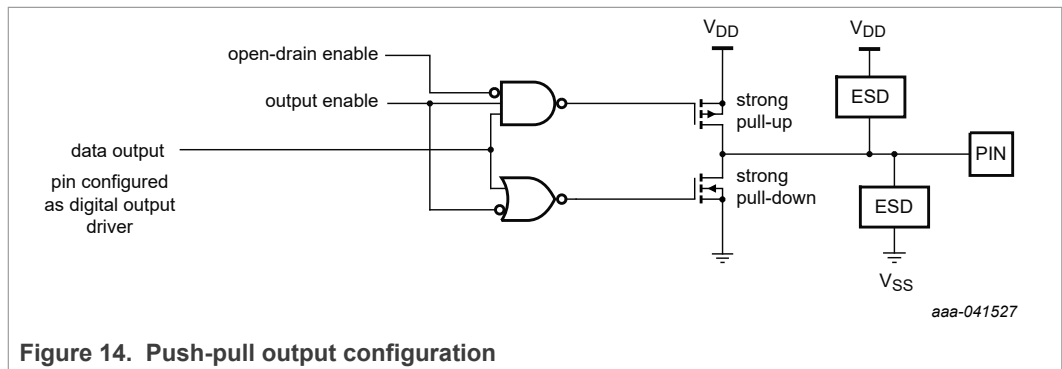


Figure 14. Push-pull output configuration

9.2.2.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V<sub>DD</sub>.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

Device uses a pseudo open-drain mode. The pin cannot be pulled up above V<sub>DD</sub>. The pins are not 5 V tolerant when V<sub>DD</sub> is grounded.

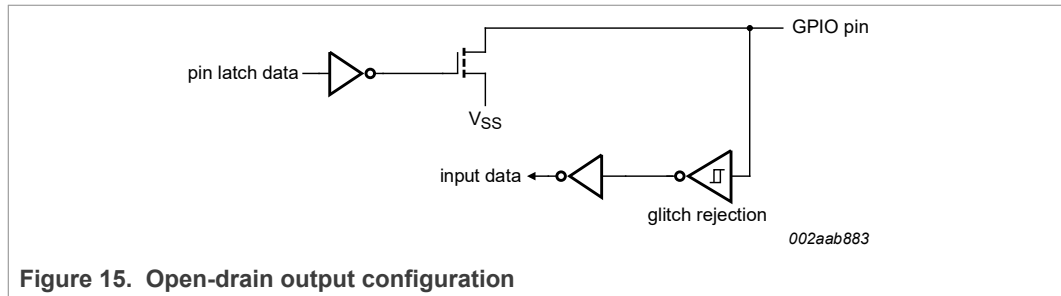


Figure 15. Open-drain output configuration

### 9.2.3 Programmable I/O pins state register (IOState)

When read, this register returns the actual state of all I/O pins. When written, each register bit will be transferred to the corresponding I/O pin programmed as output.

Table 7. IOState - Programmable I/O pins state register (address 0x04h) bit description

Bit	Symbol	Description
7:0	IOLevel	Set the logic level on the output pins. Write to this register: logic 0 = set output pin to zero logic 1 = set output pin to one Read this register returns states of all pins.

### 9.2.4 I<sup>2</sup>C-bus address register (I2CAdr)

The contents of the register represents the device’s own I<sup>2</sup>C-bus address. The most significant bit corresponds to the first bit received from the I<sup>2</sup>C-bus after a START condition. A logic 1 in I2CAdr corresponds to a HIGH level on the I<sup>2</sup>C-bus, and a logic 0 corresponds to a LOW level on the I<sup>2</sup>C-bus. The least significant bit is not used, but should be programmed with a ‘0’.

I2CAdr is not needed for device operation, but should be configured so that its address does not conflict with an I<sup>2</sup>C-bus device address used by the bus controller.

### 9.2.5 I<sup>2</sup>C-bus clock rates (I2CCLK)

This register determines the serial clock frequency. The various serial rates are shown in [Table 8](#). The frequency can be determined using the following formula:

$$I2C\text{-busclock freq} = \frac{15000000}{(8 \times I2CCLK)}$$

Table 8. I<sup>2</sup>C-bus clock frequency

I2CCLK (I2CCLKH + I2CCLKL)	I <sup>2</sup> C-bus clock frequency
5 (minimum)	375 kHz
7	268 kHz
9	208 kHz
19	99 kHz

Table 8. I<sup>2</sup>C-bus clock frequency...continued

I2CClk (I2CClKH + I2CClKL)	I <sup>2</sup> C-bus clock frequency
255	7.4 kHz

**Remark:** I2CClk is the 16-bit number formed by I2CClKH : I2CClKL.

**Caution:** The upper 8-bit portion will rarely be used as the I2C baud rate will be very slow.

### 9.2.6 I<sup>2</sup>C-bus time-out (I2CTO)

The time-out register is used to determine the maximum time that SCL is allowed to be LOW before the I<sup>2</sup>C-bus state machine is reset.

When the I<sup>2</sup>C-bus interface is running, I2CTO is loaded after each I<sup>2</sup>C-bus state transition.

Table 9. I2CTO - I<sup>2</sup>C-bus time-out register (address 0x09h) bit description

Bit	Symbol	Description
7:1	TO[7:1]	time-out value
0	TE	enable/disable time-out function logic 0 = disable logic 1 = enable

The least significant bit of I2CTO (TE bit) is used as a time-out enable/disable. A logic 1 will enable the time-out function. The time-out period can be calculated as follows:

$$timeout\ period = \frac{I2CClock+1}{1500000} \times ((1 + I2CTO[7:1]) \times 512) seconds$$

The time-out value may vary, and it is an approximate value.

I2CClock is the register value from [Section 9.2.5 "I2C-bus clock rates \(I2CClk\)"](#).

### 9.2.7 I<sup>2</sup>C-bus status register (I2CStat)

This register reports the I<sup>2</sup>C-bus transmit and receive frame status, whether the frame transmits correctly or not.

Table 10. I<sup>2</sup>C-bus status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I <sup>2</sup> C-bus status description
1	1	1	1	0	0	0	0	I2C_OK
1	1	1	1	0	0	0	1	I2C_NACK_ON_ADDRESS
1	1	1	1	0	0	1	0	I2C_NACK_ON_DATA
1	1	1	1	1	0	0	0	I2C_TIME_OUT

## 10 Limiting values

**Table 11. Limiting values**
*In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1] [2]</sup>*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+4.6	V
T <sub>amb(bias)</sub>	bias ambient temperature		-55	+150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C
V <sub>I</sub>	input voltage	5 V tolerant I/O pins; V <sub>DD</sub> ≥ 1.71 V	<sup>[3]</sup> <sup>[4]</sup> -0.5	+5.4	V
		3 V tolerant I/O - all pins	<sup>[5]</sup> -0.5	+3.6	V
I <sub>OH(I/O)</sub>	HIGH-level output current per input/output pin				
		GPIO3 to GPIO7	-	20	mA
		all other pins	-	8	mA
I <sub>OL(I/O)</sub>	LOW-level output current per input/output pin		-	20	mA
I <sub>I/O(tot)(max)</sub>	maximum total I/O current		-	120	mA
P <sub>tot/pack</sub>	total power dissipation per package		<sup>[6]</sup> -	1.5	W

[1] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

[2] Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V<sub>SS</sub> unless otherwise noted.

[3] Applies to all 5 V tolerant I/O pins except the 3 V tolerant pin GPIO5

[4] Including the voltage on outputs in 3-state mode.

[5] V<sub>DD</sub> present or not present.

[6] Based on package heat transfer, not device power consumption.

## 11 Static characteristics

**Table 12. Static characteristics**
*V<sub>DD</sub> = 1.71 V to 3.6 V; T<sub>amb</sub> = -40 °C to +105 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>DD</sub>	supply voltage		1.71		3.6	V
I <sub>DD</sub>	supply current	V <sub>DD</sub> = 3.3 V				
		Operating mode	-	2.1	4.0	mA
		Idle mode	-	1.3	3.4	mA
I <sub>DD(tpd)</sub>	total Power-down mode supply current	V <sub>DD</sub> = 3.3 V	-	6	75	μA
V <sub>POR</sub>	power-on reset voltage		-	-	0.2	V
V <sub>th(HL)</sub>	negative-going threshold voltage	except SCL, SDA	0.22V <sub>DD</sub>	0.4V <sub>DD</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	SCL, SDA only	-0.5	-	0.3V <sub>DD</sub>	V

**Table 12. Static characteristics...continued**

$V_{DD} = 1.71\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{th(LH)}$	positive-going threshold voltage	except SCL, SDA	-	$0.6V_{DD}$	$0.7V_{DD}$	V
$V_{IH}$	HIGH-level input voltage	SCL, SDA only	<sup>[2]</sup> $0.7V_{DD}$	-	5.4	V
$V_{OL}$	LOW-level output voltage	$I_{OL} = 4\text{ mA}$ ; $2.5\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	-	0.5	V
		$I_{OL} = 3\text{ mA}$ ; $1.71\text{ V} \leq V_{DD} \leq 2.5\text{ V}$	-	-	0.5	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 4\text{ mA}$ ; $2.5\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	$V_{DD} - 0.4$	-	-	V
		$I_{OH} = 3\text{ mA}$ ; $1.71\text{ V} \leq V_{DD} \leq 2.5\text{ V}$	$V_{DD} - 0.5$	-	-	V
$C_{io}$	input/output capacitance		<sup>[3]</sup> -	-	15	pF
$I_{IL}$	LOW-level input current	logic 0; all ports; $V_I = 0.4\text{ V}$	-	-	-80	$\mu\text{A}$
$I_{LI}$	input leakage current	all ports; $V_I = V_{IL}$ or $V_{IH}$	<sup>[4]</sup> -	-	-10	$\mu\text{A}$
$I_{T(HL)}$	negative-going transition current	logic 1-to-0; all ports; $V_I = 2.0\text{ V}$ at $V_{DD} = 3.6\text{ V}$	-30	-	-450	$\mu\text{A}$
$I_{pu}$	pull-up current	$V_I = 0\text{ V}$ ;	<sup>[5]</sup>			$\mu\text{A}$
		$2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	10	50	90	$\mu\text{A}$
		$1.71\text{ V} \leq V_{DD} \leq 2.0\text{ V}$	7	50	85	$\mu\text{A}$
		$V_{DD} < V_I < 5\text{ V}$	0	0	0	$\mu\text{A}$

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2]  $V_{DD} \geq 1.71\text{ V}$ ; otherwise limited to 3.6 V max when  $V_{DD} = 0\text{ V}$

[3] Pin capacitance is characterized but not tested.

[4] Measured with pins in high-impedance mode.

[5] Pull-up current measured across the weak pull-up resistor

## 12 Dynamic characteristics

**Table 13. I<sup>2</sup>C-bus timing characteristics**

All the timing limits are valid within the operating supply voltage and ambient temperature range;  $V_{DD} = 1.71\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ ; and refer to  $V_{IL}$  and  $V_{IH}$  with an input voltage of  $V_{SS}$  to  $V_{DD}$ .

Symbol	Parameter	Conditions	Standard mode I <sup>2</sup> C-bus		Fast mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
$f_{SCL}$	SCL clock frequency		0	100	0	400	kHz
$t_{BUF}$	bus free time between a STOP and START condition		4.7	-	1.3	-	$\mu\text{s}$
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	$\mu\text{s}$
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	$\mu\text{s}$
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	$\mu\text{s}$
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time		-	0.6	-	0.6	$\mu\text{s}$
$t_{VD;DAT}$	data valid time	LOW-level	-	0.6	-	0.6	$\mu\text{s}$
		HIGH-level	-	0.6	-	0.6	$\mu\text{s}$

Table 13. I<sup>2</sup>C-bus timing characteristics...continued

All the timing limits are valid within the operating supply voltage and ambient temperature range;  $V_{DD} = 1.71\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+105\text{ °C}$ ; and refer to  $V_{IL}$  and  $V_{IH}$  with an input voltage of  $V_{SS}$  to  $V_{DD}$ .

Symbol	Parameter	Conditions	Standard mode I <sup>2</sup> C-bus		Fast mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{LOW}$	LOW period of the SCL clock		4.7	-	1.3	-	µs
$t_{HIGH}$	HIGH period of the SCL clock		4.0	-	0.6	-	µs
$t_f$	fall time of both SDA and SCL signals		-	0.3	-	0.3	µs
$t_r$	rise time of both SDA and SCL signals		-	1	-	0.3	µs
$t_{SP}$	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns

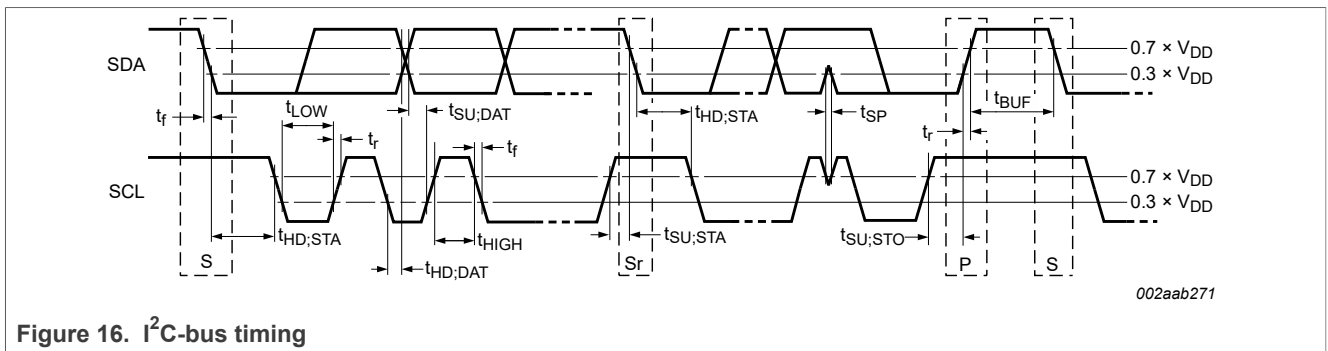


Figure 16. I<sup>2</sup>C-bus timing

Table 14. USART dynamic characteristics

$T_{amb} = -40\text{ °C to }105\text{ °C}$ ;  $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  unless noted otherwise;  $C_L = 10\text{ pF}$ ; input slew = 10 ns. Simulated parameters sampled at the 30%/70% level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
<b>USART target (in synchronous mode)</b>					
$t_{su(D)}$	data input set-up time	$3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	8	-	ns
		$1.71\text{ V} \leq V_{DD} < 3.0\text{ V}$	3	-	ns
$t_{h(D)}$	data input hold time	$3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	10	-	ns
		$1.71\text{ V} \leq V_{DD} < 3.0\text{ V}$	5	-	ns
$t_{v(Q)}$	data output valid time	$3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	0	39	ns
		$1.71\text{ V} \leq V_{DD} < 3.0\text{ V}$	0	42	ns

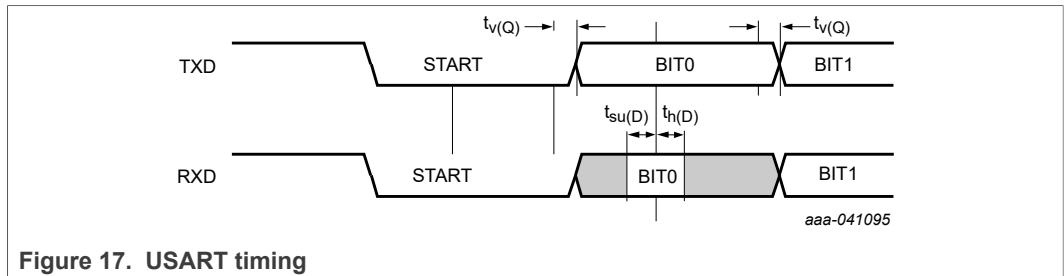


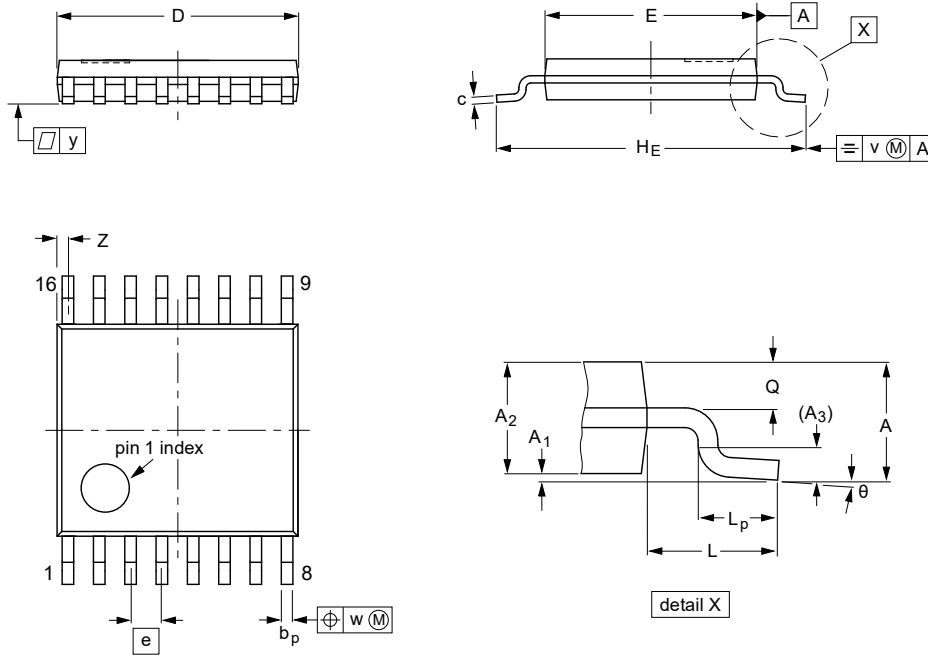
Figure 17. USART timing



13 Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18

Figure 18. Package outline SOT403-1 (TSSOP16)

14 PCB layout

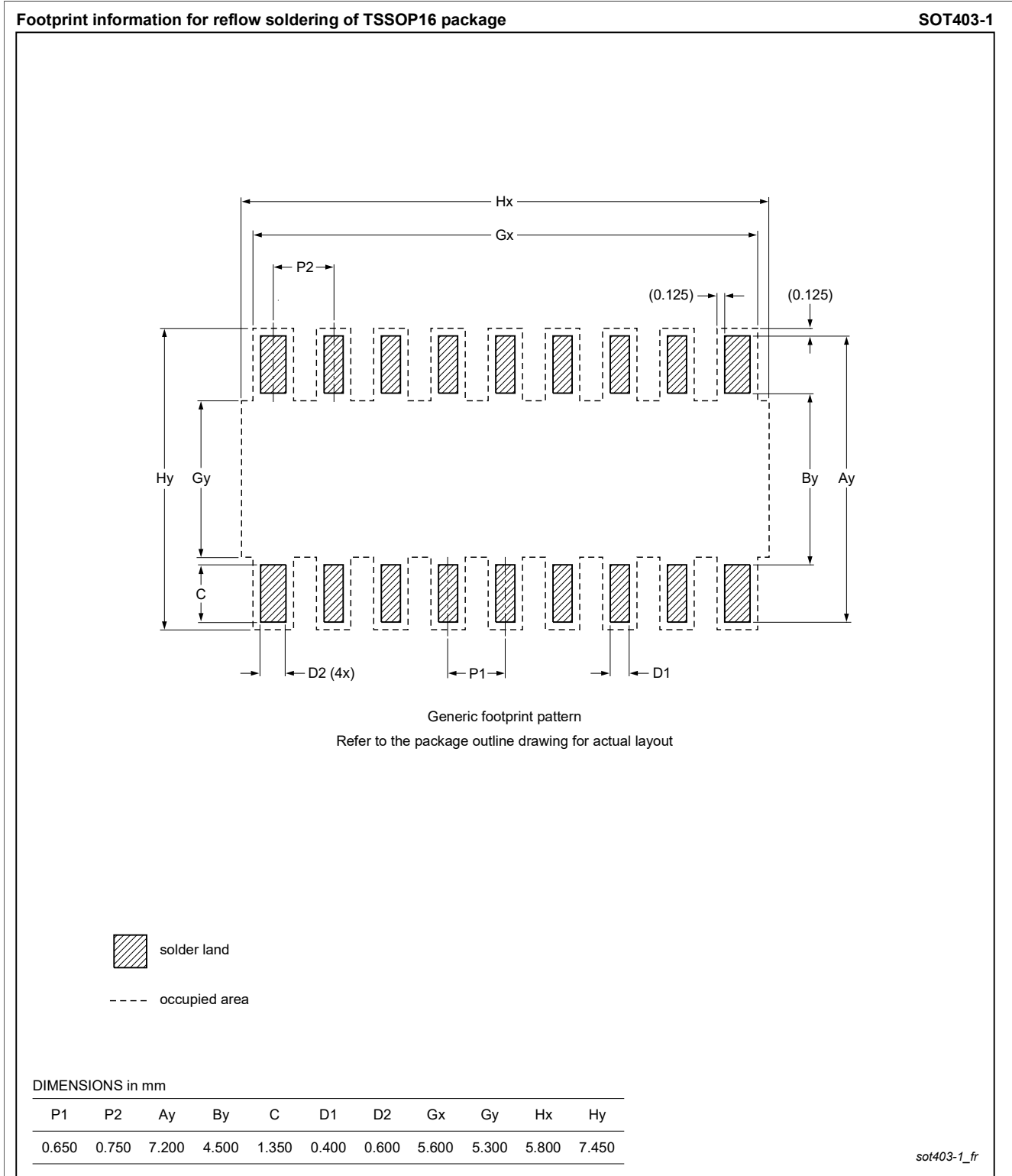
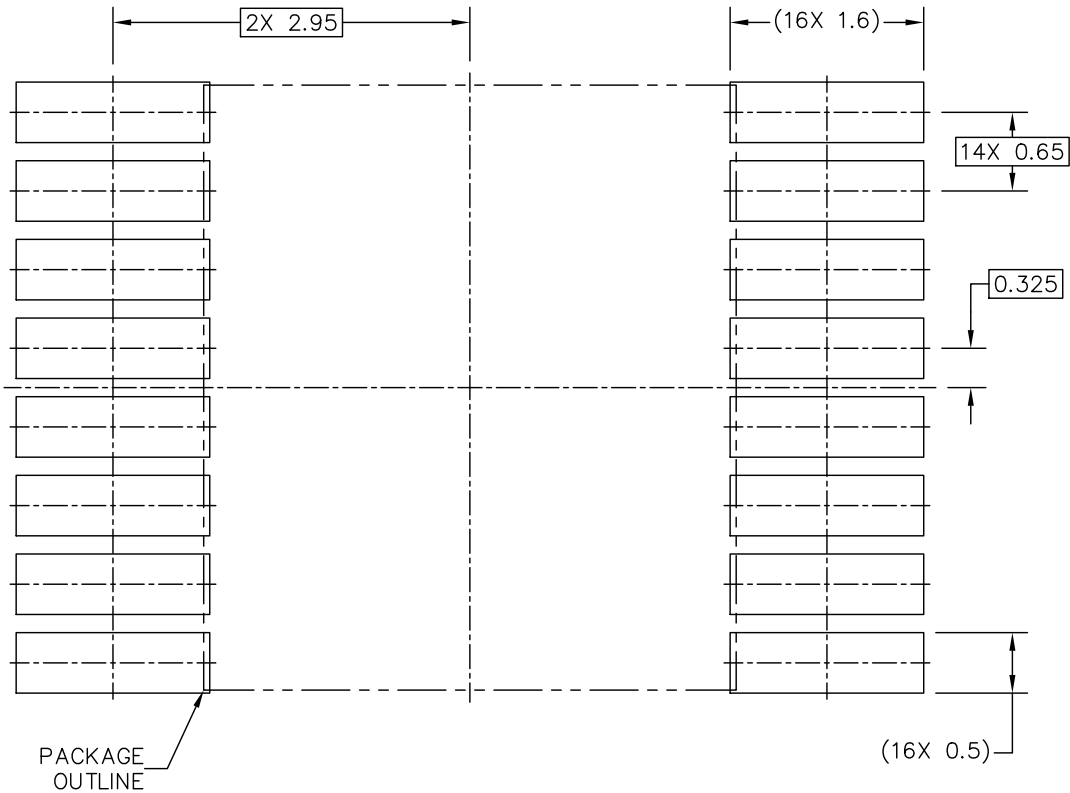


Figure 19. SOT403-1 (TSSOP16) footprint information for reflow soldering

PDSO-G-16 I/O  
4.4 X 5 X 1.1 PKG, 0.65 PITCH

SOT403-1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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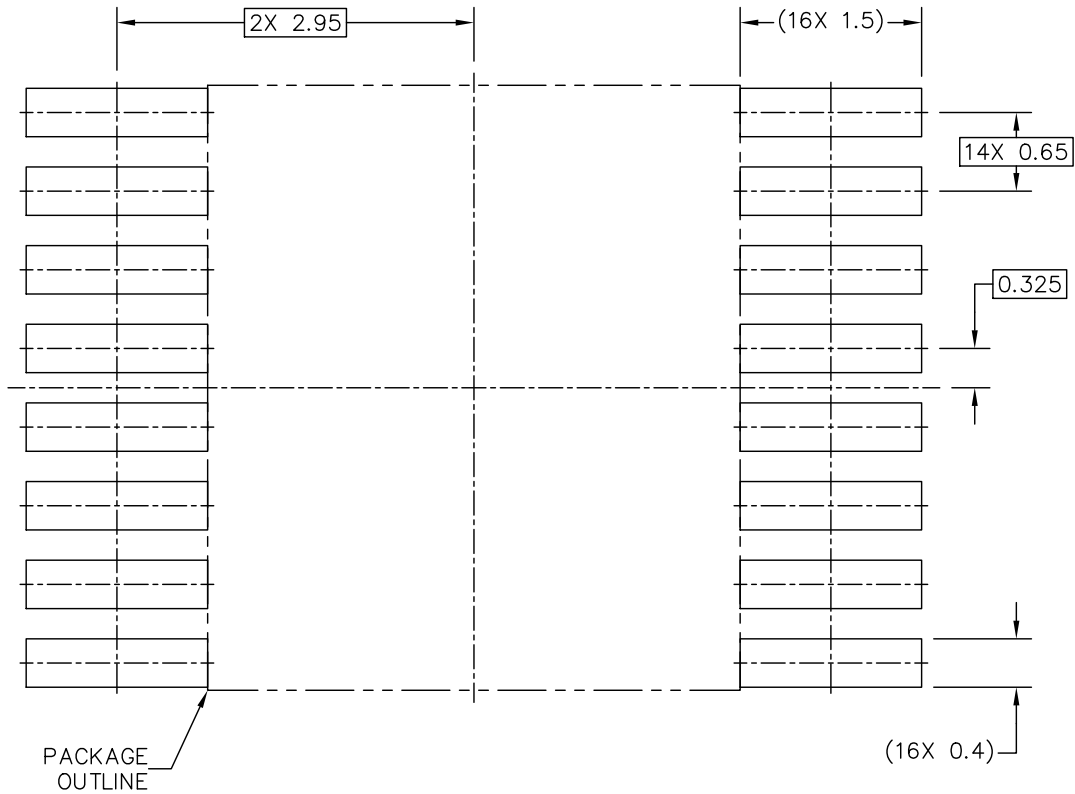
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Figure 20. SOT403-1 (TSSOP16) solder mask opening pattern

PDSO-G-16 I/O  
4.4 X 5 X 1.1 PKG, 0.65 PITCH

SOT403-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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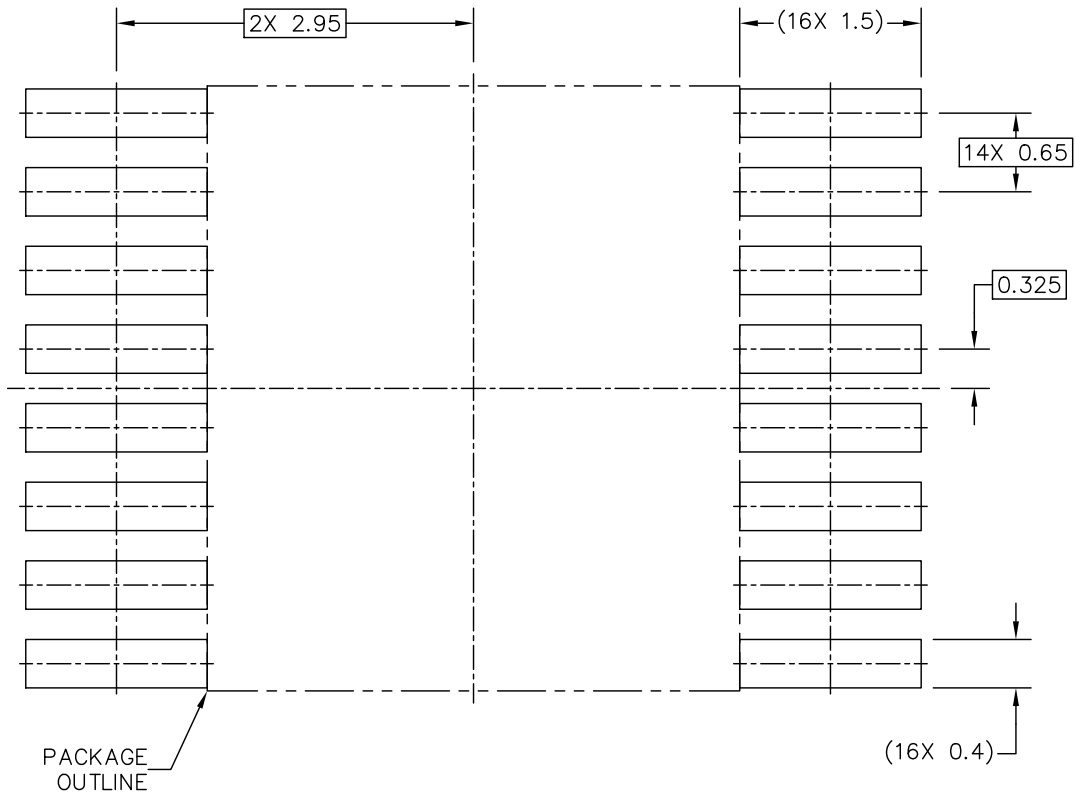
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Figure 21. SOT403-1 (TSSOP16) I/O pads and solderable area

PDSO-G-16 I/O  
4.4 X 5 X 1.1 PKG, 0.65 PITCH

SOT403-1



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 22. SOT403-1 (TSSOP16) Solder paste stencil

## 15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 23](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 15](#) and [Table 16](#)

**Table 15. SnPb eutectic process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 16. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 23](#).

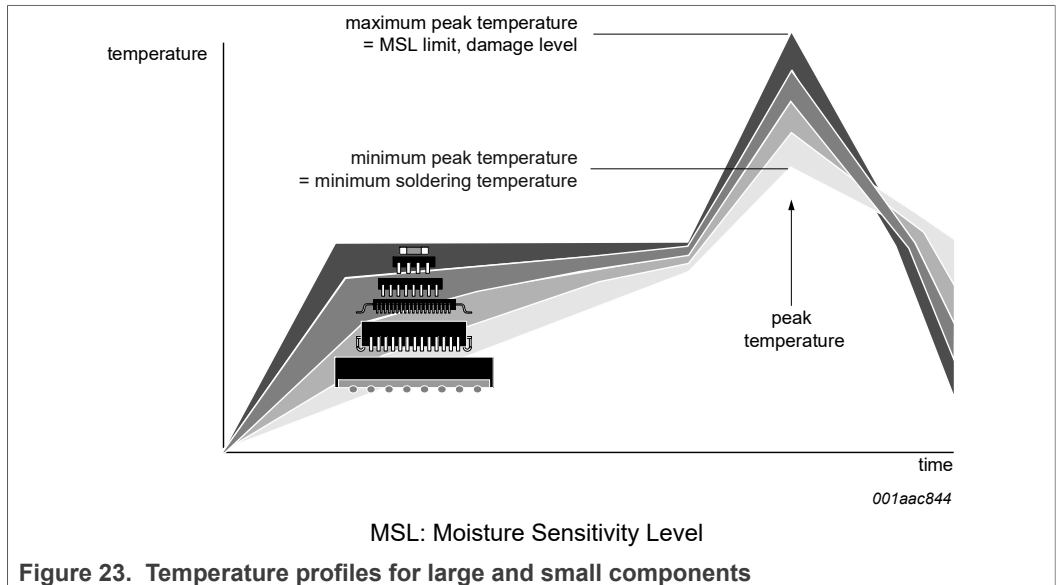


Figure 23. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 16 Abbreviations

Table 17. Abbreviations

Acronym	Description
ASCII	American Standard Code for Information Interchange
FIFO	First In, First Out
GPIO	General Purpose Input/Output
I <sup>2</sup> C-bus	Inter Integrated Circuit bus
RX FIFO	Receive FIFO
TX FIFO	Transmit FIFO
UART	Universal Asynchronous Receiver/Transmitter

## 17 Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SC18IM704 v.1.0	20210922	Product data sheet	-	-



## 18 Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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