NXP Semiconductors
Data Sheet: Technical Data

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RF112

RF112 Transceiver Data Sheet

Features

- Zero I/F operation in 2.4GHz (2.4-2.5GHz) Low and 5GHz (4.9-6GHz) High Industrial, Scientific, and Medical (ISM) Bands
  - Three independently operating RF sub-systems.
  - One dual band 1x2 MIMO transceiver, TRX
  - One dual band observation receiver, RO1
  - One high band observation receiver, RO2
  - Aggregate support for 1x Transmit, 4x Receive antenna operation
- Receiver features
  - Direct conversion, low noise and high dynamic range receive chain
  - High speed AGC interface (RSSI detector and RX gain control) to baseband
  - Analog baseband filters (20, 40 and 80 MHz modulation bandwidth) with on-chip calibration
  - Analog differential I/Q interface to baseband IC
- Transmitter features
  - Direct conversion with adjustable gain transmit chain
  - Analog baseband filter (20, 40 and 80 MHz modulation bandwidth) with on-chip calibration
  - Analog differential I/Q interface to baseband
- Flexible frequency generation system
  - 40 MHz crystal or external oscillator for frequency reference
  - Adjustable crystal load to tune for minimum frequency error
  - 4X multiplied input reference that can be routed to an output differential pair to be used as a low jitter 160 MHz reference by other devices in the system
  - Independent synthesizers for each sub-system driven by a common reference
- Two interfaces for configuration and bi-directional data exchanges with the baseband IC
  - A low complexity high-speed custom LVDS bus (LLCP)
  - A traditional low-speed I2C bus
- Programmable digital core for transceiver control and calibration
- Auxiliary ADC support for calibration and external functions (voltage and temperature measurements)
- 64 pin QFN package

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1 Introduction

The purpose and scope of this document is to provide the specifications for the RF112 1x4 ISM transceiver.

The RF112 Transceiver consists of three RF sub-systems; one dual band 1x2 MIMO transceiver, denoted TRX, one dual band observation receiver, denoted RO1, and one high band observation receiver, denoted RO2, together with a crystal oscillator and a digital core which is used to control the transceiver, and interfaces. The TRX, RO1, and RO2 sub-systems operate independently. The dual band units can be configured to work in either low band or high band, but since they share synthesizer, channel filters and analog baseband interfaces the bands cannot be used concurrently.

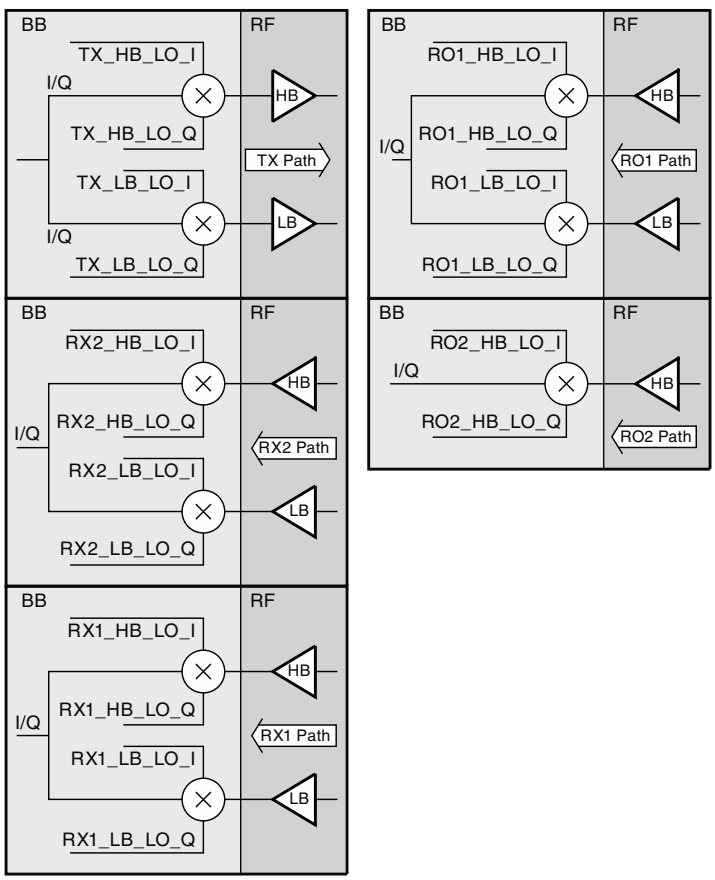


Figure 1. RF112 Transceiver Simplified model

The RF112 Transceiver uses a direct conversion architecture for both RX and TX. The chip has independent synthesizers for each sub-system driven from a common reference. The frequency reference can be a 40 MHz crystal or external oscillator. The input reference is multiplied internally by 4 and can be routed to an output differential driver for use as a low jitter 160 MHz frequency reference by other devices in the system. The

gain in receive mode should be controlled by the baseband IC. The receive chain has low noise and high dynamic range. The analog baseband filters have on-chip calibration and supports 20, 40, or 80 MHz modulation bandwidth. An internal crystal oscillator is implemented to enable usage of a low cost crystal. The reference frequency can be fine-tuned to minimize the frequency error. A LVDS clock output is included to provide a reference clock to the baseband chip. An auxiliary ADC is implemented for calibration purposes and to serve various external functions like power and temperature measurements.

The two interfaces, a traditional low-speed I2C, and a low complexity high-speed custom LVDS buses are available for configuration and bi-directional data exchanges with the baseband. The high-speed LLCP interface can be used to provide a continuous stream of RF envelope detector samples after the LNA in each receiver chain. This allows the receiver AGC algorithm, located on the baseband chip, to observe the wideband signal level and optimize the receiver gain for best performance. The interface allows quick updates of the transmitter and receiver gains.

This figure shows top level block diagram of the RF112 Transceiver.

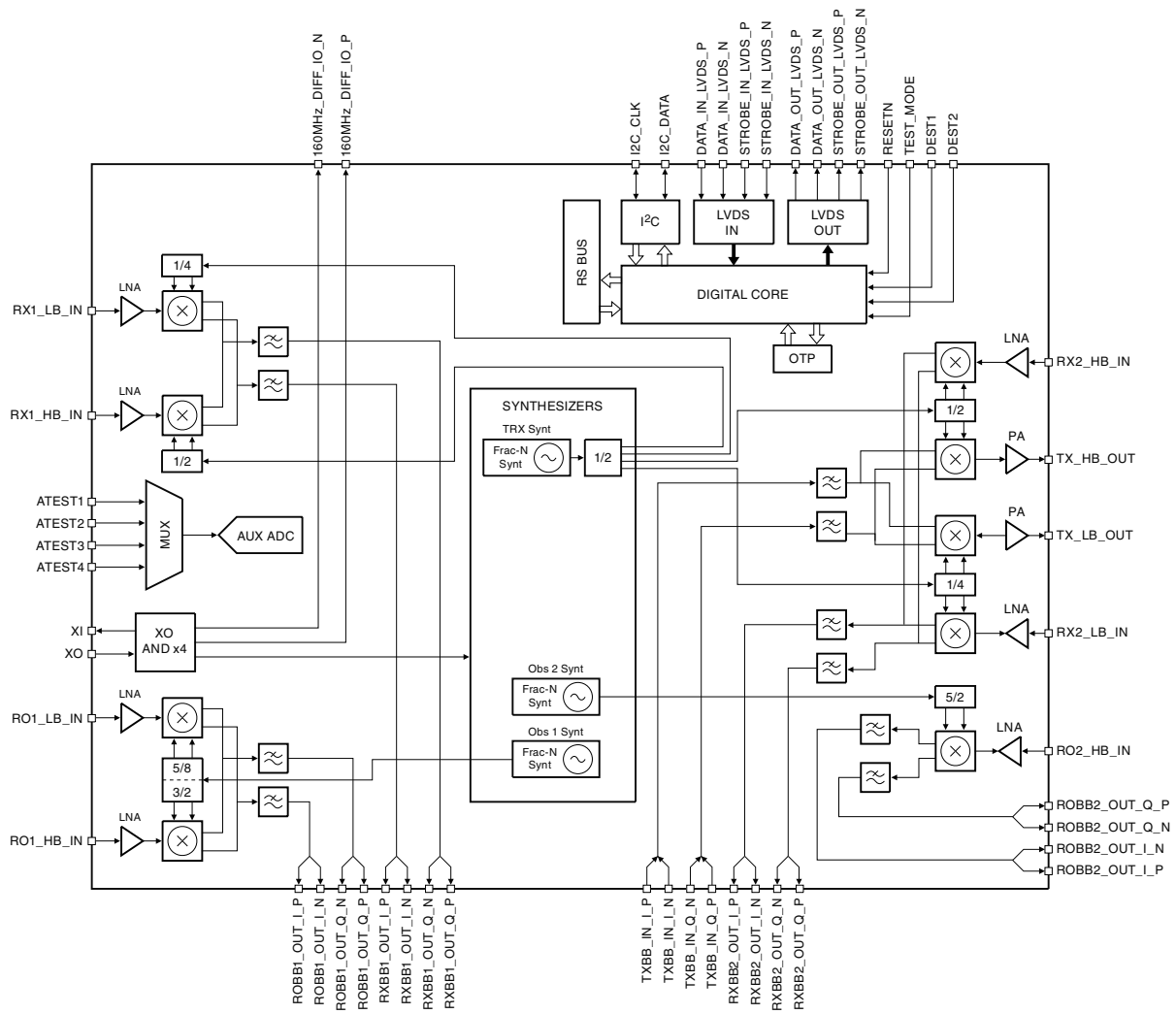


Figure 2. RF112 Transceiver block diagram

The TRX sub-system is capable of operating in TDD mode in either high band or low band. The TRX consists of one high band transceiver and one low band transceiver which share baseband filters and analog interfaces. The transceivers each have one transmitter and two identical receivers, the transmitter and one of the receivers share the same LO, the second receiver LO-phases are generated independently from the same synthesizer as the transmit-receive-pair. The LO generation for the TRX sub-system is kept running all the time, to keep the LO-phase relations fixed after chip power-on.

The observation receiver chains are identical to the main receive chains, but they have their own completely independent synthesizers. The two RO1 receivers (LB and HB) share synthesizer and baseband, and can, hence, not be used concurrently. The observation receiver synthesizers are kept running all the time.

The TRX receivers and the two observation receivers can be run at exactly the same LO frequency, so that the transceiver can be used in 1x3 Low Band or 1x4 MIMO High Band configuration, but with reduced performance.

The analog filter bandwidths of the two TRX receivers are always the same. However, the bandwidth selection of the receivers and transmitters are completely independent. The bandwidth setting of the observation receivers are independent of both the TRX receivers and transmitters and of the other observation receiver.

Below is the RF112 block diagram of the Transceiver digital controller:

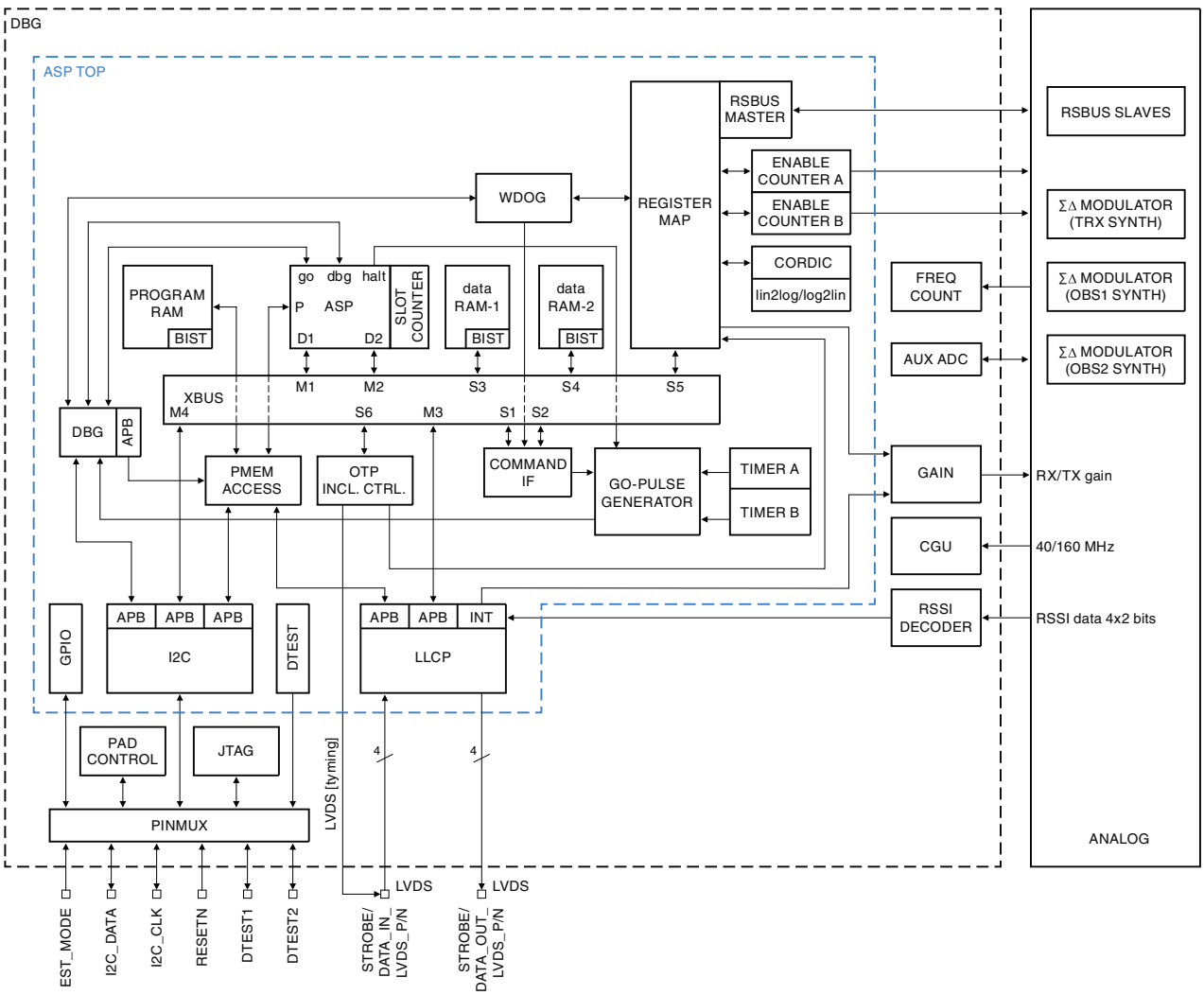


Figure 3. RF112 Digital Block Diagram

The digital part of RF112 consists of an ASP and a number of digital hardware blocks, and interfaces both with the analogue part - via an RS bus, signals, and clocks - and with the outside world - via LLCP and I2C interfaces. The internal clock frequency is 160 MHz in normal operation, during boot a 40 MHz clock is used. The digital part is used to control and calibrate the analog part of the chip, both RF and baseband signal interfaces are analog.

2 Pin assignments

2.1 RF112 transceiver QFN layout diagrams

This figure shows the complete view of the RF112 QFN diagram.

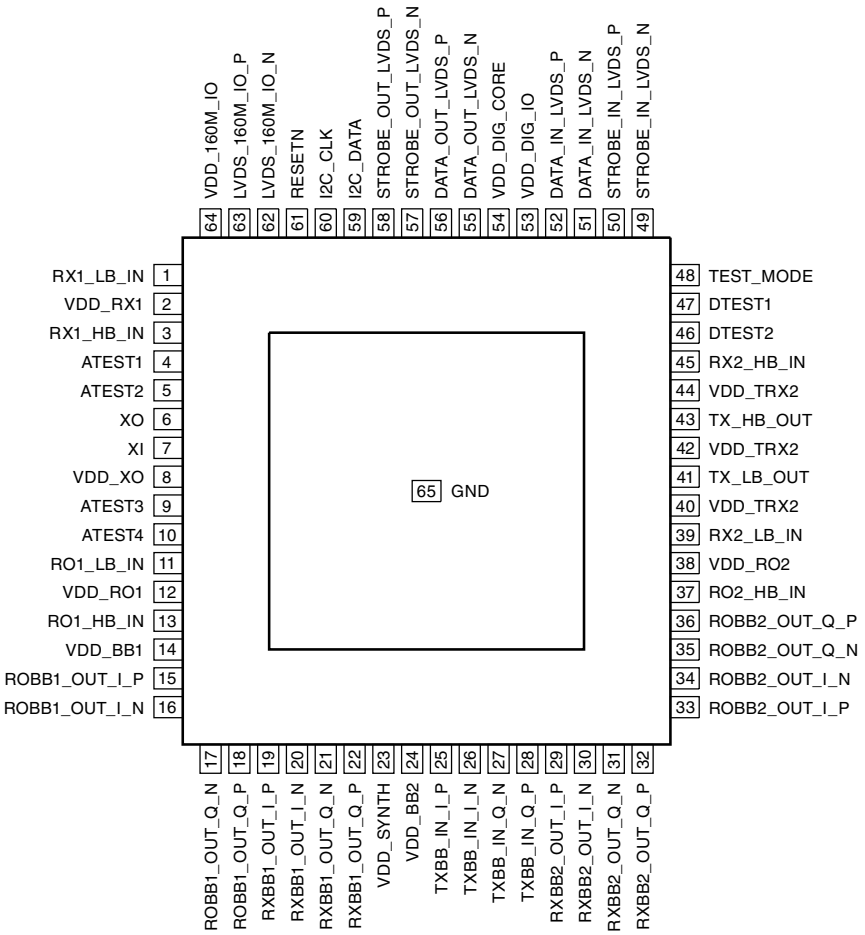


Figure 4. RF112 Transceiver QFN layout

2.2 Pinout list

This table provides the pinout listing for the RF112 Transceiver by bus.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
Digital core LVDS					
DATA_IN_LVDS_N	Data in negative	51	I	V_{DD}_DIG_IO	1
DATA_IN_LVDS_P	Data in positive	52	I	V_{DD}_DIG_IO	1
STROBE_IN_LVDS_N	Data in strobe negative	49	I	V_{DD}_DIG_IO	1
STROBE_IN_LVDS_P	Data in strobe positive	50	I	V_{DD}_DIG_IO	1
DATA_OUT_LVDS_N	Data out negative	55	O	V_{DD}_DIG_IO	
DATA_OUT_LVDS_P	Data out positive	56	O	V_{DD}_DIG_IO	
STROBE_OUT_LVDS_N	Data out strobe negative	57	O	V_{DD}_DIG_IO	
STROBE_OUT_LVDS_P	Data out strobe positive	58	O	V_{DD}_DIG_IO	
RESETN	Reset enable	61	I	V_{DD}_DIG_IO	
TEST_MODE	Test mode	48	I	V_{DD}_DIG_IO	2
Clocking					
XO	Crystal output	6	I	V_{DD}_XO	
XI	Crystal input	7	O	V_{DD}_XO	
LVDS_160M_IO_N	160 MHz clock IO negative	62	IO	V_{DD}_160M_IO	
LVDS_160M_IO_P	160 MHz clock IO positive	63	IO	V_{DD}_160M_IO	
I2C					
I2C_CLK	Serial clock	60	I	V_{DD}_DIG_IO	
I2C_DATA	Serial data	59	IO	V_{DD}_DIG_IO	
Analog test					
ATEST1	Analog test 1	4	IO	V_{DD}_XO	
ATEST2	Analog test 2	5	IO	V_{DD}_XO	
ATEST3	Analog test 3	9	IO	V_{DD}_XO	3
ATEST4	Analog test 4	10	IO	V_{DD}_XO	
Digital test					
DTEST1	Digital test 1	47	I	V_{DD}_DIG_IO	4
DTEST2	Digital test 2	46	I	V_{DD}_DIG_IO	4
Receiver Channel 1					
RX1_LB_IN	Low band input Receiver Channel 1 received signal	1	I	V_{DD}_RX1	
RX1_HB_IN	High band input Receiver Channel 1 received signal	3	I	V_{DD}_RX1	
RXBB1_OUT_I_N	Base band I output negative differential signal of received channel 1	20	O	V_{DD}_BB1	

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
RXBB1_OUT_I_P	Base band I output positive differential signal of received channel 1	19	O	V_{DD}_BB1	
RXBB1_OUT_Q_N	Base band Q output negative differential signal of received channel 1	21	O	V_{DD}_BB1	
RXBB1_OUT_Q_P	Base band Q output positive differential signal of received channel 1	22	O	V_{DD}_BB1	
Receiver Channel 2					
RX2_LB_IN	Low band input Receiver Channel 2 received signal	39	I	V_{DD}_TRX2	
RX2_HB_IN	High band input Receiver Channel 2 received signal	45	I	V_{DD}_TRX2	
RXBB2_OUT_I_N	Base band I output negative differential signal of received channel 2	30	O	V_{DD}_BB2	
RXBB2_OUT_I_P	Base band I output positive differential signalof received channel 2	29	O	V_{DD}_BB2	
RXBB2_OUT_Q_N	Base band Q output negative differential signal of received channel 2	31	O	V_{DD}_BB2	
RXBB2_OUT_Q_P	Base band Q output positive differential signal of received channel 2	32	O	V_{DD}_BB2	
Observation Channel 1					
RO1_LB_IN	Low band input Observation Channel 1 received signal	11	I	V_{DD}_RO1	
RO1_HB_IN	High band input Observation Channel 1 received signal	13	I	V_{DD}_RO1	
ROBB1_OUT_I_N	Base band I output negative differential signal of received Observation Channel 1	16	O	V_{DD}_BB1	
ROBB1_OUT_I_P	Base band I output positive differential signal of received Observation Channel 1	15	O	V_{DD}_BB1	
ROBB1_OUT_Q_N	Base band Q output negative differential signal of received Observation Channel 1	17	O	V_{DD}_BB1	
ROBB1_OUT_Q_P	Base band Q output positive differential signal of received Observation Channel 1	18	O	V_{DD}_BB1	
Observation Channel 2					
RO2_HB_IN	High band input Observation Channel 2 received signal	37	I	V_{DD}_RO2	

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
ROBB2_OUT_I_N	Base band I output negative differential signal of received Observation Channel 2	34	O	V_{DD}_BB2	
ROBB2_OUT_I_P	Base band I output positive differential signal of received Observation Channel 2	33	O	V_{DD}_BB2	
ROBB2_OUT_Q_N	Base band Q output negative differential signal of received Observation Channel 2	35	O	V_{DD}_BB2	
ROBB2_OUT_Q_P	Base band Q output positive differential signal of received Observation Channel 2	36	O	V_{DD}_BB2	
Transmit Channel					
TX_LB_OUT	Transmit low band output	41	O	V_{DD}_TRX2	
TX_HB_OUT	Transmit high band output	43	O	V_{DD}_TRX2	
TXBB_IN_Q_P	Base band Q input positive differential transmit signal	28	I	V_{DD}_BB2	
TXBB_IN_I_P	Base band I input positive differential transmit signal	25	I	V_{DD}_BB2	
TXBB_IN_I_N	Base band I input negative differential transmit signal	26	I	V_{DD}_BB2	
TXBB_IN_Q_N	Base band Q input negative differential transmit signal	27	I	V_{DD}_BB2	
Power					
VDD_RX1	Channel 1 receiver supply	2	-	-	
VDD_XO	Oscillator supply	8	-	-	
VDD_RO1	Observer 1 input supply	12	-	-	
VDD_BB1	Base band channel 1 and observer 1 supply	14	-	-	
VDD_SYNTH	Synthesizer supply	23	-	-	
VDD_BB2	Base band channel 2 and observer 2 supply	24	-	-	
VDD_RO2	Observer 2 input supply	38	-	-	
VDD1_TRX2	Channel 2 receiver and transmitter supply	40	-	-	
VDD2_TRX2	Channel 2 receiver and transmitter supply	42	-	-	
VDD3_TRX2	Channel 2 receiver and transmitter supply	44	-	-	
VDD_DIG_IO	Digital IO supply	53	-	-	
VDD_DIG_CORE	Digital Core supply	54	-	-	
VDD_160M_IO	Clocking IO supply	64	-	-	
Ground					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	65	-	-	5

1. A 100 Ohms resistor should be placed between this pad and the other polarity pad.
2. In normal mode should be pulled to ground.
3. Application requires pull-down 10 +/-1% KOhm resistor.
4. This pin can be left unconnected since they are configured as inputs with internal pull-down at reset.
5. The 65th pin serves as a ground and thermal pad.

3 Electrical characteristics

This section describes the DC and AC electrical specifications for the chip. This section describes the DC and AC electrical specifications of the interfaces and signals for the chip.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings[1,2]

Characteristic	Symbol	Min	Max	Unit	Notes
Analog supply voltages	VDD_RX1	-0.50	2.00	V	
	VDD_XO	-0.50	2.00	V	
	VDD_RO1	-0.50	2.00	V	
	VDD_BB1	-0.50	2.00	V	
	VDD_SYNTH	-0.50	2.00	V	
	VDD_BB2	-0.50	2.00	V	
	VDD_RO2	-0.50	2.00	V	
	VDD_TRX2	-0.50	2.00	V	
	VDD_160M_IO	-0.5	2.00	V	
Digital core supply voltage	VDD_DIG_CORE	-0.50	1.00	V	
Digital I/O supply voltage	VDD_DIG_IO	-0.50	2.00	V	

Table continues on the next page...

Table 2. Absolute maximum ratings[1,2] (continued)

Characteristic	Symbol	Min	Max	Unit	Notes
Maximum voltage on non-supply pins	Digital pins, incl. GPIO:s	-0.50	2.00	V	
	Analo pins	-0.50	1.1	V	
Latch-up	Pass				JESD78
Maximum RF input			+5	dBm	Peak power, all frequenc y bands
Max ESD voltage, HBM	RF pins and BB pins	1000		V	ANSI-ESDA-JEDEC JS-011-2 011
	Other pins	2000		V	
Max ESD voltage, CDM	RF pins and BB pins	250		V	ANSI-ESDA-JEDEC JS-011-2 011
	Other pins	500		V	
Storage temperature	T_{STG}	-55	150	° C	

Notes:

1. Functional operating conditions are given in this table are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. Exposing device to Absolute Maximum Ratings conditions for long periods of time may affect reliability or cause permanent damage.

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Analog supply voltage	VDD_RX1	1.62	1.67	1.72	V	
	VDD_XO	1.62	1.67	1.72	V	
	VDD_RO1	1.62	1.67	1.72	V	
	VDD_BB1	1.62	1.67	1.72	V	
	VDD_SYNTH	1.62	1.67	1.72	V	
	VDD_BB2	1.62	1.67	1.72	V	

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
	VDD_RO2	1.62	1.67	1.72	V	
	VDD_TRX2	1.62	1.67	1.72	V	
	VDD_160M_IO	1.62	1.67	1.72	V	
Digital supply voltage	VDD_DIG_CORE	0.87	0.90	0.97	V	
	VDD_DIG_IO	1.71	1.80	1.89	V	
Low frequency Analog supply ripple	1 kHz ≤ fRipple ≤ 50 MHz					
	Single tone			10	mVp	
	Total ripple			14	mVrms	
High frequency Analog supply ripple	4.9 GHz ≤ fRipple ≤ 6.2 GHz					
	Single tone			2.5	mVpp	
Analog supply noise	1 kHz ≤ fNoise ≤ 30 kHz		1000	2000	nV/ √ Hz	
	fNoise = 100 kHz		200	400	nV/ √ Hz	
	fNoise = 1.0 MHz		20	40	nV/ √ Hz	
	fNoise = 10 MHz			4	nV/ √ Hz	
	fNoise > 50 MHz			1	nV/ √ Hz	
	4.9 GHz ≤ fNoise ≤ 6.2 GHz			1	nV/ √ Hz	
Operating temperature range	TA, ambient temperature	0			° C	
	TJ, junction temperature			105	° C	
Extended Operating temperature range	TA, ambient temperature	-40			° C	
	TJ, junction temperature			105	° C	
Reference clock frequency	Crystal or external clock source	40	MHz			
Crystal load capacitance	Effective differential load capacitance	5	10	12	pF	Implemented on-chip as single-ended capacitors on XI and XO
External Clock Source Input Level	XO CMOS input	0.80		0.99	Vpp	
External Clock Source Duty Cycle	XO CMOS input	45	50	55	%	
External Clock Source Phase Noise	TCXO CMOS input at 40MHz frequency					
	Offset = 10 kHz			-143	dBc/Hz	
	Offset = 100 kHz			-155		
	Offset = 1 MHz and above			-160		

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input external clock differential input voltage level	LVDS_160M_IO_P/N Input	200	400		mVpp	1
Input external clock input common mode voltage level	LVDS_160M_IO_P/N Input	0.2		1.2	V	1
Input external clock duty cycle	LVDS_160M_IO_P/N Input	45	50	55	%	1
Output reference clock output load	LVDS_160M_IO_P/N output		100		Ω	1
Rx BB external output load (kick -back filter)	R1		50		Ω	3
	C1		10		pF	3
TX BB input common mode				0.5	V	
TX BB input signal level	Full scale from DAC			0.35	Vp	
Frequency Range	HB Lowest			4900	MHz	
	HB Highest	6000			MHz	
	LB Lowest			2400	MHz	
	LB Highest	2500			MHz	

3.1.3 Power Sequencing

Power rails can ramp simultaneously for all voltages, Core power suppliesVDD_DIG_CORE (0.9V) should not begin to ramp before other supplies, and should reach 90% of nominal voltage no more than 5ms after I/O rails ramp as shown in the figure below. Analog 1.67 V supply and I/O 1.8 V supply are expected to begin ramp simultaneously.

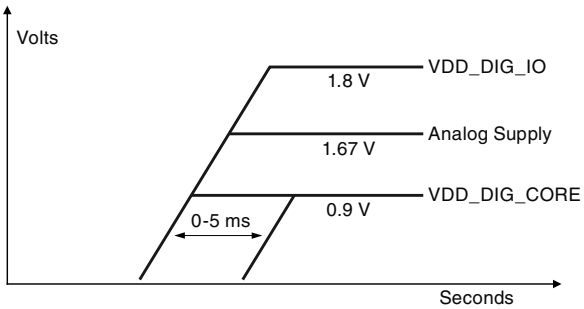


Figure 5. RF112 Transceiver power sequencing

3.2 General specification

3.3 Receiver specification

Each TRX receiver consist of two identical dual band chains with shared baseband filters, as shown in the figure below. The main building blocks consist of the LNA, the mixer and the active leapfrog lowpass filter. The double-sided bandwidth of the analog filter supports a large range of fixed settings ranging from 20 to 80 MHz.The filter bandwidth needs to be calibrated by the baseband chip. The analog receiver gain can be controlled at RF and in the active analog filter. The peak envelop signal can be measured at RF before baseband filtering.

The figure below shows the detailed block diagram of one receive chain. The second receive chain and the observation chains are identical, except for the RO2 chain which has no LB input.

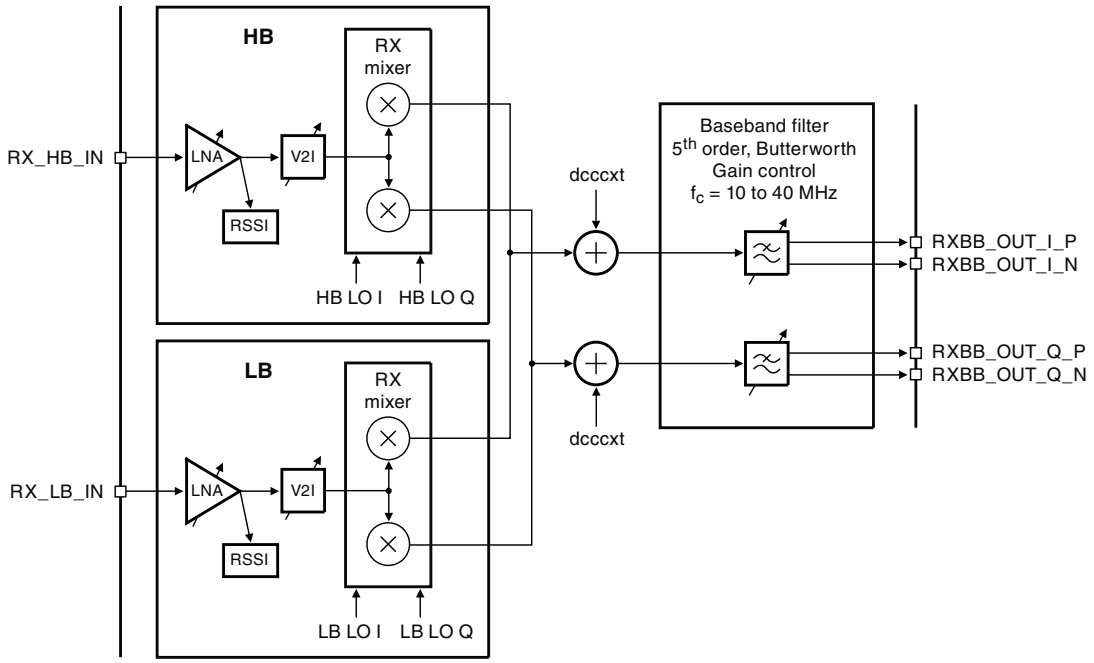


Figure 6. Block diagram of one receive chain.

The receive data path is DC coupled to avoid settling issues. To mitigate offset errors it is recommended to perform offset compensation at the input of the active analog filter. The DC offset compensation algorithm has to be run in the baseband.

The observation receivers are identical to the TRX receivers, except for that the second observation receiver has no LB chain.

3.3.1 RxRF RSSI

The RxRF RSSI have three detection levels, that needs to be sampled at a nominal rate of 20 MSps using sample clocks derived from the 160 MHz synthesizer, synchronized for all four receiver branches.

The decay rate of the peak detectors can be configurable to allow for a setting with nonsignificant decay during a 50 ns sampling interval, but not so slow decay that it becomes unable to track a change in signal level due to a radar pulse falling edge, that is caused by out-of-band RADAR pulses which change the energy level for short durations of 500-1000 ns in a periodic pattern.

The sampling in the analog detector is done using the 160 MHz clock from the synthesizer, down-sampling and filtering is performed in the digital core.

3.3.2 Rx BB interface

The Rx BB output shall be connected to the ADC input in the baseband chip as shown in below:

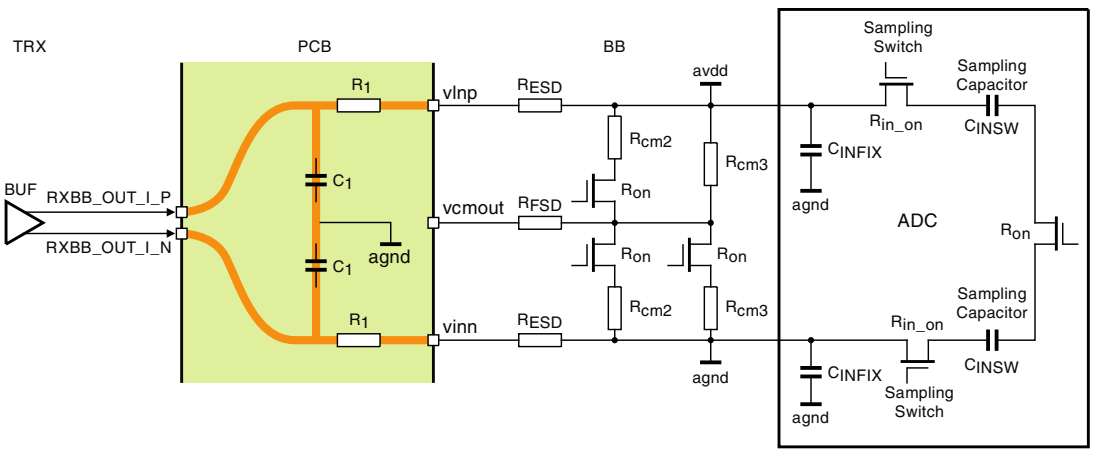


Figure 7. Connection of Rx BB output of transceiver chip (TRX) to ADC input of baseband chip (BB). Note that Rcm2 and Rcm3 shall be disconnected, input common mode voltage of the ADC is set by the Rx BB output buffer.

This table shows receiver specification. All RF signal levels are referred to the input of an ideal matching network with no losses.

Table 4. Receiver specification

Parameter	Conditions	Min	Typ	Max	Unit
RX input impedance	HB and LB, differential, including matching		50		Ω
RX input return loss, |S11|	HB and LB, all gain settings, including matching	6	>10		dB
Noise figure	Maximum gain setting All channel bandwidths RMS value over all subcarrier freq				
	4900 MHz		4.5		dB
	5300 MHz		4.9		dB
	6000 MHz		5.4		dB
	2400-2500 MHz		4.4		dB
Max input signal level	Minimum gain RMS power of OFDM burst where EVM ≤ -32 dB	-20	-10		dBm
RX1, RX2, RO1, and RO2 EVM	RMS value over all subcarriers. All values are applicable at both -40 dBm and -23 dBm. Ideal IQ correction and demodulation (data-aided equalization enabled).				
	Over process, voltage and temp (PVT):				

Table continues on the next page...

Table 4. Receiver specification (continued)

Parameter	Conditions	Min	Typ	Max	Unit
	4900 MHz, ChBW: 20/40 MHz, PVT		-40	-36	dB
	4900 MHz, ChBW: 80 MHz, PVT		-39	-36	dB
	5300 MHz, ChBW: 20/40 MHz, PVT		-39	-36	dB
	5300 MHz, ChBW: 80 MHz, PVT		-38	-36	dB
	6000 MHz, ChBW: 20/40 MHz, PVT		-38	-36	dB
	6000 MHz, ChBW: 80 MHz, PVT		-37	-36	dB
	2400-2500 MHz, ChBW: 20/40 MHz, PVT		-39	-36	dB
	Room temperature (RT), TJ ≈ 50 ° C				
	4900 MHz, ChBW: 20/40 MHz, PV			-38	dB
	4900 MHz, ChBW: 80 MHz, PV			-37	dB
	5300 MHz, ChBW: 20/40 MHz, PV			-38	dB
	5300 MHz, ChBW: 80 MHz, PV			-37	dB
	6000 MHz, ChBW: 20/40 MHz, PV			-38	dB
	6000 MHz, ChBW: 80 MHz, PV			-36	dB
Gain specification					
RX total gain	Gain into 100 Ω load.				
	Minimum, HB			5.5	dB
	Maximum, HB	61.5			dB
	Minimum, LB			2	dB
	Maximum, LB	65			dB
RX gain variation	Over temperature. For all gain settings				
	HB	-4		+4	dB
	LB	-4		+4	dB
RX RF gain control range	HB		38		dB
	LB		41		dB
RX RF gain flatness	Max-Min; over frequency.				
	HB			2.5	dB
	LB			1	dB
RX BB gain control range			30		dB

Table continues on the next page...

Table 4. Receiver specification (continued)

Parameter	Conditions	Min	Typ	Max	Unit
RX gain step	RF HB		5.5		dB
	RF LB		6		dB
	Analog baseband		3		dB
RX gain settling time	Gain settled to ± 1 dB of steady state after gain update command (20MHz channel BW) Excluding LLCP transfer time.			200	ns
Analog filter					
Analog RX filter cutoff frequency (signal bandwidth is twice the cutoff)	5th order Butterworth, 3 dB point				
	Ch BW 20 MHz		12.5		MHz
	Ch BW 40 MHz		25.0		MHz
	Ch BW 80 MHz		50.0		MHz
Accuracy of analog RX filter cutoff frequency after calibration		-7		+7	%
Analog RX filter suppression	At center of adjacent channel		18		dB
	At center of alternate channel		48		dB
Analog RX filter group delay variation	Deviation of group delay from the group delay at DC, normalized to half the channel bandwidth, i.e. the given values are the products of Δ gd and the nominal channel BW, fchBW . fchBW = {20, 40, 80} MHz				
	Range: 0 to 30% of fchBW	-0.35		+0.35	
	Range: 30% to 46% of fchBW	-0.80		+0.80	
Analog RX signal path delay	Channel bandwidth B = 20/40/80 MHz Cannot be measured		1/B		s
Analog RX baseband output voltage	Into 100 Ω load.				
	Common mode voltage	0.45		0.55	V
	Peak differential voltage	-0.9		+0.9	V
	Target operating peak differential voltage amplitude for best performance		0.6		V
IQ error and offset					

Table continues on the next page...

Table 4. Receiver specification (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Resolution of RX DC offset comp. at output	Maximum baseband gain		± 5		mV
DC offset at output after calibration	Maximum gain Measurement bandwidth ≤ 10 kHz	-50		50	mV
Rx image rejection ratio	Uncalibrated	25			dB
RSSI					
RSSI thresholds	referred to the 1dB compression point (CP1dB)				
	High threshold		-6		dBc
	Middle threshold		-15		dBc
	Low threshold		-24		dBc
RSSI accuracy			+/-3.2		dB
RSSI sample rate	Configurable	10/20			MSps
General					
EVM degradation due to Rx spurious signal	Degradation compared to neighboring channel. RF level chosen to give -30dB EVM with maximum gain for neighboring channel. 40 MHz channel bandwidth.			3	dB
Rx RF pin isolation	See Table 6				

3.4 Transmitter specification

The transmitter consists of a high band and a low band RF chain with shared baseband reconstruction filter, see figure below.

A fifth order Butterworth reconstruction filter suppresses the DAC alias signals, the filter bandwidth needs to be calibrated by the baseband chip. The baseband signal is then up-converted and amplified. The LO leakage depends on the DC offset and needs to be minimized by DC offset compensation of the digital signal in the baseband. The TX gain can be adjusted at several places and most of the gain control is done at RF to ensure that the LO leakage remains low for all output power levels.

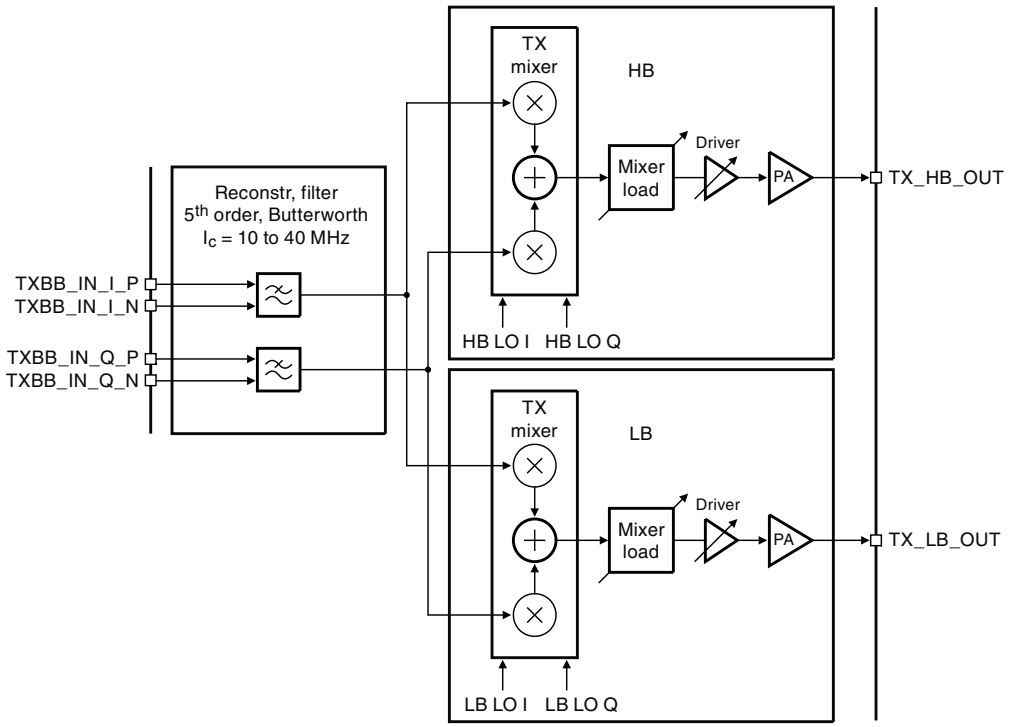


Figure 8. Detailed block diagram of the transmit chains

3.4.1 Tx BB interface

The Tx BB input shall be connected to the DAC output in the baseband chip as shown in figure below:

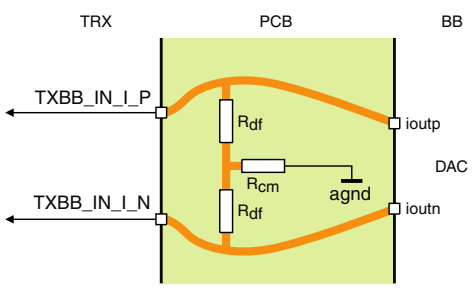


Figure 9. Tx BB interface

The DAC settings and external resistors Rdif and Rcm must be chosen to fulfill the TX BB input common mode and input signal level requirements.

This table shows the transmitter specification. Unless otherwise specified, all values assume that the receivers are disabled. All RF signal levels are referred to the output of an ideal matching network with no losses.

Table 5. Transmitter specification

Parameter	Conditions	Min	Typ	Max	Unit
RF channel bandwidth	ChBW	20/40/80			MHz
Signal modulation standards	802.11b/g/a/n/ax				
TX output return loss	50 Ω characteristics impedance, Including off-chip impedance matching -6 dBm output level	6			dB
TX EVM	RMS value over all subcarriers. All values are applicable at both -6 dBm and -26 dBm. Ideal IQ correction and demodulation (data-aided equalization enabled).				
	Over process, voltage and temp (PVT):				
	4900 MHz, ChBW: 20/40 MHz, PVT		-41	-36	dB
	4900 MHz, ChBW: 80 MHz, PVT		-39	-36	dB
	5300 MHz, ChBW: 20/40 MHz, PVT		-40	-36	dB
	5300 MHz, ChBW: 80 MHz, PVT		-38	-36	dB
	6000 MHz, ChBW: 20/40 MHz, PVT		-39	-36	dB
	6000 MHz, ChBW: 80 MHz, PVT		-37	-36	dB
	2400-2500 MHz, ChBW: 20/40 MHz, PVT		-44	-38	dB
	Room temperature (RT), TJ ≈ 50 ° C				
	4900 MHz, ChBW: 20/40 MHz, PV			-38	dB
	4900 MHz, ChBW: 80 MHz, PV			-38	dB
	5300 MHz, ChBW: 20/40 MHz, PV			-38	dB
	5300 MHz, ChBW: 80 MHz, PV			-38	dB
	6000 MHz, ChBW: 20/40 MHz, PV			-38	dB
	6000 MHz, ChBW: 80 MHz, PV			-37	dB

Table continues on the next page...

Table 5. Transmitter specification (continued)

Parameter	Conditions	Min	Typ	Max	Unit
TX spectrum mask	HE PPDU, 3dB better than standard, except when limited by TX noise floor, in the figure examples from Figure 11 to Figure 15, also see spectrum maskFigure 10.				
	ChBW 20MHz: [A = 9.75MHz, B = 10.25MHz, C = 20MHz, D = 30MHz]				
	level B			-23	dBr
	level C			-31	dBr
	level D, HB			-43	dBr
	level D, LB			-48	dBr
	ChBW 40MHz: [A = 19.5MHz, B = 20.5MHz, C = 40MHz, D = 60MHz]				
	level B			-23	dBr
	level C			-31	dBr
	level D, HB			-43	dBr
	level D, LB			-48	dBr
	ChBW 80MHz (HB only):[A = 39.5MHz, B = 40.5MHz, C = 80MHz, D = 120MHz]				
	level B			-23	dBr
	level C			-31	dBr
	level D, HB			-43	dBr
	level D, LB			-48	dBr
Transmit signal level into 50 Ohms load	Maximum with full performance	-6			dBm
	Minimum with full performance			-26	dBm
	Minimum with EVM<-36dB (Return loss, gain step etc. may be out of spec, also note spectrum mask degradation)		-40	-38	dBm
Power control resolution			2		dB
TX gain settling time	Gain settled to within ± 1 dB of steady state after gain update command			400	ns
Analog filter					
Reconstr. filter cutoff frequency	5th order Butterworth, 3 dB point				
	Ch BW 20 MHz		12.5		MHz
	Ch BW 40 MHz		25.0		MHz
	Ch BW 80 MHz		50.0		MHz
Accuracy of reconstr filter cutoff frequency after calibration		-5		+5	%

Table continues on the next page...

Table 5. Transmitter specification (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Reconstr. filter suppression	At center of adjacent channel		20		dB
	At center of alternate channel		50		dB
Reconstr. filter group delay variation	Deviation of group delay from the group delay at DC, normalized to half the channel bandwidth, i.e. the given values are the products of Δ gd and the nominal channel BW, fchBW . fchBW = {20, 40, 80} MHz				
	Range: 0 to 30% of fchBW	-0.35		+0.35	-
	Range: 30% to 46% of fchBW	-0.80		+0.80	-
Analog TX signal path delay	Channel bandwidth B = 20/40/80 MHz Cannot be measured.		1/B		s
General					
Unwanted emissions below 1 GHz	30 MHz ≤ f < 1.0 GHz RBW = 100 kHz OFDM signal, $P_{RMS\_TX\_burst}$ = -6 dBm 40 MHz channel BW			-70	dBm
Unwanted emissions above 1 GHz	RBW = 1 MHz OFDM signal, $P_{RMS\_TX\_burst}$ = -6 dBm 40 MHz channel BW Harmonics excluded Reference spurs excluded Valid for frequencies at least 100 MHz from the LO or outside the adjacent channel, whichever is largest.				
	1.000 GHz ≤ f < 3.000 GHz			-70	dBm
	3.000 GHz ≤ f < 4.200 GHz			-80	dBm
	4.200 GHz ≤ f < 4.500 GHz			-80	dBm
	4.500 GHz ≤ f ≤ 5.150 GHz			-80	dBm
	5.150 GHz < f < 6.500 GHz			-80	dBm
	6.500 GHz ≤ f < 7.500 GHz			-80	dBm

Table continues on the next page...

Table 5. Transmitter specification (continued)

Parameter	Conditions	Min	Typ	Max	Unit
	7.500 GHz ≤ f < 12.75 GHz			-80	dBm
TX noise floor	Spurs excluded. Valid for frequencies at least 100 MHz from the LO or outside the adjacent channel, whichever is largest. P_{OUT} ≤ -6 dBm, over PVT		<-146	-144	dBm/Hz
Tx image rejection ratio	Uncalibrated	25			dB
Tx RF pin isolation	see Table 6				

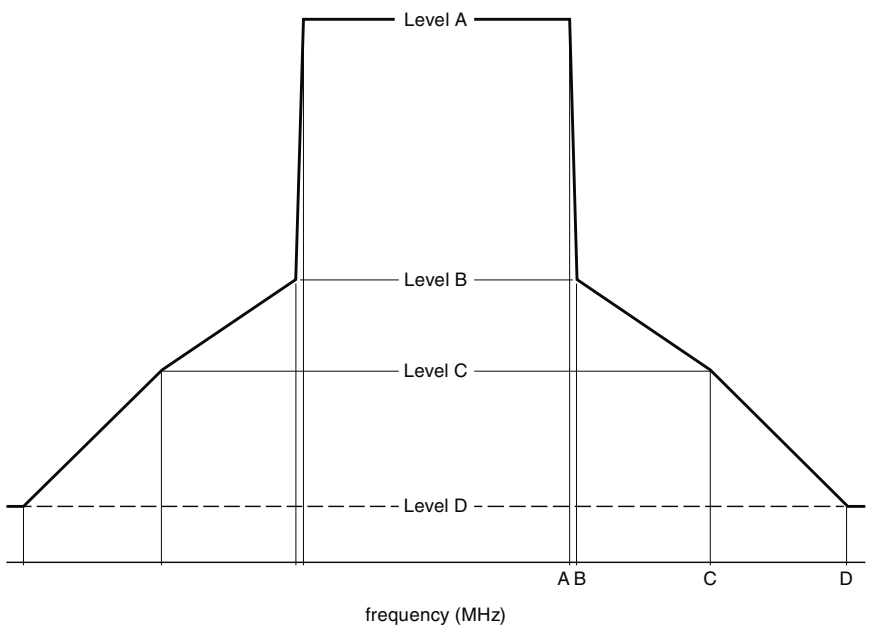


Figure 10. Spectrum Mask

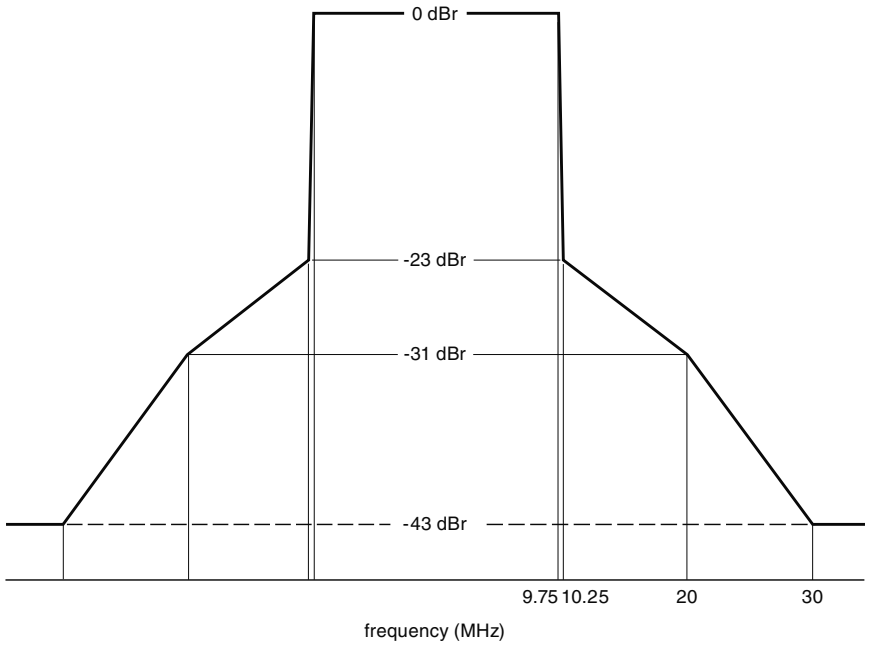


Figure 11. Transmit spectrum mask, high band, 20MHz band width

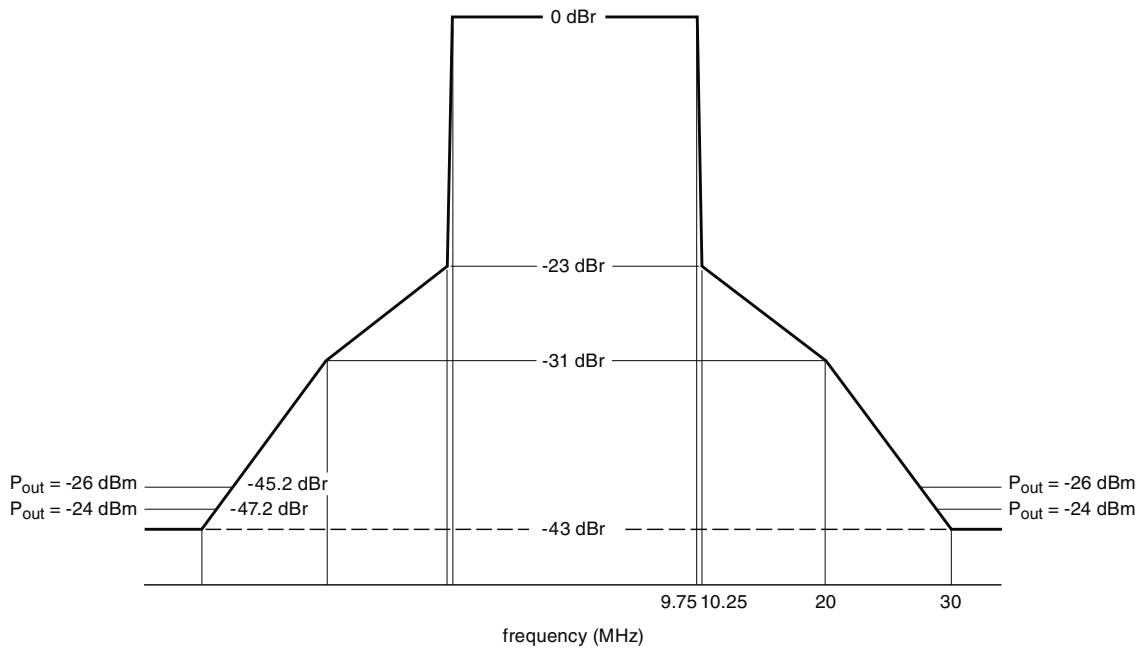


Figure 12. Transmit spectrum mask, low band, 20 MHz band width – at low output power limited by TX noise floor see examples in dashed ----.

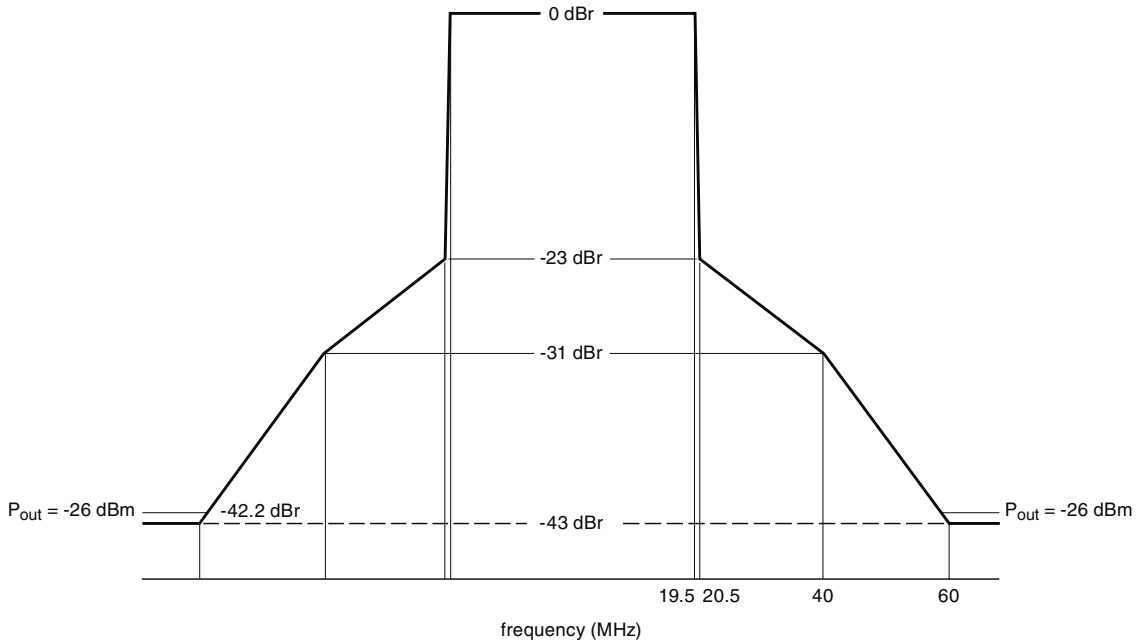


Figure 13. Transmit spectrum mask, high band, 40MHz band width – at low output power limited by TX noise floor see examples in dashed ----.

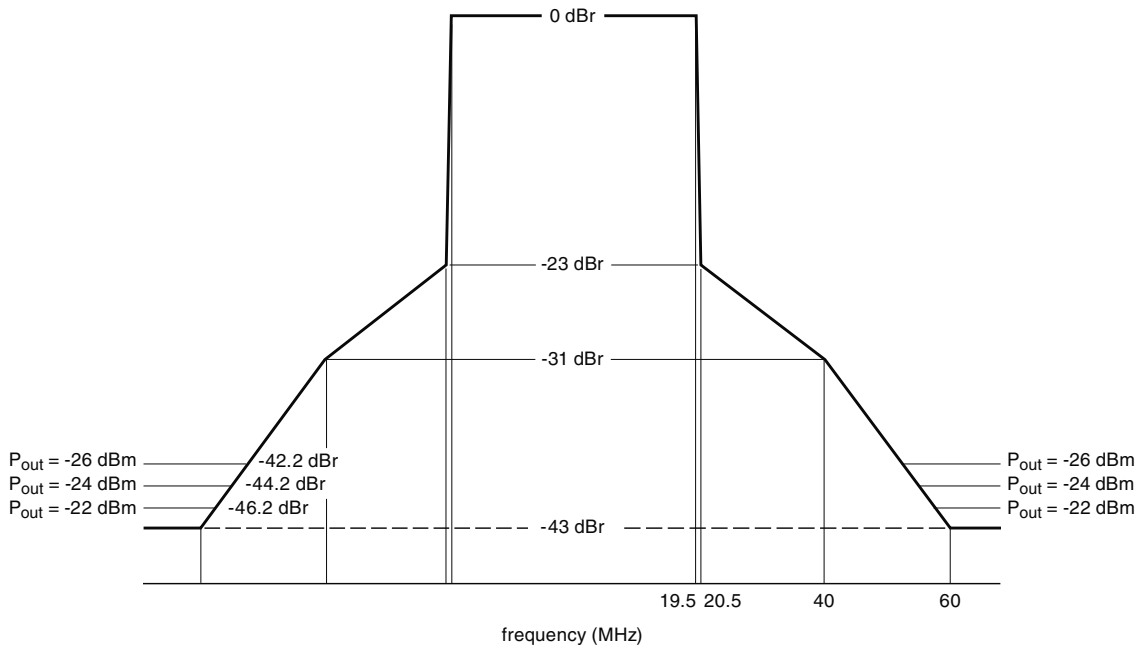


Figure 14. Transmit spectrum mask, low band, 40MHz band width – at low output power limited by TX noise floor see examples in dashed ----.

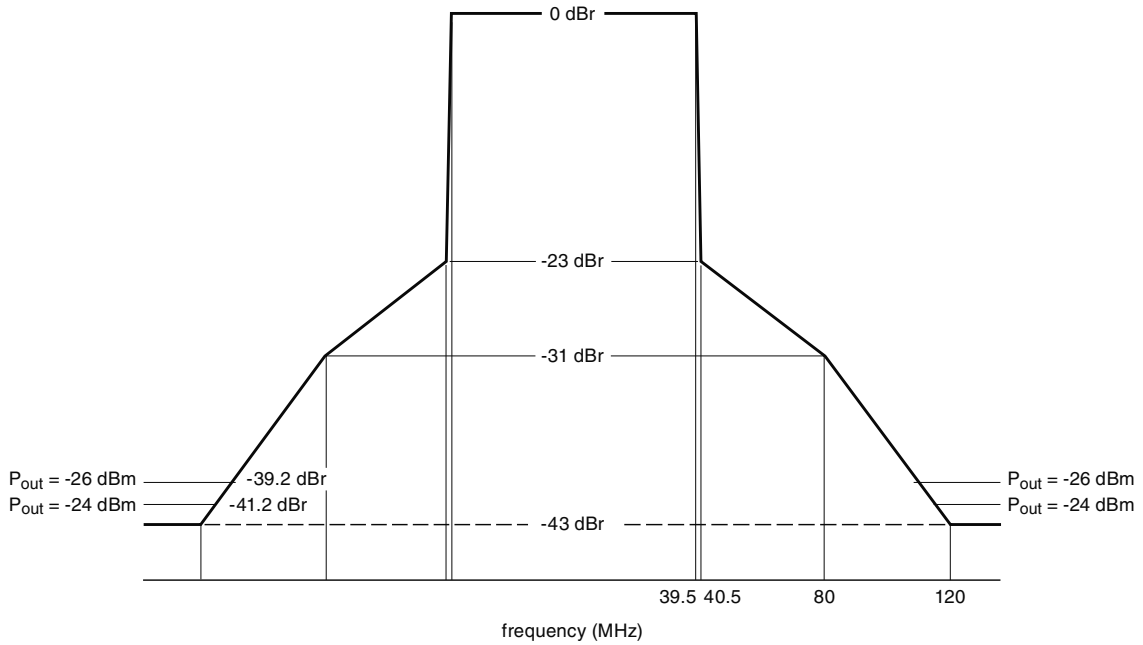


Figure 15. Transmit spectrum mask, high band, 80MHz band width – at low output power limited by TX noise floor see examples in dashed ----.

3.5 Isolation

This table shows the minimum isolation between RF pins.

Table 6. isolation between RF pins

Path	Pin	**TRX: RX1**		**TRX: RX2**		**RO1**		**RO2**	**TRX: TX**		**Unit**
		RX1_LB_IN	RX1_HB_IN	RX2_LB_IN	RX2_HB_IN	RO1_LB_IN	RO1_HB_IN	RO2_HB_IN	TX_LB_OUT	TX_HB_OUT	
TRX: RX1	RX1_LB_IN	-	-	45	25	45	25	25	-	-	dB
	RX1_HB_IN		-	25	45	25	45	45	-	-	dB
TRX: RX2	RX2_LB_IN			-	-	45	25	25	-	-	dB
	RX2_HB_IN				-	25	45	45	-	-	dB
RO 1	RO1_LB_IN					-	-	25	25	25	dB
	RO1_HB_IN						-	45	25	25	dB
RO 2	RO2_HB_IN							-	25	25	dB
TRX: TX	TX_LB_OUT								-	-	dB

Table continues on the next page...

Table 6. isolation between RF pins (continued)

	TX_HB_OUT									-	dB

3.6 Frequency generation specification

Several LO-signals and clocks have to be generated independently in RF112 Transceiver.

To retain the RF path coherence after power-up, all the synthesizers as well as all LO dividers must be running all the time after power on. The frequency dividers must be able to track the frequency while tuning, not missing any clock pulses, so that the mixer phases will be the same when returning to the same frequency after a frequency change.

The TRX and the two observation receiver chains each require its own synthesizers. The clocks used by the LVDS interfaces are generated internally in the LVDS IP and are consequently not described here. An overview of the LO and clock generation architecture is shown in the figure below.

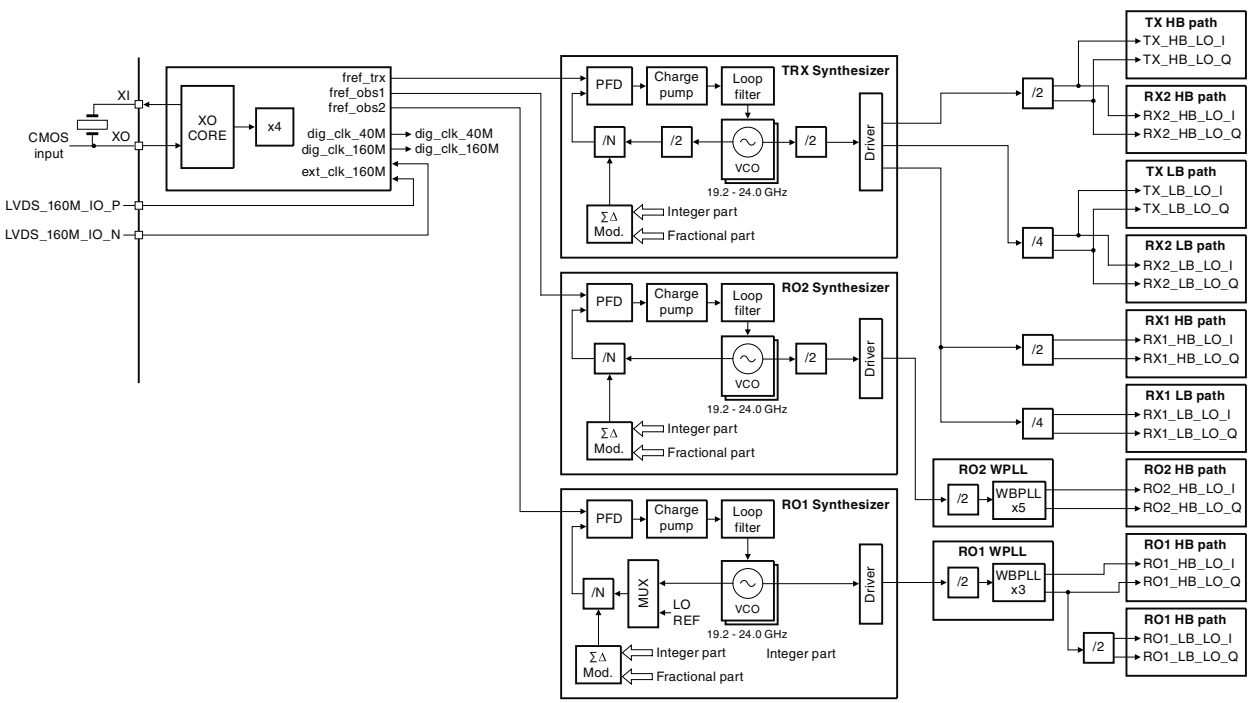


Figure 16. LO and clock generation block diagram

The transmitters require very low wideband noise. The LOs for the TRX are therefore generated from a high frequency VCO running at four or eight times the LO frequency.

The observation receiver LOs are generated from synthesizers in the 2 to 4 GHz range followed by WBPLLs. The dual observation receivers use a ratio between the synthesizer and WBPLL of 3/2 or 3/4, while the HB only observation receiver uses a ratio of 5/2 to minimize the frequency overlap of the two VCOs. There are no requirements on phase coherence for the observation receivers.

The figure below shows the Graphical illustration of the frequency planning. Y-axis has no relevance.

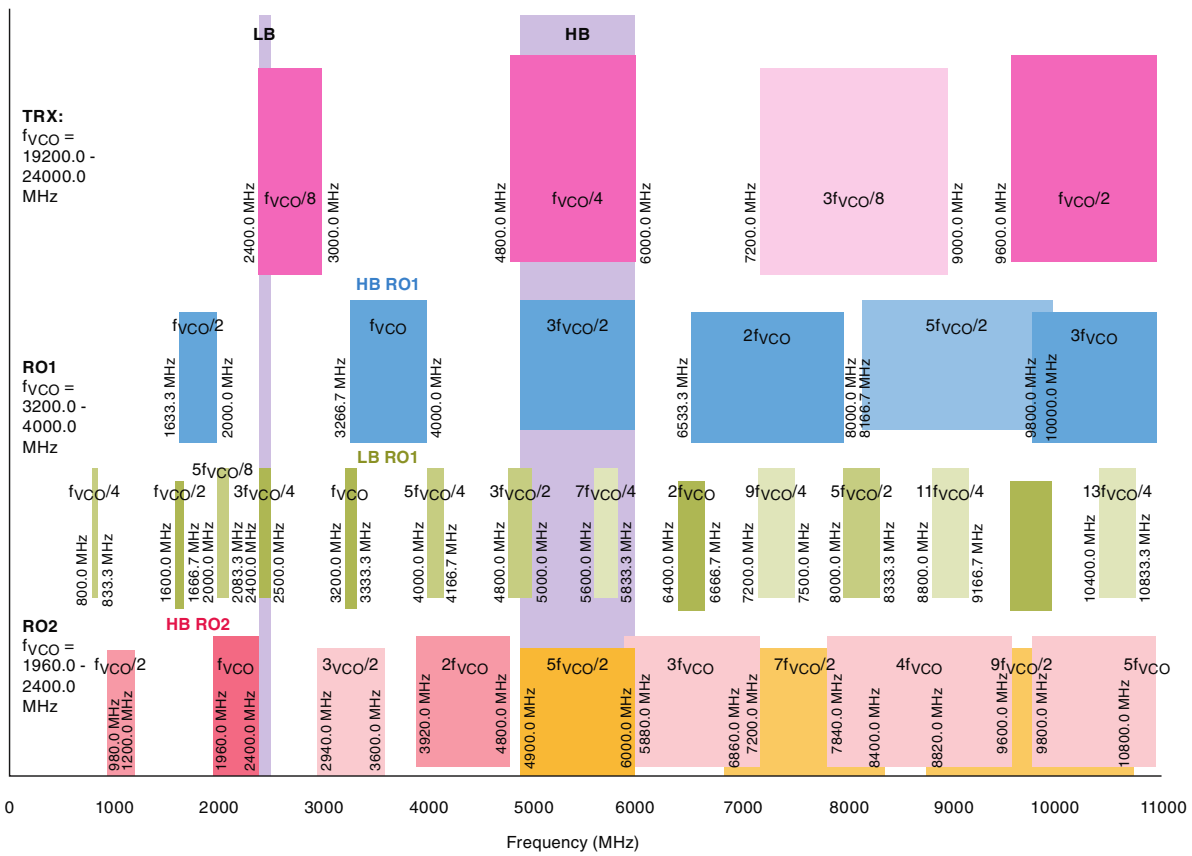


Figure 17. Graphical illustration of the frequency planning. Y-axis has no relevance.

The synthesizer reference frequency, typically 160.0 MHz, is generated by multiplying the crystal oscillator clock at 40 MHz by 4 using a DLL. The crystal oscillator can either drive its own crystal or receive an external clock input - either as a sinusoidal signal or a 0.9 V CMOS signal.

The LVDS interface can be used to output a 160 MHz reference clock, to be used by other chips, see below Figure 18 . To reset and configure the transceiver a 40 MHz clock must be input through or generated by the crystal.

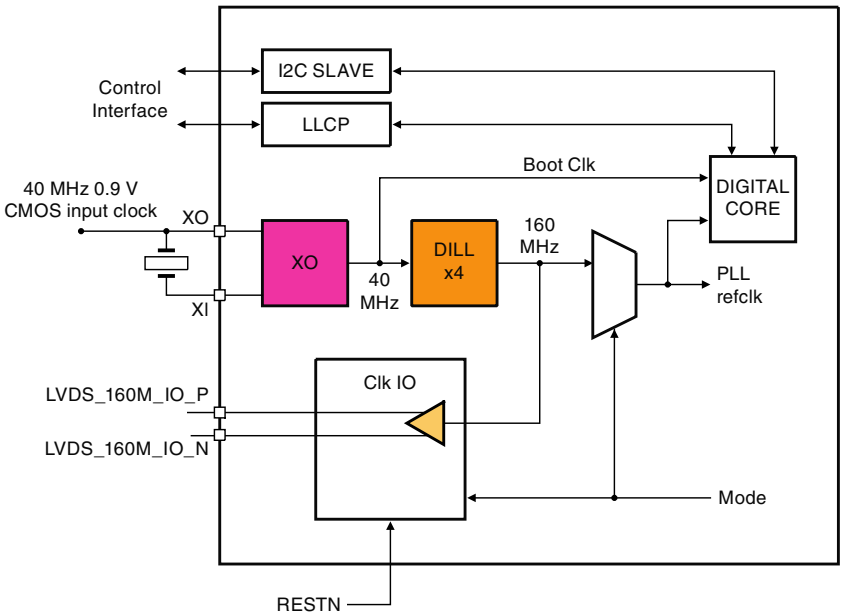


Figure 18. Generation of synthesizer references and digital clocks

This table shows the frequency generation specification.

Table 7. Frequency generation specification

Parameter	Conditions	Min	Typ	Max	Unit
VCO frequency	TRX-VCO: Lowest			19.2	GHz
	TRX-VCO: Highest	24.0			GHz
	RO2-VCO: Lowest			1960	MHz
	RO2-VCO: Highest	2400			MHz
	RO1-VCO: Lowest			3200	MHz
	RO1-VCO: Highest	4000			MHz
LO frequency	HB Lowest			4900	MHz
	HB Highest	6000			MHz
	LB Lowest			2400	MHz
	LB Highest	2500			MHz
LO frequency resolution				20	Hz
LO spurious free dynamic range	Reference spurs and integer boundary spurs excluded TRX HB/LB		-65		dBc
Integrated SSB LO phase noise	TRX HB (10 kHz to 50 MHz)		-44	-40	dBc

Table continues on the next page...

Table 7. Frequency generation specification (continued)

Parameter	Conditions	Min	Typ	Max	Unit
	TRX LB (10 kHz to 50 MHz)		-50	-43	dBc
	RO2 HB (10 kHz to 50 MHz)		-43	-39	dBc
	RO1 HB (10 kHz to 50 MHz)		-44	-39	dBc
	RO1 LB (10 kHz to 50 MHz)		-50	-43	dBc
TRX phase noise	At HB/LB LO frequency (w.c. over frequency)				
	Offset = 10 kHz		-95		dBc/Hz
	Offset = 100 kHz		-103		dBc/Hz
	Offset = 1 MHz		-106		dBc/Hz
	Offset = 10 MHz		-128		dBc/Hz
	Offset = 100 MHz (cannot be validated)		-150		dBc/Hz
RO2 RX phase noise	At HB LO frequency (w.c. over frequency)				
	Offset = 10 kHz		-95		dBc/Hz
	Offset = 100 kHz		-103		dBc/Hz
	Offset = 1 MHz		-106		dBc/Hz
	Offset = 10 MHz		-122		dBc/Hz
	Offset = 100 MHz (cannot be validated)		-136		dBc/Hz
RO1 RX phase noise	At HB/LB LO frequency (w.c. over frequency)				
	Offset = 10 kHz		-95		dBc/Hz
	Offset = 100 kHz		-103		dBc/Hz
	Offset = 1 MHz		-106		dBc/Hz
	Offset = 10 MHz		-125		dBc/Hz
	Offset = 100 MHz (cannot be validated)		-136		dBc/Hz
Synthesizer PLL Specifications					
PLL comparison frequency	4 times XO frequency		160		MHz
Reference spur level HB/LB	TRX, fLO ± N x 40 MHz		-60		dBc
	TRX, fLO ± N x 160 MHz		-60		dBc
	RO1, fLO ± N x 40 MHz		-60		dBc
	RO1, fLO ± N x 160 MHz		-60		dBc

Table continues on the next page...

Table 7. Frequency generation specification (continued)

Parameter	Conditions	Min	Typ	Max	Unit
	RO2, fLO ± N x 40 MHz		-60		dBc
	RO2, fLO ± N x 160 MHz		-60		dBc
PLL settling time	In-band frequency hop fLO within 10 kHz of final frequency		6	10	µs
Channel switching time	Any frequencies over the tuning range, inclusive of all programming, register writes and calibrations.			600	µs
Turnaround time	TX to RX: Includes time to load Rx gain state			2	µs
	RX to TX: Includes time to load Tx gain state			2	µs
XO Crystal Oscillator Specifications					
XO frequency tuning range	Typical crystal load capacitance		± 40		ppm
XO frequency resolution	T ypical crystal and typical load capacitance Static setting of fine tuning cap bank		±0.1		ppm
160MHz_DIFF_IO signal characteristics as an output					
160MHz_DIFF_IO output frequency			160		MHz
160MHz_DIFF_IO output clock jitter	Integrated from 10kHz to 80MHz		1		ps
160MHz_DIFF_IO output duty cycle		40	50	60	%
160MHz_DIFF_IO differential output voltage level (LVDS)			200		mV (VPP_DIFF[1,2])
160MHz_DIFF_IO output common mode voltage level (LVDS)			0.467		V[1,2]
Notes: 1- The LVDS_160MHz_IO measurment is to be taken based on 100 Ohms terminating load impedance as in the figure below					

Table 7. Frequency generation specification

Parameter	Conditions	Min	Typ	Max	Unit

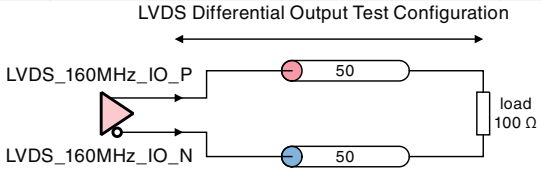


Figure 19. LVDS Load Termination

2. Please see the figure below that defines the Vcm and the VPP_SE versus VPP_DIFF

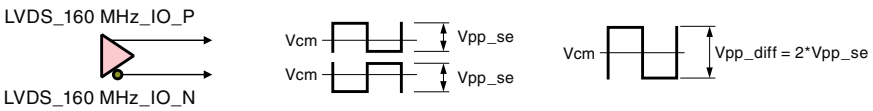


Figure 20. LVDS Signal Swing

3.7 Digital Interface

RF112 transceiver has two types of interfaces; one I2C interface for general non-time-critical control, and one Lightweight LVDS Communication Protocol (LLCP) interface.

3.7.1 LLCP Interface Characteristics

The LLCP is a Lightweight Low-voltage differential signaling (LVDS) Communication Protocol block. It provides high speed serial communication between the baseband SOC and RF112 . It makes use of two signals, the serial data (DIN/DOUT) and the strobe (SIN/SOUT). In the same fashion as the SpaceWire protocol, the clock is recovered internally by XORing the data and the strobe lines. The LLCP supports 8b10b encoding/ decoding across both data and strobe pair.

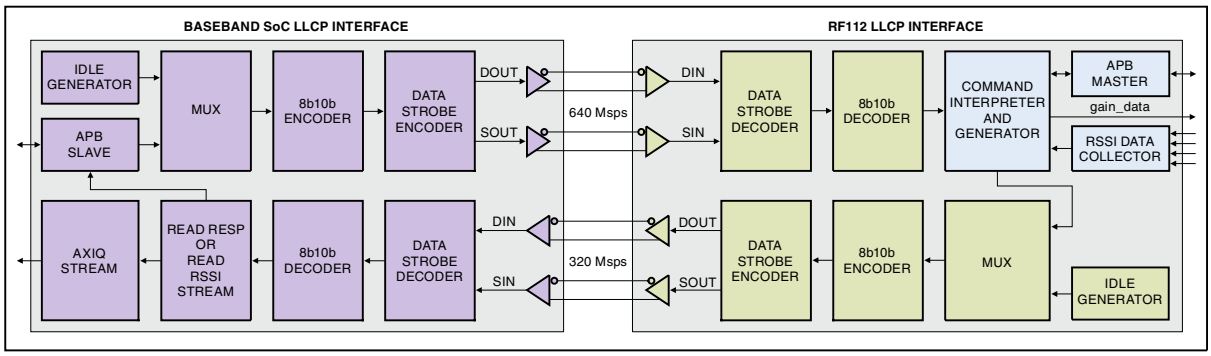


Figure 21. LLCP communication interface

This section shows the electrical LLCP characteristics

3.7.1.1 LLCP DC electrical characteristics

This table provides the DC electrical characteristics for the LLCP interface.

Table 8. LLCP DC electrical characteristics (VDD_DIG_IO = 1.8V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Differential Voltage	Vod	250.0	350.0	450.0	mV	1, 2
High-level output voltage	Voh	1.25	1.375	1.6	V	3
Low-level output voltage	Vol	0.9	1.025	1.25	V	3
Output common mode voltage	Vocm	1.125	1.2	1.375	V	2
Input Differential Voltage	Vid	100.0	-	600.0	mV	1, 5
Input common mode voltage	Vicm	0.05	-	1.57	V	5

1. |Vpadp-Vpadn|
2. Test condition: Rload=100Ohm between padp and padn.
3. Test condition: Rload=100Ohm between padp and padn
4. For recommended operating conditions, see Table 3
5. See figure "LLCP Input Waveform".

3.7.1.2 LLCP AC Timing Specifications

This table provides the LLCP AC electrical characteristics for LLCP interface.

Table 9. LLCP AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Output Transition time Low to High	Ttlh	0.12	0.58	ns	1, 2, 3
Output Transition time High to Low	Tthl	0.1	0.73	ns	1, 2, 3
Receive rate Transmit rate	-	-	640 320	Mbps	
Offset Voltage imbalance pk-pk	V_{OS}		150	mV	4

1. Test condition: Rload=100Ohm between padp and padn.
2. Measurement levels are 20-80% from output voltage.
3. See figure "LLCP LVDS Output Waveform" below.
4. See figure "Output Offset Voltage imbalance waveform" below.

NOTE

Skew between Data and Strobe:

LLCP data and strobe pairs should be routed as 100 Ohm differential pairs with matched routing length to ensure equivalent propagation time for each differential signal. Propagation time mismatch should be checked at receiver; mismatched propagation delay beyond ±80ps between data and strobe signals might exceed capabilities of on-die timing compensation circuits and prevent correct operation of interface.

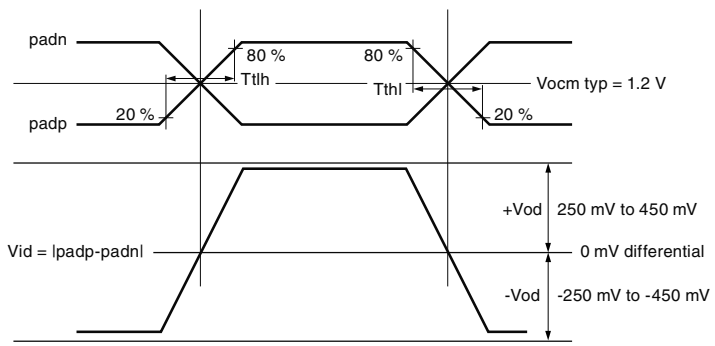


Figure 22. LLCP LVDS Output Waveform

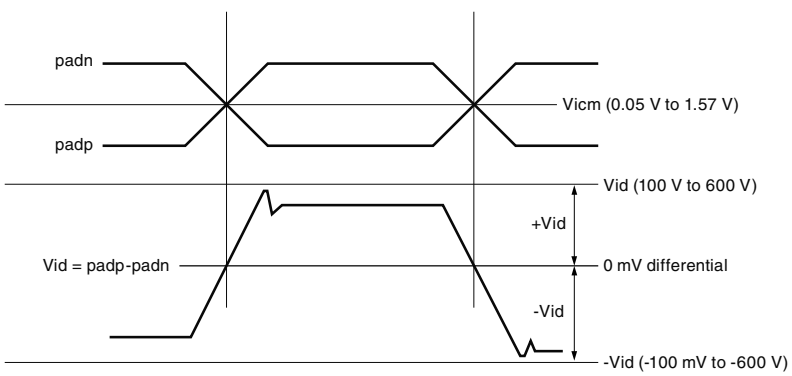


Figure 23. LLCP Input Waveform

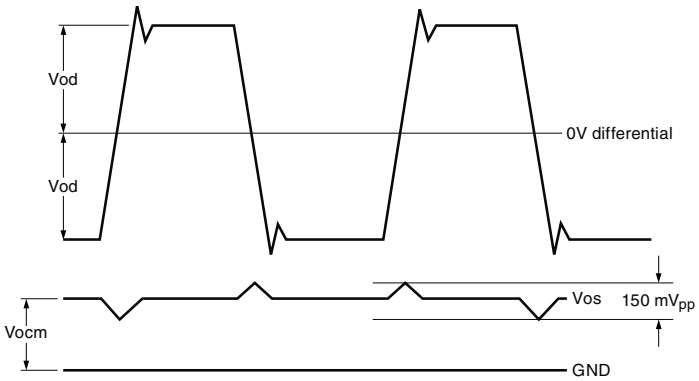


Figure 24. Output Offset Voltage Imbalance Waveform

3.8 Device start-up

The RF112 Transceiver is not equipped with any on-chip power-on-reset functionality. Instead the transceiver has a dedicated reset pin, RESETN, which has the functionality *resetn* in operational mode. The RF112 Transceiver is asynchronously reset whenever the *resetn* signal is low. To properly leave the reset mode a stable glitch free clock is required. Therefore, the reset values of the XO and the regulator powering it are such that the XO automatically starts up regardless of whether a crystal is mounted or an external clock is provided. The reset condition must not be released, that is *resetn* set high, until all supply voltages have been stable long enough to allow the XO to start up and provide a glitch free clock. If an external clock is provided to the RF112 Transceiver, then reset must not be released until the quality of that clock can be guaranteed.

Table 10. Start-up specification

Parameter	Conditions	Min	Typ	Max	Unit
Minimum reset time	Crystal oscillator			2	ms
Maximum DLL calibration time				700	µs

Upon power-up and release from reset, the chip has its 160 MHz differential clock IO buffer tri-stated. It has the internal crystal oscillator enabled to generate a 40 MHz clock, and that clock is driven to internal components to allow configuration via the I^2C and/or the LLCP interfaces.

The firmware download and further configuration are possible over either the I^2C or LLCP (running at 100 Mbps) interfaces.

After firmware download and a command to calibrate the DLL, the completion of calibration is reported in a register that can be polled over the LLCP or I^2C interfaces.

The 160 MHz differential clock IO output can be enabled with a firmware command over the LLCP or I^2C interfaces subsequent to DLL calibration.

3.9 Specification of auxiliary functions

3.9.1 Auxiliary ADC

The auxiliary ADC will be used for internal calibration and during test.

Internal signals are routed to the AUX ADC via the analog test bus.

External signals can be applied to the AUX ADC via the ATEST1 to ATEST4 pins, without using the analog testbus. The AUX ADC MUX has inputs directly connected to the ATEST pads. Both single-ended and differential external signals can be connected to the AUX ADC.

This table shows an auxiliary ADC specification.

Table 11. Auxiliary ADC specification

Parameter	Conditions	Min	Typ	Max	Unit
Conversion time per sample	11 bits, 20 MHz internal ADC clock		0.6	1.0	µs
Resolution	Number of converted bits (diff mode)		11		bits
	Effective number of bits		10		bits
External AUX ADC input range	Single-ended mode, input referred to ground (10 bits)	0		1.0	V
	Differential mode (11 bits)	-0.9		0.9	Vpp-diff
DNL				2	LSB
INL				2.5	LSB
Equivalent input noise				2	LSB
Input capacitance	Single ended mode		4.5		pF
	Differential mode		9		pF
Common mode level	Differential mode		0.45		V
Analog signal Bandwidth	External input from pins		0.7		MHz

3.9.2 Temperature sensor

Temperature information is available in the regulators as a temperature dependent voltage. Most regulators have the possibility to apply a buffered version of this voltage onto the analog testbus. The voltage can then be measured with the AUX ADC, which makes it possible to measure the temperature at different locations on the chip. Output value can be processed by calibration unit to provide values in Celsius.

This table shows the temperature sensor specification.

Table 12. Temperature sensor specification

Parameter	Conditions	Min	Typ	Max	Unit
Temperature responsivity	LSB is referred to register content which is a 14-bit averaged ADC value.				
	At 27 ° C		27		LSB / ° C
Accuracy at 100 ° C	1 sigma value		± 6		° C
Output value	LSB is referred to register content which is a 14-bit averaged ADC value.				
	100°C (658 mV)		1935		LSB
	50°C (571 mV)		606		LSB
	27°C (531 mV)		-5		LSB
	-40°C (414 mV)		-1786		LSB
Relative accuracy	Temperature change..		±2		° C

4 Package information

4.1 Mechanical dimensions

The target package is a single row 64-pin extended lead QFN with 0.5mm pitch. This table shows the package specification of the chip.

Table 13. Package specification

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Number of pins			64 + Flag as ground		
Pin pitch			0.5		mm
Thermal resistance	Junction to case.		0.9		K/W

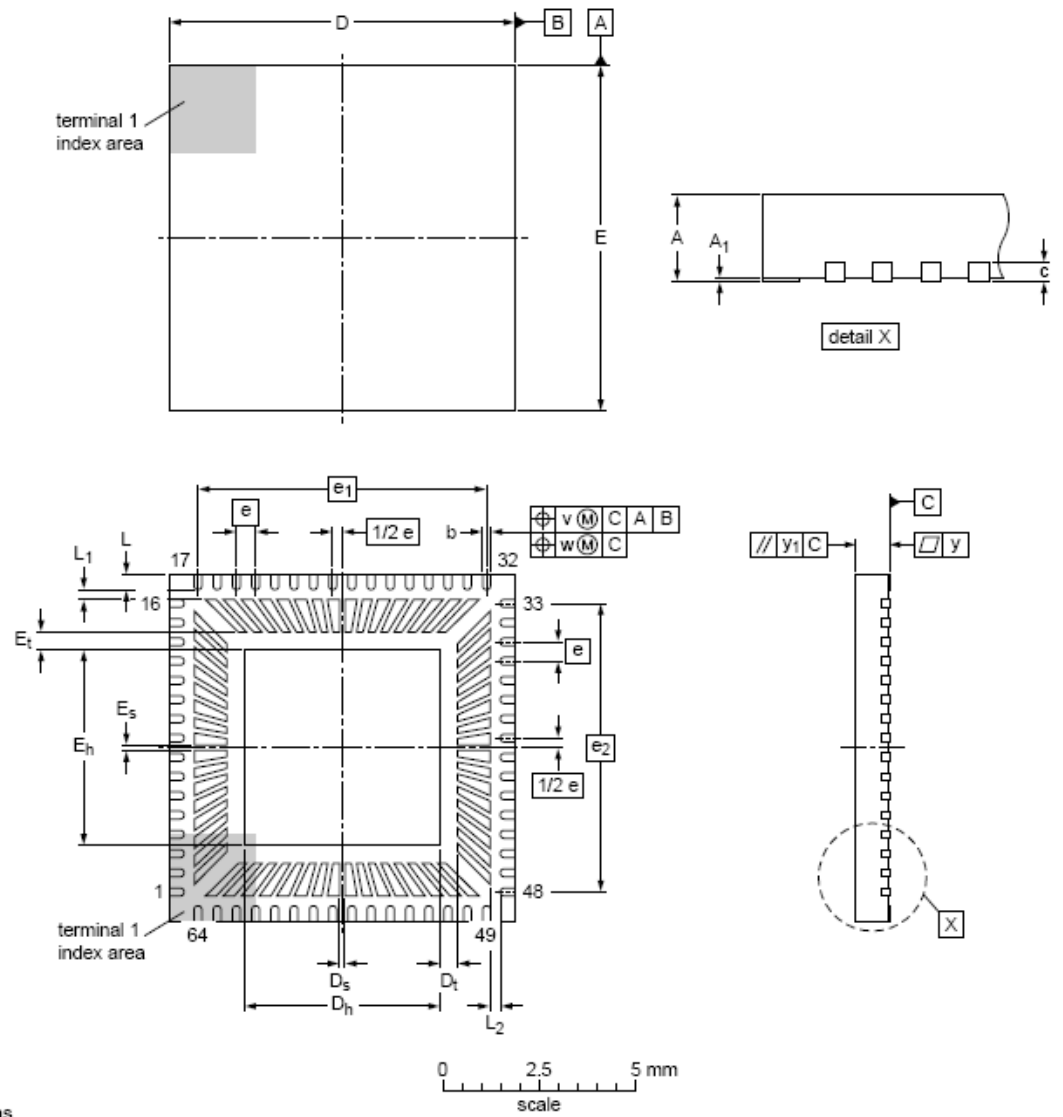
Table continues on the next page...

Table 13. Package specification (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
	Junction to ambient for a device soldered in a 4-layer 2S2P circuit board with large ground plane. No forced air flow.		25		K/W

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

HVQFN64: plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 x 9 x 0.85 mm **SOT804-4**



Dimensions

Unit		A	A_1	b	c	$D^{(1)}$	D_h	D_s	D_t	$E^{(1)}$	E_h	E_s	E_t	e	e_1	e_2	L	L_1	L_2	v	w	y	y_1
	max	1.00	0.05	0.30		9.1	5.25	0.19	0.50	9.1	5.25	0.19	0.50				0.5						
mm	nom	0.85	0.02	0.21	0.2	9.0	5.10	0.14	0.45	9.0	5.10	0.14	0.45	0.5	7.5	7.5	0.4	0.25	0.25	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		8.9	4.95	0.09	0.40	8.9	4.95	0.09	0.40				0.3						

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot804-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT804-4	---	---	---			~~10-05-26~~ 10-05-27

Package outline HVQFN64 (SOT804-4)

Figure 25. Mechanical dimensions of the RF112

5 Orderable part information

Table below shows the encoding of orderable part number

Table 14. Part encoding

Part Code	Meaning
RF112L0HS9B	Production standard temperature part operating from 0℃ to 105℃
RF112L0HX9B	Production extended temperature part operating from -40℃ to 105℃

6 Application

A typical application includes a number of external components and a specified PCB design for some specific pins.

6.1 External components

6.1.1 Crystal

To generate the reference clock an external crystal is required. For the requirements on the crystal, see the section Recommended operating conditions.

6.1.2 De-coupling

All supplies must be de-coupled using external de-coupling capacitors to fulfill the supply ripple and noise reuirements. Two capacitors are recommended per supply, one of these must be placed close to the pin.Recommended values are one 0.1µF and one 10µ F capacitor.

6.2 PCB design

To achieve the required performance the PCB design must fulfill the requirements listed in below table.

Table 15. PCB trace requirements

Pin name	PCB trace requirement
TX_HB_OUT	50 Ω transmission line
TX_LB_OUT	50 Ω transmission line
VDD_TRX2	Maximum trace length until all three traces are joined < 1mm. All three traces must be matched Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
RX1_HB_IN	50 Ω transmission line
RX1_LB_IN	50 Ω transmission line
RX2_HB_IN	50 Ω transmission line
RX2_LB_IN	50 Ω transmission line
RO1_HB_IN	50 Ω transmission line
RO1_LB_IN	50 Ω transmission line
RO2_HB_IN	50 Ω transmission line
VDD_RX1	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
VDD_RO1	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
VDD_RO2	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
VDD_BB1	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
VDD_BB2	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
XO	Place crystal close to XI and XO ports.
XI	
VDD_XO	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
VDD_SYNTH	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
VDD_160M_IO	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
VDD_DIG_CORE	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.
VDD_DIG_IO	Maximum trace/via distance to decoupling capacitor < 1mm for the small decoupling capacitor, <5mm for the large decoupling capacitor.

7 Revision history

This table summarizes revisions to this document.

Table 16. Revision history

Revision	Date	Description
1	June 2024	Initial release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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