MFS8620BMDA8ES – NXP Standard

Configuration report for ASIL-D OTP program ID: A8 rev E

Rev. 1.0 - 06/11/2023

Report

1 General description

The FS8620 is an automotive grade multi-output power supply integrated circuit, targeting various application such as radar, vision, ADAS domain controller, radio and infotainment, etc. It includes multiple switch mode and linear voltage regulators as well as external frequency synchronization interface for optimized system EMC performance.

The FS8620 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering ASIL D safety integrity level. It is developed in compliance with ISO 26262-2018 standard and it is qualified in compliance with AEC-Q100 rev H(Grade1, MSL3).

Note: Electrical characteristics for the FS8620 are maintained in the FS86 datasheet.

2 Features and benefits

- One configurable synchronous high voltage buck controller with external FETs
- One configurable boost converter with integrated low-side switch.
- One Low voltage single phase synchronous BUCK converter
- Two configurable LDO with up to 400 mA current capability.
- Up to 400 mA Load switch operation supported on LDO1
- Two input pins for wake-up detection and battery voltage sensing
- Analog Multiplexer with full System Voltages monitoring
- Enhanced leader/follower power up sequencing management
- I2C interface support (Fast-mode Plus (FM+), up to 1 Mbit/s)
- Fully independent safety state machine with monitoring mechanism targeting ASIL-D applications
- Up to 10 voltage monitoring input for FS86 and external PMIC voltage rails
- Dedicated interface for MCU monitoring with simple or challenger watchdog monitoring
- External IC failure monitoring
- Logical and Analog Built-in Self-Test

3 Applications

- Radar (Corner radar, Imaging radar, ...)
- Vision (Mono camera, Stereo camera, night vision, ...)
- ADAS domain controller
- Infotainment
- V2x



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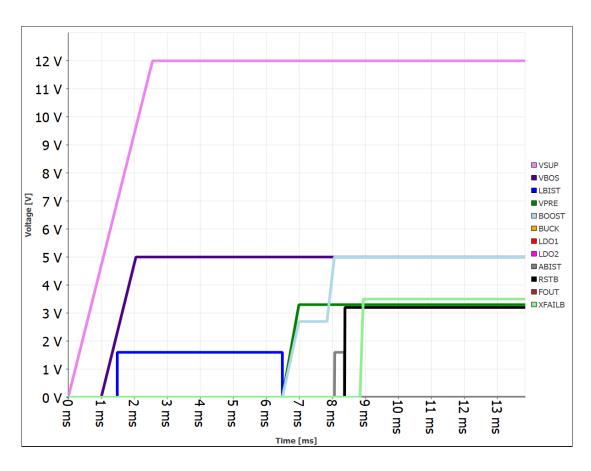
4 Ordering information

Table 1. Ordering information

Type number ^{[1][2]}	Package	age		
Type manner	Name	Description	Version	
MFS8620BMDA8ES	QFN48eP	HPQFN48, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks	SOT619-26(D)	

^[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power-up sequence summary

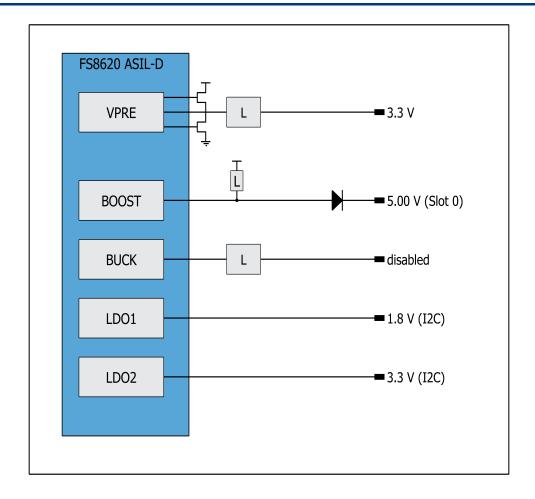


The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

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^[2] For production part number use prefix S instead of P

6 Hardware configuration diagram



7 OTP configuration

See FS86 datasheet for parametric details. The OTP configuration summary for A8 sequence ID is provided in Tables below.

Table 2. Main Configuration

Functional block	Feature	OTP selection
	Main Device I2C Address	0x20
	FailSafe Device I2C Address	0x21
	Battery Short Function Enable	Disabled
	Battery Short Timer Slection	1 ms
	MCU Application	Application with MCU
System configuration	VSUP Threshold Lockout	Power-up when VSUP > 4.7 V
	Transition To DFS	Transition to DFS without power down sequence
	Autoretry Enable Configuration	Enabled
	Autoretry Number Configuration	15 times
	Device ID	0x01
	CLK1 Divider Settings	2.22 MHz
	CLK2 Divider Settings	455 KHz
	Enable Clock Modulation	Enable clock modulation
	Clock Modulation Configuration	Triangular modulation
Clock and Synchronisation	Enable PLL	Disabled
	FOUT Slot Assignment Enable	FOUT slot assignment disabled
	FOUT Power Down Slot	Do not drive FOUT high
	XFAILB Configuration	Wait for XFAILB release in a slot
	XFAILB Release Slot	Released in Slot 2

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XFAILB Assertion Impact	Power down

Table 3. Power-up sequence

Functional block	Feature	OTP selection
Power-up sequence	Power-up/down Slot Timing	0.5 ms
	BOOST Power-up Slot	Slot 0
	BUCK Power-up Slot	Slot 0
	LDO1 Power-up Slot	Enabled by I2C
	LDO2 Power-up Slot	Enabled by I2C
	Power-up Last Slot	Power up end in Slot 3
	Power Down First Slot	Power down starts in Slot 5

Table 4. Switching and LDOs regulators

Functional block	Feature	OTP selection
	BOOST Enable	Enabled
	BOOST Voltage	5.00 V
	Minimum ON Time	50 ns
	BOOST Slope Compensation	125 mV/us
	Comp Resistor	750 KOhm
BOOST configuration	Comp Capacitance	125 pF
	BOOST Current Limitation	2 A
	BOOST Low Side Slew Rate Control	500 V/us
	BOOST Clock Selection	CLK1
	BOOST Clock Phase Delay	Delayed by 1 Clock Cycle
	BOOST Behaviour In Case Of TSD	Shutdown + DFS

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VPRE Minimum ON Time	60 ns
VPRE Output Voltage	3.3 V
Soft-Start Ramp	0.5 ms
Slope Compensation Ramp	83 mV/us
VPRE Current Limitation	150 mV
VPRE Minimum OFF Time	80 ns
VPRE Low Side Slew Rate Control	PU/PD/900 mA
VPRE High Side Slew Rate Control	PU/PD/520 mA
VPRE Clock Selection	CLK2
VPRE Clock Phase Delay	Not delayed
VPRE Switch Off Delay	OFF dly 250 us
BUCK Enable	Disabled
Buck Inductor Selection	1 uH
BUCK Output Voltage	1.1 V
BUCK Clock Selection	CLK1
BUCK Clock Phase Delay	Not delayed
BUCK Compensation Resistor	65 KOhm
BUCK Transconductance	48 us
BUCK Current Limitation	4.5 A
BUCK Soft Start Ramp	10.41 mV/us
BUCK Behaviour In Case Of TSD	Shutdown
LDO1 Output Voltage	1.8 V
Enable LDO1 Load Switch Mode	Disabled
LDO1 Behaviour In Case Of TSD	Shutdown
	Soft-Start Ramp Slope Compensation Ramp VPRE Current Limitation VPRE Minimum OFF Time VPRE Low Side Slew Rate Control VPRE High Side Slew Rate Control VPRE Clock Selection VPRE Clock Phase Delay VPRE Switch Off Delay BUCK Enable Buck Inductor Selection BUCK Output Voltage BUCK Clock Selection BUCK Clock Phase Delay BUCK Compensation Resistor BUCK Transconductance BUCK Current Limitation BUCK Soft Start Ramp BUCK Behaviour In Case Of TSD LDO1 Output Voltage Enable LDO1 Load Switch Mode

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	LDO2 Output Voltage	3.3 V
LDO2 configuration	LDO2 Current Limitation	400 mA
	LDO2 Behaviour In Case Of TSD	Shutdown

Table 5. System safety

Functional block	Feature	OTP selection
	Enable ERRMON Monitoring	Disabled
	Enable FCCU Monitoring	FCCU monitoring enabled
	Disable Watchdog Monitoring	Watchdog monitoring enabled
System safety configuration	Watchdog Selection	Challenger watchdog
Cystem salety comigaration	Enable Fault Recovery Strategy	Fault recovery strategy enabled
	RSTb 8s Timer Disable	Counter enabled
	Delay Before RSTb Release	No delay
	Fault Impact On RSTb And PGOOD	Fault asserting RSTb will assert PGOOD
	VMON0 Assignment To ABIST1	Assigned
	VMON1 Assignment To ABIST1	Not assigned
	VMON2 Assignment To ABIST1	Not assigned
	VMON3 Assignment To ABIST1	Not assigned
ABIST1 configuration	VMON4 Assignment To ABIST1	Not assigned
ADIOTTOOMINGUIANOT	VMON5 Assignment To ABIST1	Not assigned
	VMON6 Assignment To ABIST1	Not assigned
	VMON7 Assignment To ABIST1	Assigned
	VMON8 Assignment To ABIST1	Not assigned
	VMON9 Assignment To ABIST1	Not assigned

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Table 6. Voltage monitoring DAC

Functional block	Feature	OTP selection
	VMON1 Enable	Enabled
	Regulator Assignement To VMON1	PWRDWN_ DFS (DFS if OV)
	VMON1 Threshold Configuration	0.875 V
VMON1_DAC configuration	VMON1 Undervoltage Threshold	90.0 %
VWOITI_D/IC coningulation	VMON1 Overvoltage Threshold	110.0 %
	VMON1 Assignement To PGOOD	Not assigned
	VMON1 Undervoltage Deglitcher	100 us
	VMON1 Overvoltage Deglitcher	100 us
	VMON2 Enable	Disabled
	VMON2 Threshold Configuration	0.825 V
	VMON2 Undervoltage Threshold	96.0 %
VMON2_DAC configuration	VMON2 Overvoltage Threshold	104.0 %
	VMON2 Assignement To PGOOD	Not assigned
	VMON2 Undervoltage Deglitcher	100 us
	VMON2 Overvoltage Deglitcher	100 us
	VMON3 Enable	Disabled
	VMON3 Threshold Configuration	1.1 V
VMON3_DAC configuration	VMON3 Undervoltage Threshold	96.0 %
	VMON3 Overvoltage Threshold	104.0 %
	VMON3 Assignement To PGOOD	Not assigned
	VMON3 Undervoltage Deglitcher	100 us
	VMON3 Overvoltage Deglitcher	100 us

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Table 7. Voltage monitoring RES INT

Functional block	Feature	OTP selection
	VMON0 Enable	Enabled
	Regulator Assignement To VMON0	PWRDWN_ DFS (DFS if OV)
	VMON0 Voltage Configuration	3.3 V
VMON0_I2C configuration	VMON0 Undervoltage Threshold	96.0 %
viviono_izo configuration	VMON0 Overvoltage Threshold	104.0 %
	VMON0 Assignement To PGOOD	Not assigned
	VMON04 Undervoltage Deglitcher	100 us
	VMON04 Overvoltage Deglitcher	100 us
VMON4_RINT configuration	VMON4 Enable	Enabled
	VMON4 Voltage Configuration	1.8 V
	Regulator Assignement To VMON4	LDO1 (Shutdown if OV)
	VMON4 Undervoltage Threshold	96.0 %
	VMON4 Overvoltage Threshold	104.0 %
	VMON4 Assignement To PGOOD	Not assigned

Table 8. Voltage monitoring RES EXT

Functional block	Feature	OTP selection
VMON5_RES configuration	VMON5 Enable	Disabled
	VMON5 Undervoltage Threshold	90.0 %
	VMON5 Overvoltage Threshold	110.0 %
	VMON5 Assignement To PGOOD	Not assigned
VMON6_RES configuration	VMON6 Enable	Disabled
	VMON6 Undervoltage Threshold	95.0 %

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	VMON6 Overvoltage Threshold	104.0 %
	VMON6 Assignement To PGOOD	Not assigned
	VMON7 Enable	Enabled
VMON7_RES configuration	VMON7 Undervoltage Threshold	96.0 %
VINOIV _INES SOMINGUIDADI	VMON7 Overvoltage Threshold	104.0 %
	VMON7 Assignement To PGOOD	Not assigned
	VMON8 Enable	Disabled
VMON8_RES configuration	VMON8 Undervoltage Threshold	96.0 %
Vinorio_rezo coningulation	VMON8 Overvoltage Threshold	104.0 %
	VMON8 Assignement To PGOOD	Not assigned
	VMON9 Enable	Disabled
VMON9_RES configuration	VMON9 Undervoltage Threshold	90.0 %
VMONO_INEO OOMIIgaration	VMON9 Overvoltage Threshold	110.0 %
	VMON9 Assignement To PGOOD	Not assigned
	VMON56 Undervoltage Deglitcher	100 us
VMONRES Deglitcher Time configuration	VMON56 Overvoltage Deglitcher	100 us
	VMON789 Undervoltage Deglitcher	100 us
	VMON789 Overvoltage Deglitcher	100 us
	VMON123 SVS Clamp	No SVS

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