PF9453

Power management IC for i.MX 91

Rev. 1.0 — 14 August 2024 Objective short data sheet

1 General description

The PF9453 is a single chip Power Management IC (PMIC) specifically designed for the i.MX 91 processor. It provides power supply solutions for IoT (Internet of Things), smart appliance, and portable applications where size and efficiency are critical.

The device provides four high efficiency step-down regulators, three LDOs in QFN package or two LDOs for WLCSP package, one 400 mA load switch and a 32.768 kHz crystal oscillator driver. One buck regulator supports dynamic voltage scaling (DVS) along with programmable ramping up and down time. This device is characterized across -40 °C to 105 °C ambient temperature range for the HVQFN40 package or -40 °C to 85 °C ambient temperature range for WLCSP36 package, making it a good option for the industrial, extended industrial, and consumer markets. The four step-down regulators are designed to provide power for the i.MX 91 processor and the associated DRAM memory. One always-on LDO is for Secure Non-Volatile Storage (SNVS) core power supply, remaining LDOs are purposed to supply power to processor and peripheral devices. One 400 mA load switch supplies 3.3 V power to SD card, which has an internal discharge resistor, used to discharge the electric charge stored in the output when the equipment is turned off, for safety reasons.

The PF9453 is offered in two packages: 40-pin HVQFN package, 5 mm x 5 mm, 0.4 mm pitch, and 36-bump wafer-level CSP package, 2.48 mm x 2.48 mm, 0.4 mm pitch.

2 Features and benefits

- Four buck regulators
  - BUCK1: 0.6 V to 3.775 V, 25 mV step, 2000 mA
  - BUCK2: 0.6 V to 2.1875 V, 12.5 mV step, 2700 mA (QFN) / 2000 mA (WLCSP)
  - BUCK3: 0.6 V to 3.775 V, 25 mV step, 2000 mA
  - BUCK4: 0.6 V to 3.775 V, 25 mV step, 2500 mA
  - Dynamic Voltage Scaling on BUCK2
  - Monitor fault condition
- Linear regulators
  - LDO_SNVS, always-on, 1.2 V to 3.4 V in QFN or 0.8 V to 3.0 V in WLCSP with 25 mV step, 10 mA
  - LDO1, 0.8 V to 3.3 V with 25 mV step, 250 mA, voltage selection through SD_VSEL pin
  - LDO2 (QFN only), 0.5 V to 1.95 V with 25 mV step, 200 mA
- One 400 mA load switch with a built-in active discharge resistor and GPIO/I^2C control, multiplexed with DBUS debounce filter
- 32.768 kHz crystal oscillator driver and buffer output
- Power control IO
  - Power ON/OFF control
  - Standby/Run mode control
  - Watchdog reset input
- Flexible power ON/OFF sequence, One Time Programmable (OTP) device configuration
- Built-in active discharge resistor
- Fm+ 1 MHz I^2C Interface
- ESD protection
  - Human Body Model (HBM) : ± 2000 V
  - Charged Device Model (CDM) : ± 500 V
- Available in two packages
  - HVQFN40: 40-pins, 5 mm x 5 mm, 0.4 mm pitch
  - WLCSP36: 36 bumps in 6x6 array, 2.48 mm x 2.48 mm, 0.4 mm pitch

3 Applications

- IoT Devices
- White goods appliances
- Industrial application
- Portable devices

4 Ordering information

Table 1. Ordering information

Part number	Orderable part number	Topside marking	Ambient temperature	Package		
				Name	Description	Version
PF9453AHN	PF9453AHN		-40 °C to +105 °C	HVQFN40	40-pin QFN, 5.0 mm x 5.0 mm with exposed pad, 0.4 mm pitch	SOT2231-1
PF9453AUK	PF9453AUK		-40 °C to +85 °C	WLCSP36	Wafer Level Chip Scale Package; 36 bumps; 2.48 mm x 2.48 mm x 0.53 mm body (backside coating included), 0.4 mm pitch	SOT1780-14
PF9453BUK	PF9453BUK		-40 °C to +85 °C	WLCSP36	Wafer Level Chip Scale Package; 36 bumps; 2.48 mm x 2.48 mm x 0.53 mm body (backside coating included), 0.4 mm pitch	SOT1780-14

Details of the OTP programming for each device can be found in Table 5.

5 Block diagram

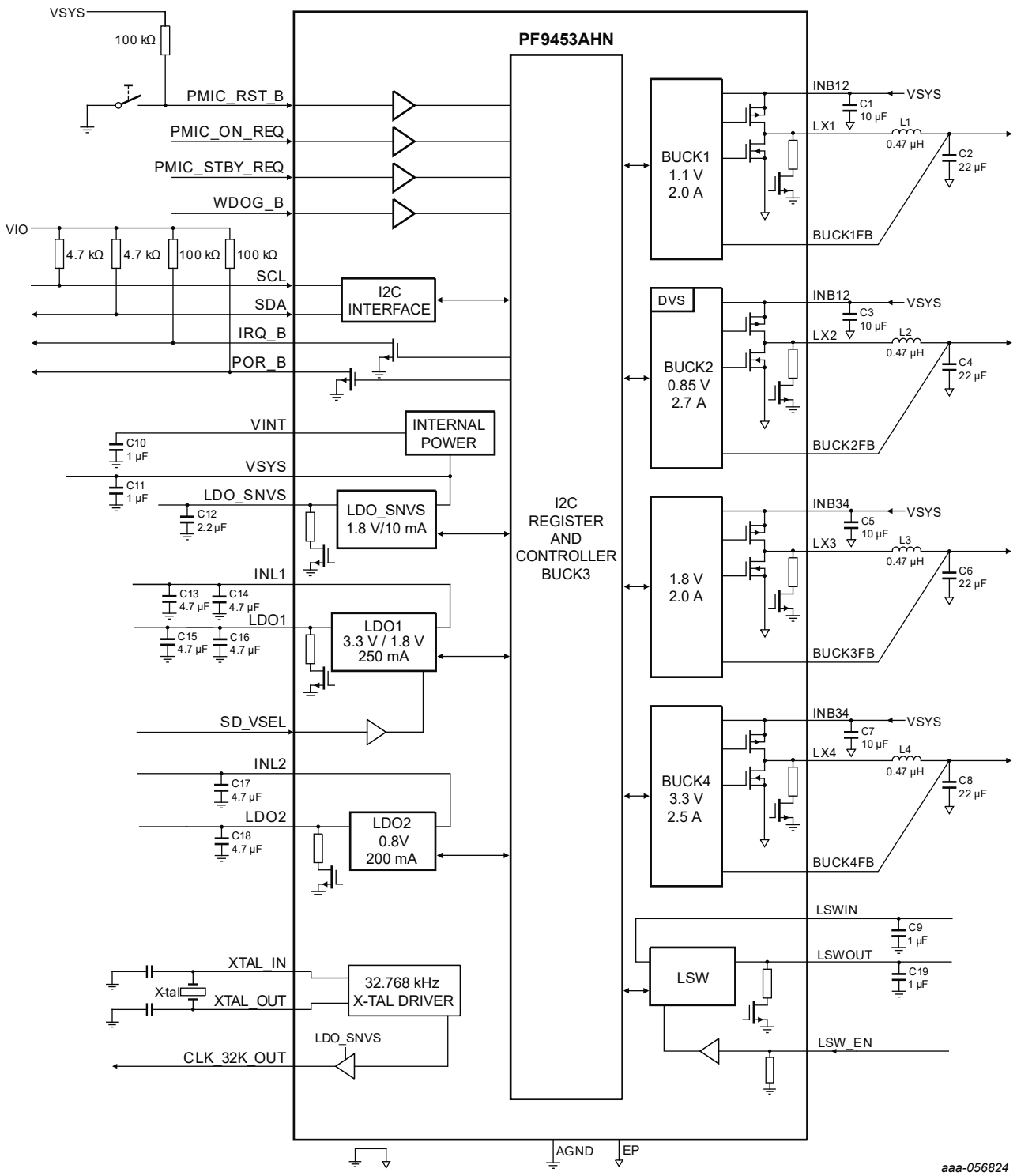


Figure 1. Block diagram - PF9453AHN (HVQFN40 package)

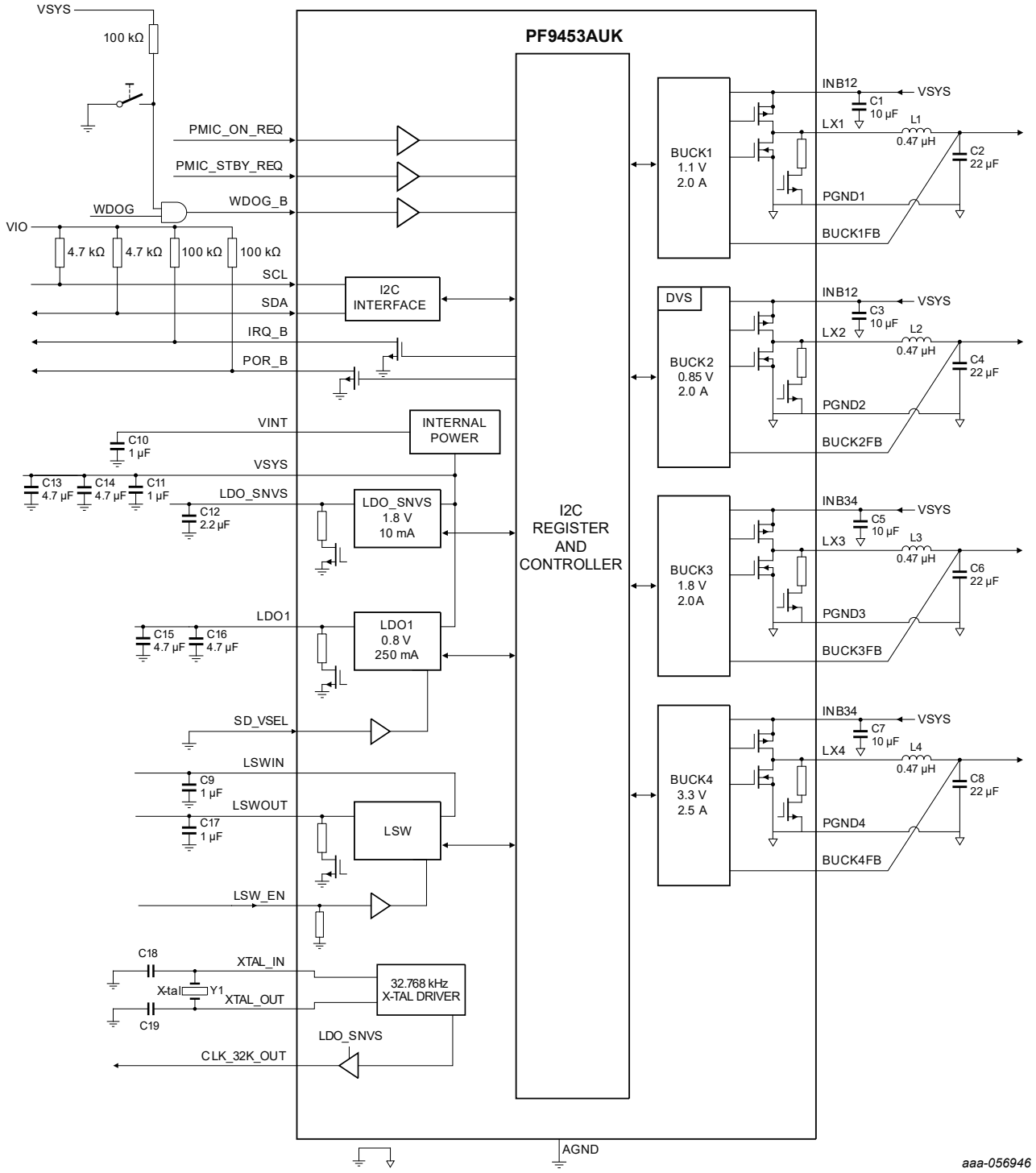


Figure 2. Block diagram - PF9453AUK (WLCSP36 package)

6 Pinning information

6.1 Pinning

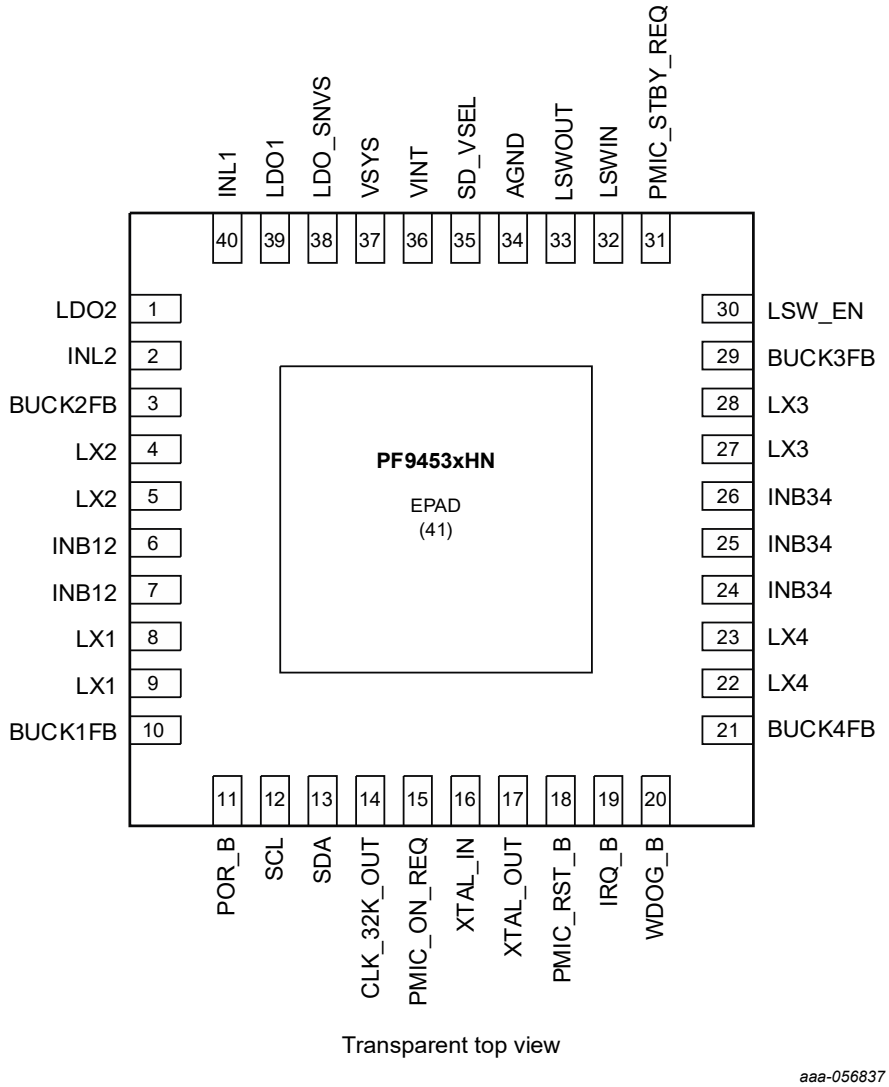


Figure 3. PF9453xHN pin map – HVQFN40 Transparent top view

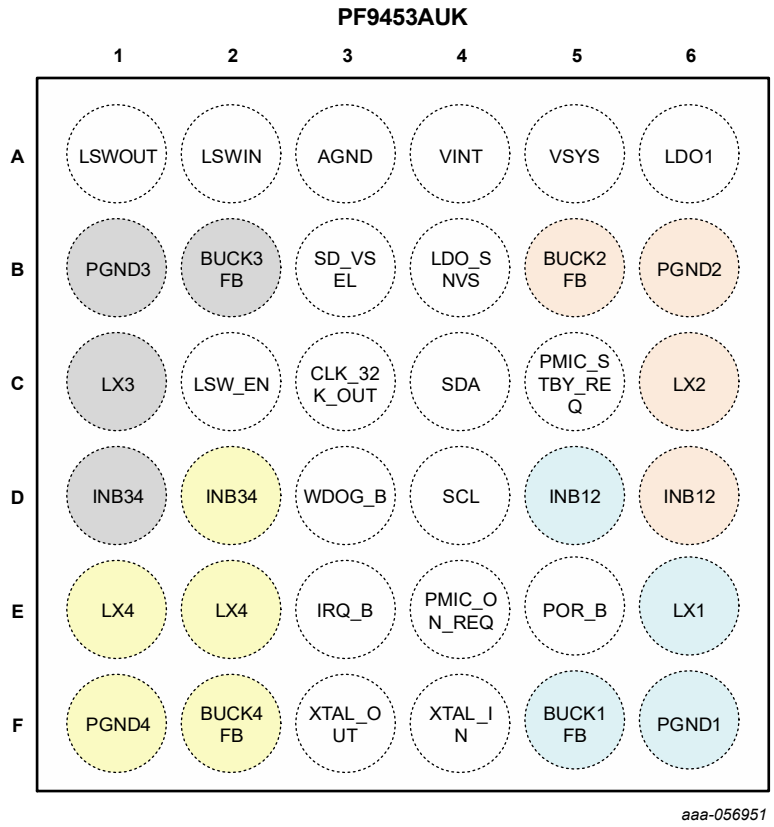


Figure 4. PF9453xHN pin map – HVQFN40 Transparent top view

6.2 Pin description

Table 2. Pin description – PF9453xHN

Symbol	Pin	Type	Description
LDO2	1	P	LDO2 output, bypass with a 4.7 µF to Ground
INL2	2	P	LDO2 input pin, bypass with a 4.7 µF to Ground
BUCK2FB	3	AI	Buck 2 feedback pin
LX2	4, 5	P	Buck 2 switching node
INB12	6, 7	P	Buck 1 and Buck 2 input pins, bypass with 2 x 10 µF
LX1	8, 9	P	Buck 1 switching node
BUCK1FB	10	AI	Buck 1 feedback pin
POR_B	11	DO	Power On reset output pin. Open drain output requiring external pull up resistor
SCL	12	DI	I^2C serial clock pin
SDA	13	DIO	I^2C serial data pin
CLK_32K_OUT	14	DO	32.768kHz clock CMOS output with LDO_SNVS power rail
PMIC_ON_REQ	15	DI	PMIC ON input from application processor. When it is asserted high, the device starts power on sequence.

Table 2. Pin description – PF9453xHN*...continued*

Symbol	Pin	Type	Description
XTAL_IN	16	AI	32.768kHz crystal oscillator input, tie to GND if XTAL is not used
XTAL_OUT	17	AO	32.768kHz crystal oscillator output, leave float if XTAL is not used
PMIC_RST_B	18	DI	PMIC reset input pin. Once it is asserted low, PMIC performs cold reset.
IRQ_B	19	DO	PMIC interrupt pin, open drain output requiring external pull up resistor
WDOG_B	20	DI	Watchdog reset input from application processor
BUCK4FB	21	AI	Buck 4 feedback pin
LX4	22, 23	P	Buck 4 switching node
INB34	24, 25, 26	P	Buck 3 and Buck 4 input pins, bypass with 2 x 10 µF
LX3	27, 28	P	Buck 3 switching node
BUCK3FB	29	AI	Buck 3 feedback pin
LSW_EN	30	DI	Load switch enable input pin. It has internal 1.5Mohm pull down resistor.
PMIC_STBY_ REQ	31	DI	Standby mode input from application processor. When it is asserted high, device enters STANDBY mode.
LSWIN	32	P	Load Switch input pin. Bypass with a 1 µF to Ground
LSWOUT	33	P	Load Switch output pin. Bypass with a 1 µF to Ground
AGND	34	P	Analog ground pin. It should be connected to ground plane through Via. Do not short to EPAD directly on top layer.
SD_VSEL	35	DI	LDO1 voltage selection input pin. LDO1 output is 3.3V when it is driven low and 1.8V when driven high.
VINT	36	P	Internal power supply output, bypass with a 1 µF to GND
VSYS	37	P	Internal power input. Bypass with a 1 µF to Ground
LDO_SNVS	38	P	LDO_SNVS output pin, bypass with a 2.2 µF to Ground
LDO1	39	P	LDO1 output. Bypass with 2 x 4.7 µF to Ground
INL1	40	P	LDO1 input pin, bypass with 2 x 4.7 µF to Ground
EPAD	41	P	Exposed pad, connect to ground.

Table 3. Pin description - PF9453AUK

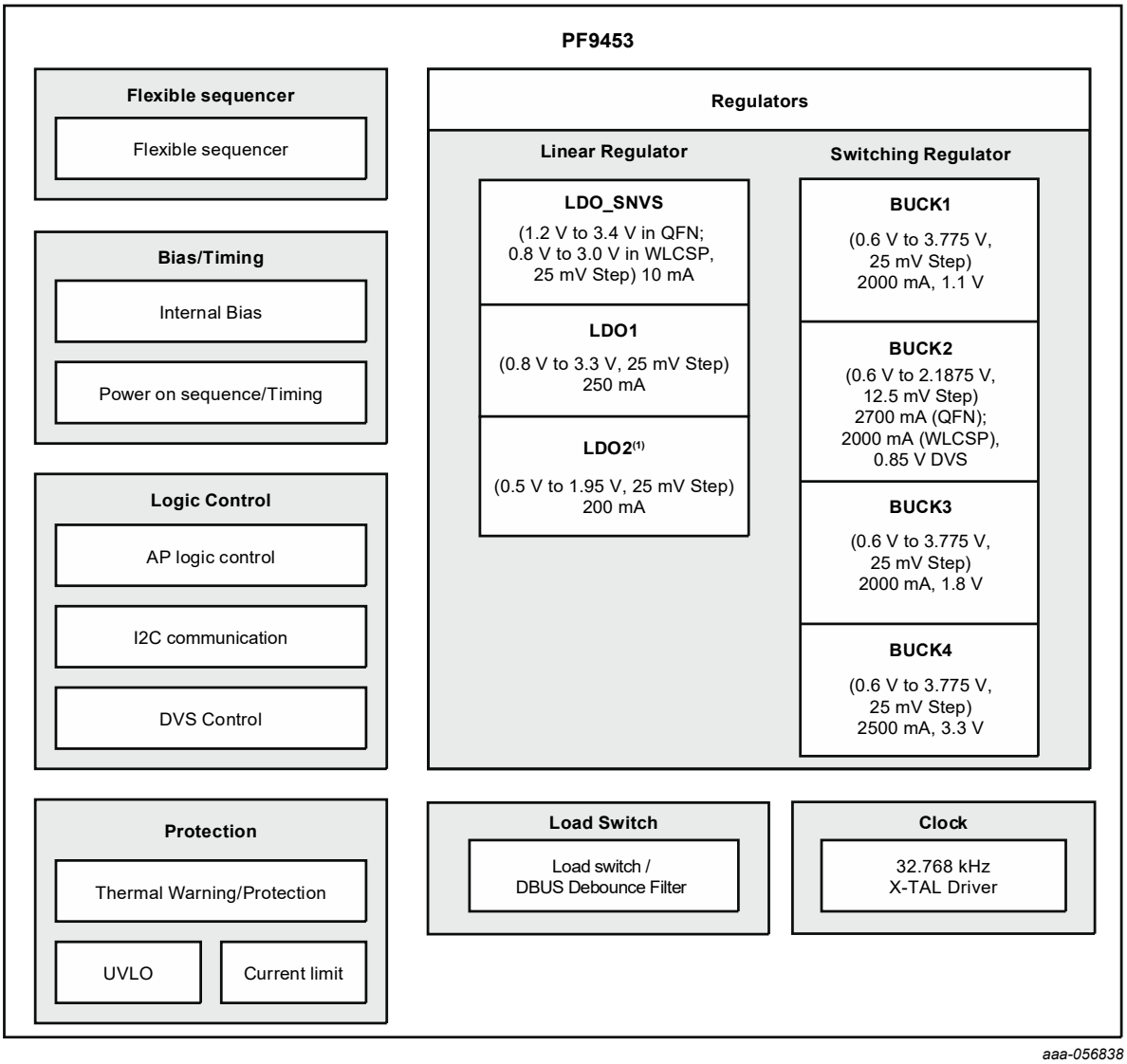
Symbol	Pin	Type	Description
LDO1	A6	P	LDO1 output. Bypass with 2 x 4.7 µF to Ground.
LDO_SNVS	B4	P	LDO_SNVS output pin, bypass with a 2.2 µF to Ground.
POR_B	E5	DO	Power On reset output pin. Open drain output requiring external pull up resistor.
IRQ_B	E3	DO	PMIC interrupt pin, open drain output requiring external pull up resistor
VSYS	A5	P	Internal power input. Bypass with a 1 µF to Ground
XTAL_IN	F4	AI	32.768kHz crystal oscillator input, tie to GND if XTAL is not used

Table 3. Pin description - PF9453AUK*...continued*

Symbol	Pin	Type	Description
XTAL_OUT	F3	AO	32.768kHz crystal oscillator output, leave float if XTAL is not used
CLK_32K_OUT	C3	DO	32.768kHz clock CMOS output with LDO_SNVS power rail.
BUCK4FB	F2	AI	Buck 4 feedback pin
PGND4	F1	P	Buck 4 Power ground
LX4	E1, E2	P	Buck 4 switching node
INB34	D1, D2	P	Buck 3 and Buck 4 input pins, bypass with 2 x 10 µF
LX3	C1	P	Buck 3 switching node
BUCK3FB	B2	AI	Buck 3 feedback pin
PGND3	B1	P	Buck 3 Power ground
LSWIN	A2	P	Load Switch input pin. Bypass with a 1 µF to Ground.
LSWOUT	A1	P	Load Switch output pin. Bypass with a 1 µF to Ground.
SCL	D4	DI	I^2C serial clock pin
SDA	C4	DIO	I^2C serial data pin
BUCK2FB	B5	AI	Buck 2 feedback pin
LX2	C6	P	Buck 2 switching node
PGND2	B6	P	Buck 2 Power ground
INB12	D5, D6	P	Buck 1 and Buck 2 input pins, bypass with 2 x 10 µF
LX1	E6	P	Buck 1 switching node
BUCK1FB	F5	AI	Buck 1 feedback pin
PGND1	F6	P	Buck 1 Power ground
WDOG_B	D3	DI	Watchdog reset input from application processor.
PMIC_STBY_REQ	C5	DI	Standby mode input from application processor. When it is asserted high, device enters STANDBY mode.
PMIC_ON_REQ	E4	DI	PMIC ON input from application processor. When it is asserted high, the device starts power on sequence.
VINT	A4	P	Internal power supply output, bypass with a 1 µF to GND.
SD_VSEL	B3	DI	LDO1 voltage selection input pin. LDO1 outputs voltage set by L1_OUT_L[6:0] when it is driven low and L1_OUT_H[6:0] when driven high.
LSW_EN	C2	DI	Load switch enable input pin. It has internal 1.5Mohm pull down resistor.
AGND	A3	P	Analog ground pin. It should be connected to ground plane through Via.

7 Functional description

7.1 Functional diagram



(1) QFN only

Figure 5. PF9453xHN functional block diagram

7.2 PF9453 OTP version

The PF9453 can be configured to each regulator default voltage and start-up sequence from the internal OTP configuration. Table 4 shows power up sequence.

Table 4. Power up sequence

Regulator	PF9453AHN	PF9453AUK	PF9453BUK
LDO_SNVS	1.8V, always-on	1.8V, always-on	1.8V, always-on
BUCK1	T4, 1.1 V	T4, 1.1V	T4, 1.1V

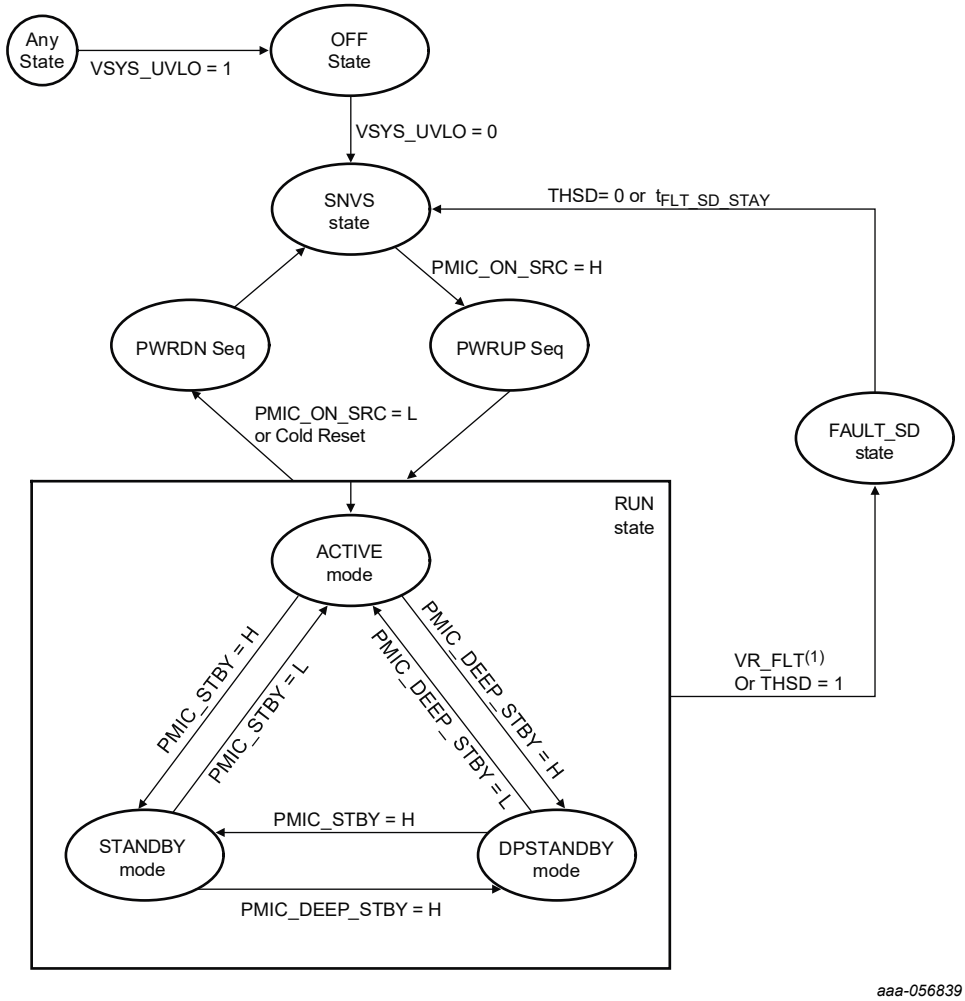
Table 4. Power up sequence*...continued*

Regulator	PF9453AHN	PF9453AUK	PF9453BUK
BUCK2	T1, 0.85 V	T1, 0.85V	T1, 0.85V
BUCK3	T3, 1.8 V	T3, 1.8V	T3, 1.8V
BUCK4	T5, 3.3 V	T5, 3.3V	T5, 3.3V
LDO1	T6, 3.3 V / 1.8 V	T2, 0.8 V	T2, 0.8 V
LDO2[1]	T2, 0.8V	n/a	n/a
Load Switch	T5	-	T5

[1] Not available in WLCSP

7.3 Power states

PF9453 has six power states: OFF, SNVS, RUN, PWRDN, PWRUP and FAULT_SD. Figure 6 shows the state transition diagram showing the conditions to enter and exit each state.



1. VR_FLT does not include LDO_SNVS.

Figure 6. Power states diagram

8 Application design-in information

8.1 Reference schematic

8.2 PF9453 Reference schematic

PF9453 (HVQFN40 and WLCSP36 package) reference schematics with i.MX 91 processor are illustrated in Figure 7 and Figure 8.

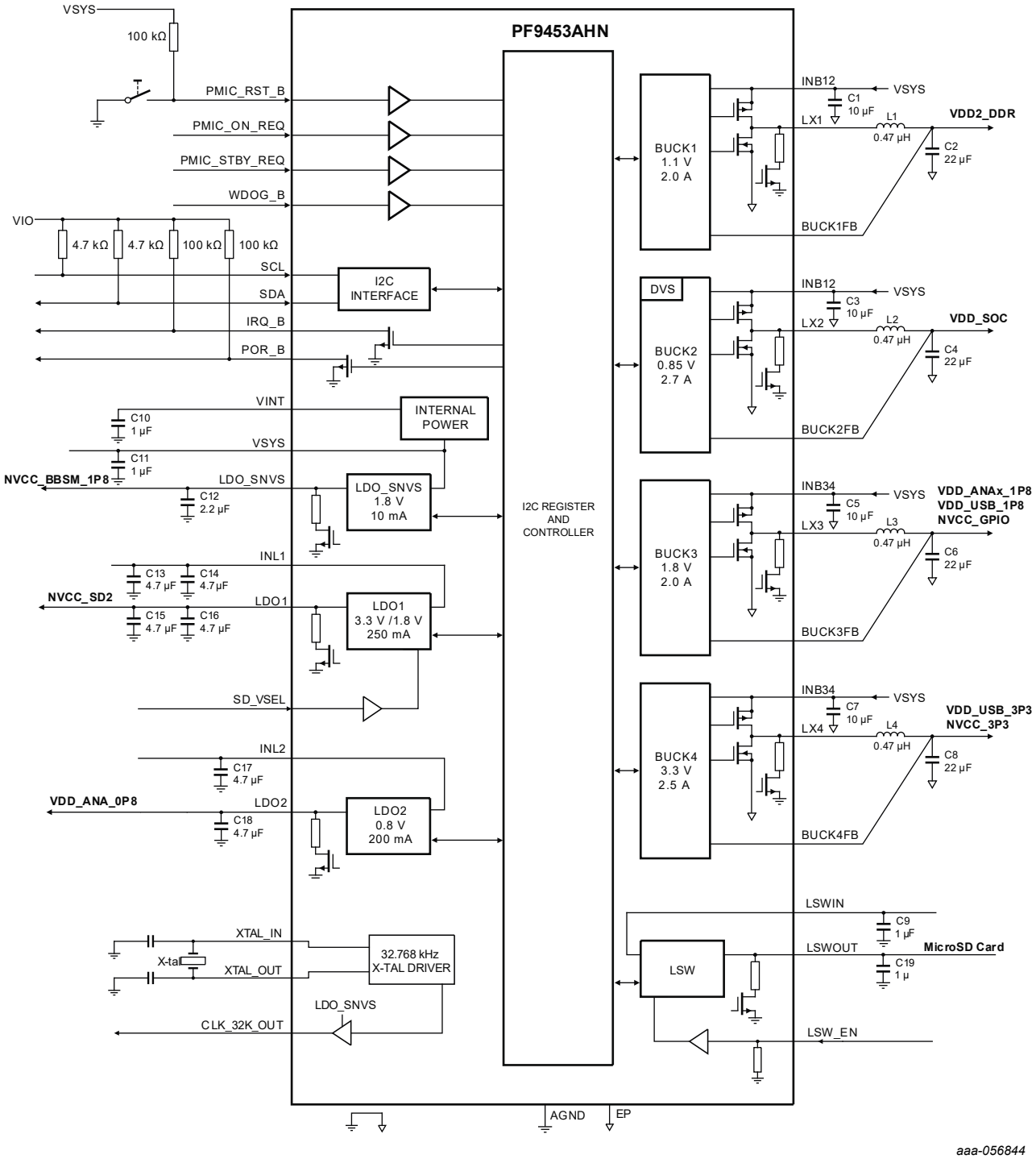


Figure 7. PF9453AHN application schematic

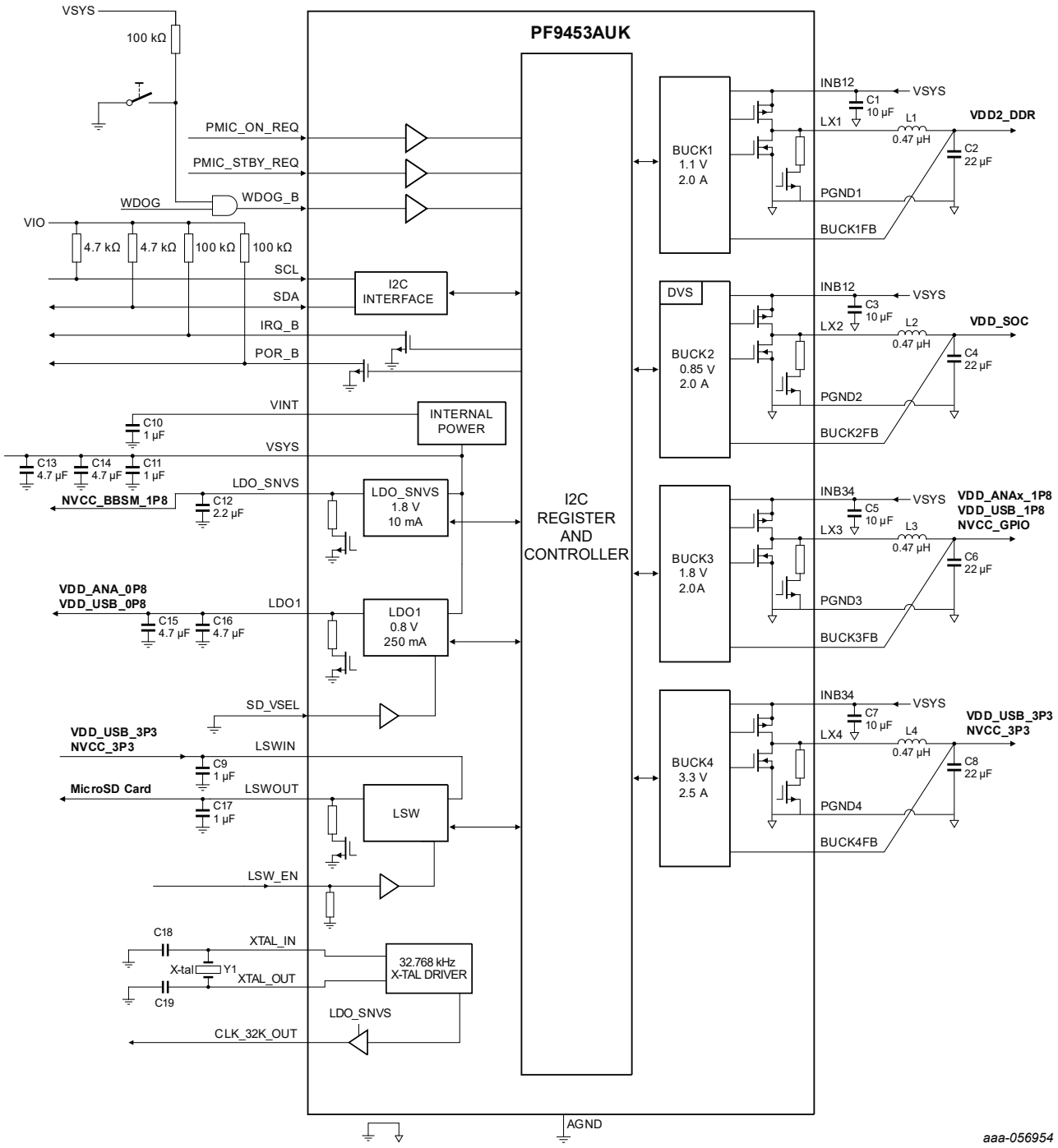


Figure 8. PF9453AUK application schematic

8.3 Layout guide

Figure 9 and Figure 10 show layout guidance.

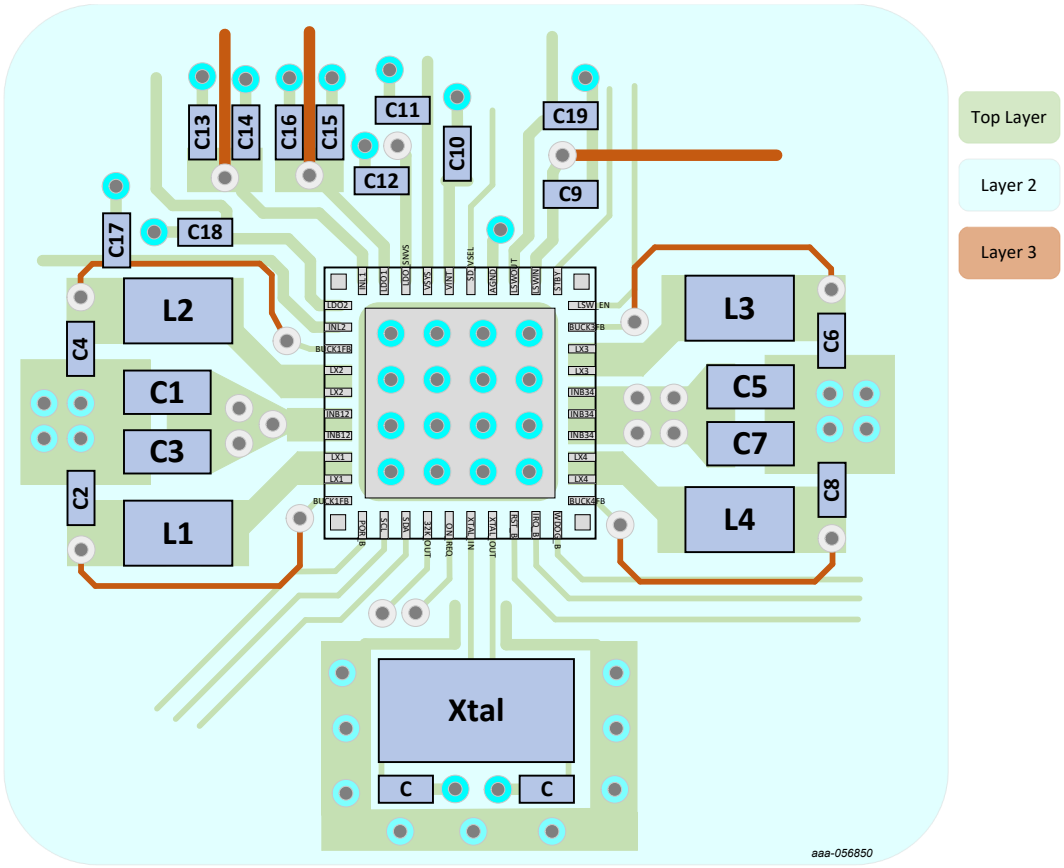


Figure 9. PF9453AHN layout

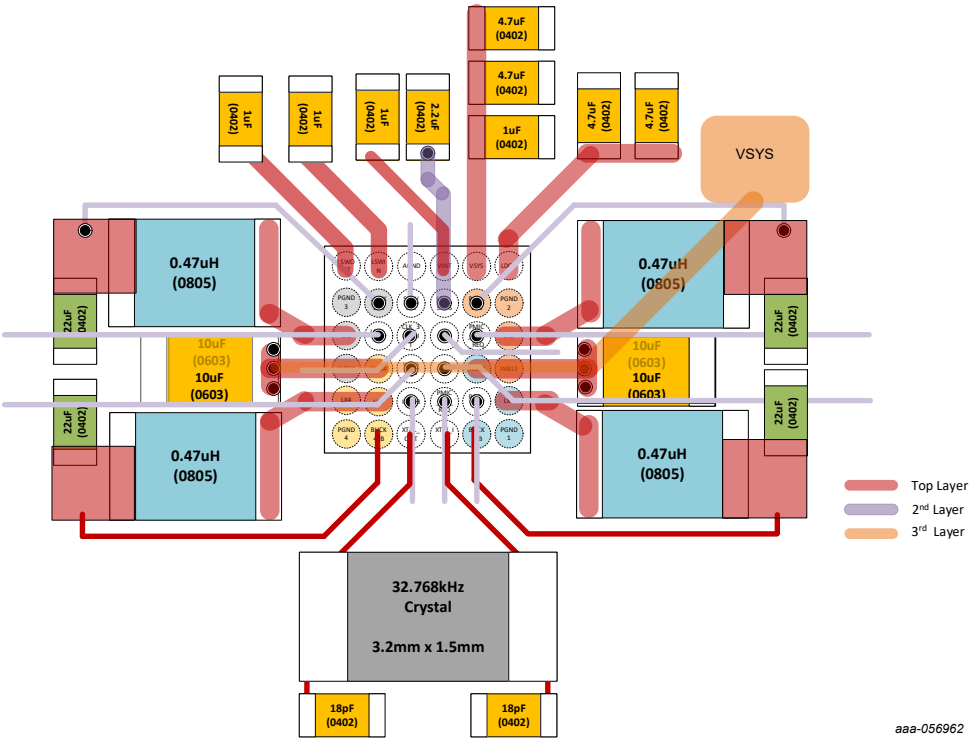


Figure 10. PF9453AUK layout

9 PF9453 QFN/WLCSP OTP version

The PF9453 can be configured to each regulator default voltage and start-up sequence from the internal OTP configuration. Table 5 shows each OTP configuration for all devices.

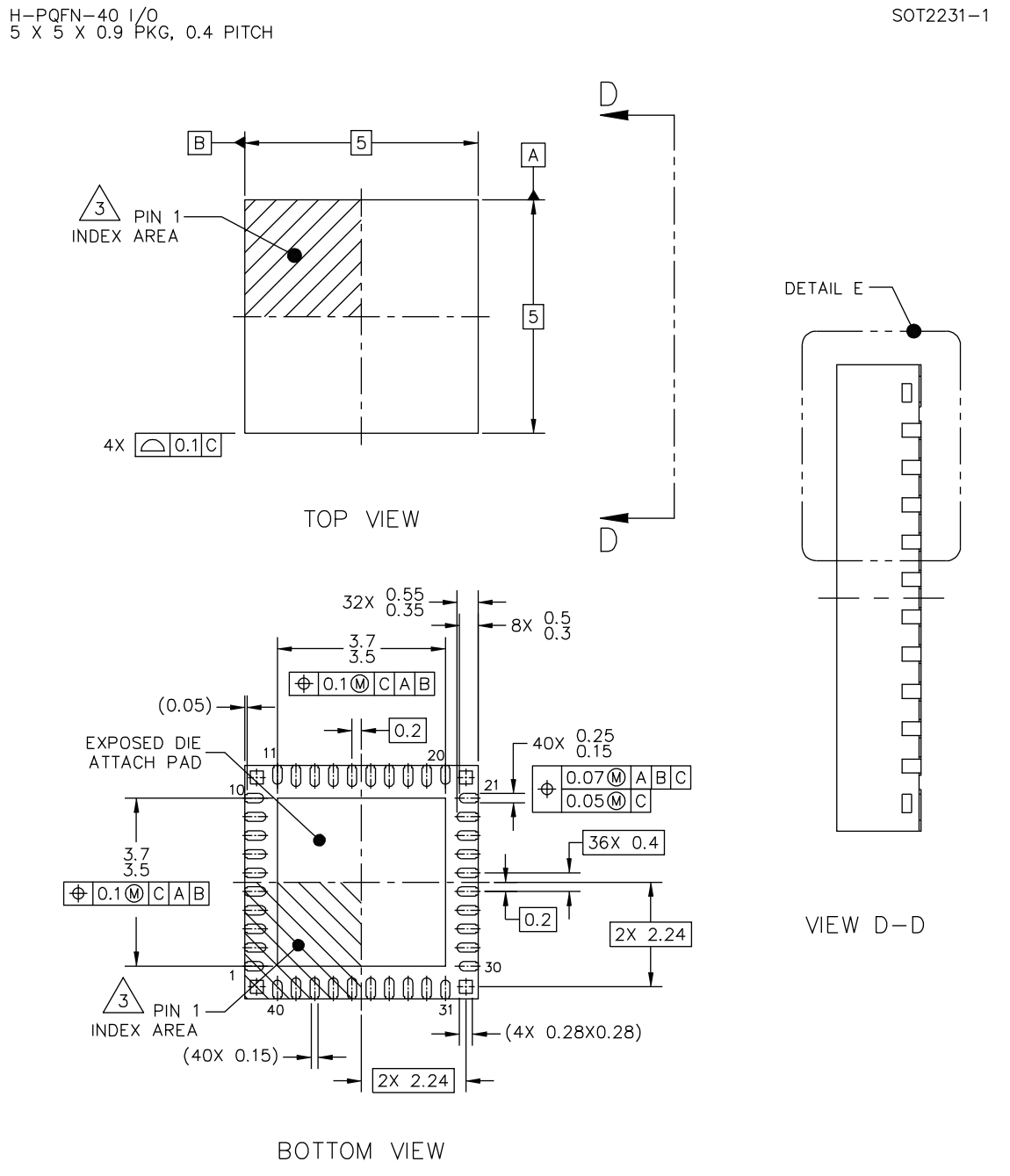
Table 5. OTP configuration

Register	Pre-programmed OTP configuration		
	PF9453AHN	PF9453AUK	PF9453BUK
OTP_LDO_SNVS	1.80 V	1.80 V	1.80 V
OTP_BUCK1_VOUT	1.10 V	1.10 V	1.10 V
OTP_BUCK1_SEQ	T4	T4	T4
OTP_BUCK2_VOUT	0.85 V	0.85 V	0.85 V
OTP_BUCK2_SEQ	T1	T1	T1
OTP_BUCK2_VOUT_MAX	1.3 V	0.90 V	0.90 V
OTP_BUCK2_VOUT_MIN	0.7 V	0.6125 V	0.6125 V
OTP_BUCK2_DVS_SPEED	25 mV / 2 µs	25 mV / 2 µs	25 mV / 2 µs
OTP_BUCK3_VOUT	1.80 V	1.80 V	1.80 V
OTP_BUCK3_SEQ	T3	T3	T3
OTP_BUCK4_VOUT	3.30 V	3.30 V	3.30 V
OTP_BUCK4_SEQ	T5	T5	T5
OTP_LDO1_VOUT_L	3.30 V	0.80 V	0.80 V
OTP_LDO1_VOUT_H	1.80 V	0.80 V	0.80 V
OTP_LDO1_SEQ	T6	T2	T2
OTP_LDO2_VOUT	0.80 V	n/a	n/a
OTP_LDO2_SEQ	T2	n/a	n/a
LOAD SWITCH / DBUS Debounce Filter Configuration, OTP_LSW_CONFIG	LOAD SWITCH	DBUS Debounce Filter	LOAD SWITCH
DBUS Filter Debounce Time, OTP_DBUS_DEB	-	5 ms	-
Load Switch SEQ, OTP_LSW_SEQ	T5	-	T5
PU CONFIG, OTP_PSQ_TON_STEP	2 ms	2 ms	2 ms
PU CONFIG, OTP_PSQ_TOFF_STEP	8 ms	8 ms	8 ms
BUCK1 Force PWM mode, OTP_BUCK1_FPWM	Auto	Auto	Auto
BUCK2 Force PWM mode, OTP_BUCK2_FPWM	Auto	Auto	Auto
BUCK3 Force PWM mode, OTP_BUCK3_FPWM	Auto	Auto	Auto
BUCK4 Force PWM mode, OTP_BUCK4_FPWM	Auto	Auto	Auto
BUCK1 Active Discharge, OTP_BUCK1_AD	Enabled	Enabled	Enabled
BUCK2 Active Discharge, OTP_BUCK2_AD	Enabled	Enabled	Enabled

Table 5. OTP configuration*...continued*

Register	Pre-programmed OTP configuration		
	PF9453AHN	PF9453AUK	PF9453BUK
BUCK3 Active Discharge, OTP_BUCK3_AD	Enabled	Enabled	Enabled
BUCK4 Active Discharge, OTP_BUCK4_AD	Enabled	Enabled	Enabled
LDO_SNVS Active Discharge, OTP_LDO_SNVS_AD	Enabled	Enabled	Enabled
LDO1 Active Discharge, OTP_LDO1_AD	Enabled	Enabled	Enabled
LDO2 Active Discharge, OTP_LDO2_AD	Enabled	n/a	n/a
Load Switch Active Discharge, OTP_LSW_AD	Enabled	Enabled	Enabled
OTP_VSYS_UVLO	2.85 V	2.85 V	2.85 V
Cold Reset Duration, OTP_TRESTART	250ms	250 ms	250ms

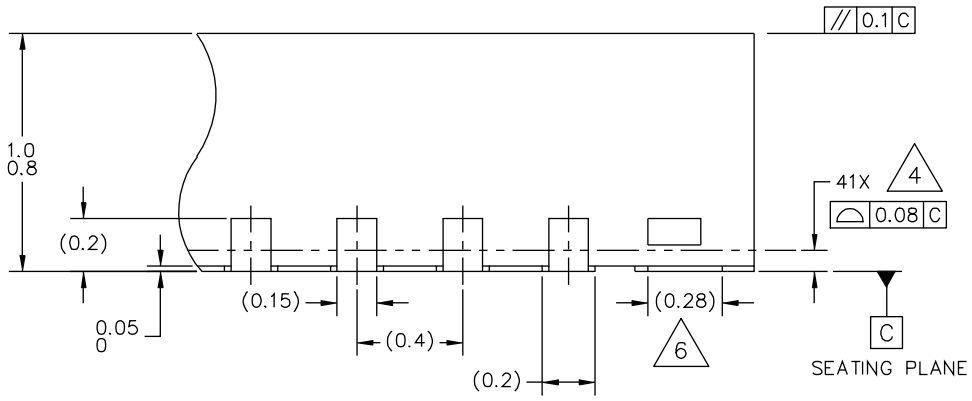
10 Package outline



DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 11. Package outline SOT2231-1 (HVQFN40)



DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 12. Package outline SOT2231-1 (HVQFN40) detail E

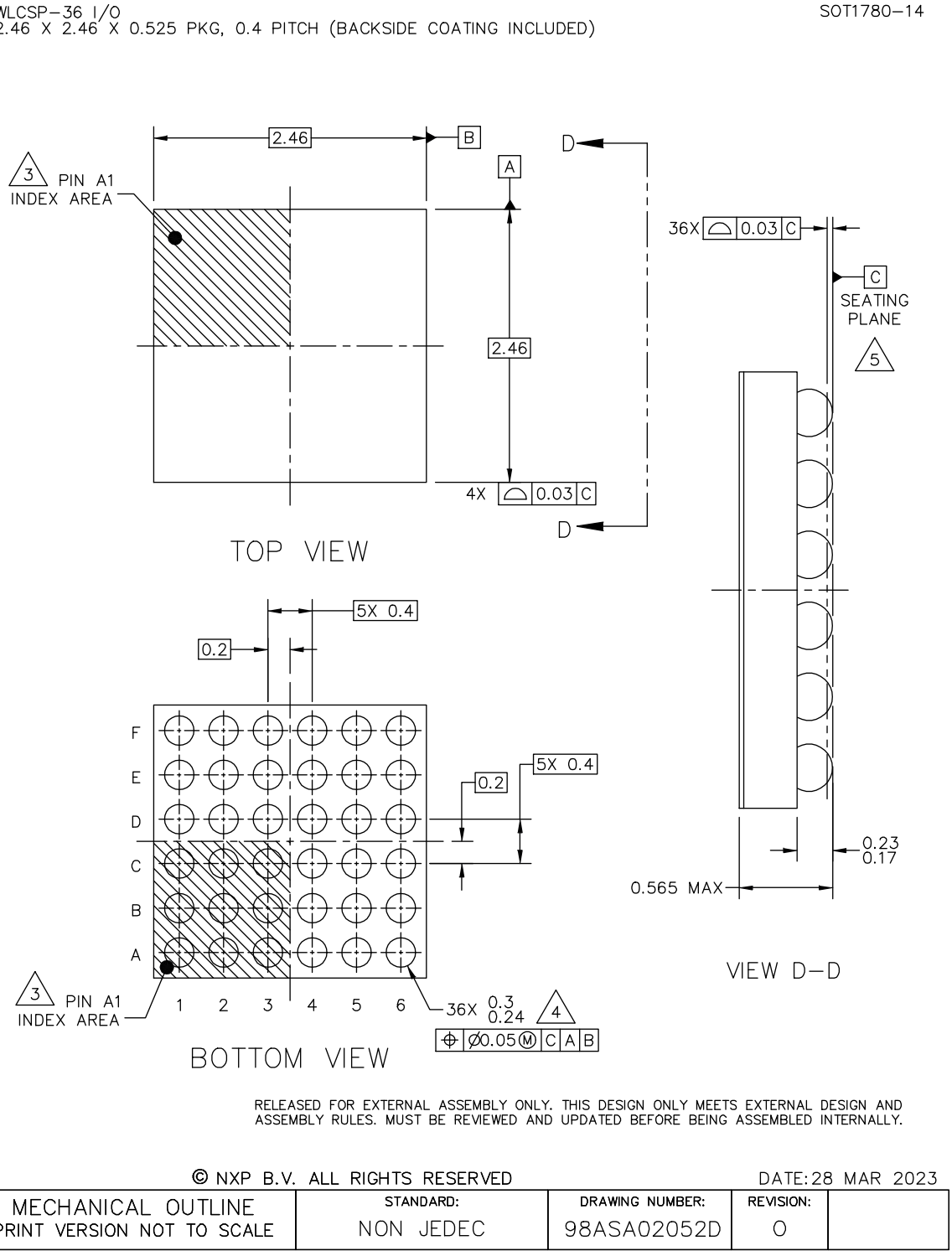
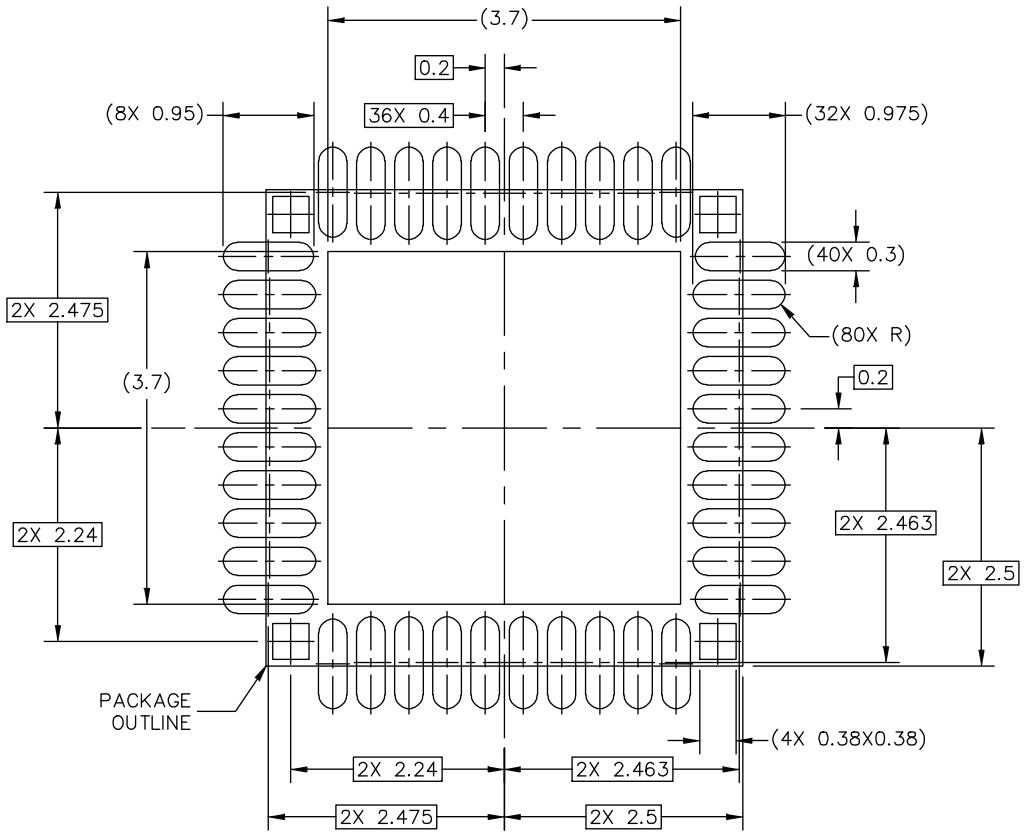


Figure 13. Package outline SOT1780-14 (WLCSP36)

11 Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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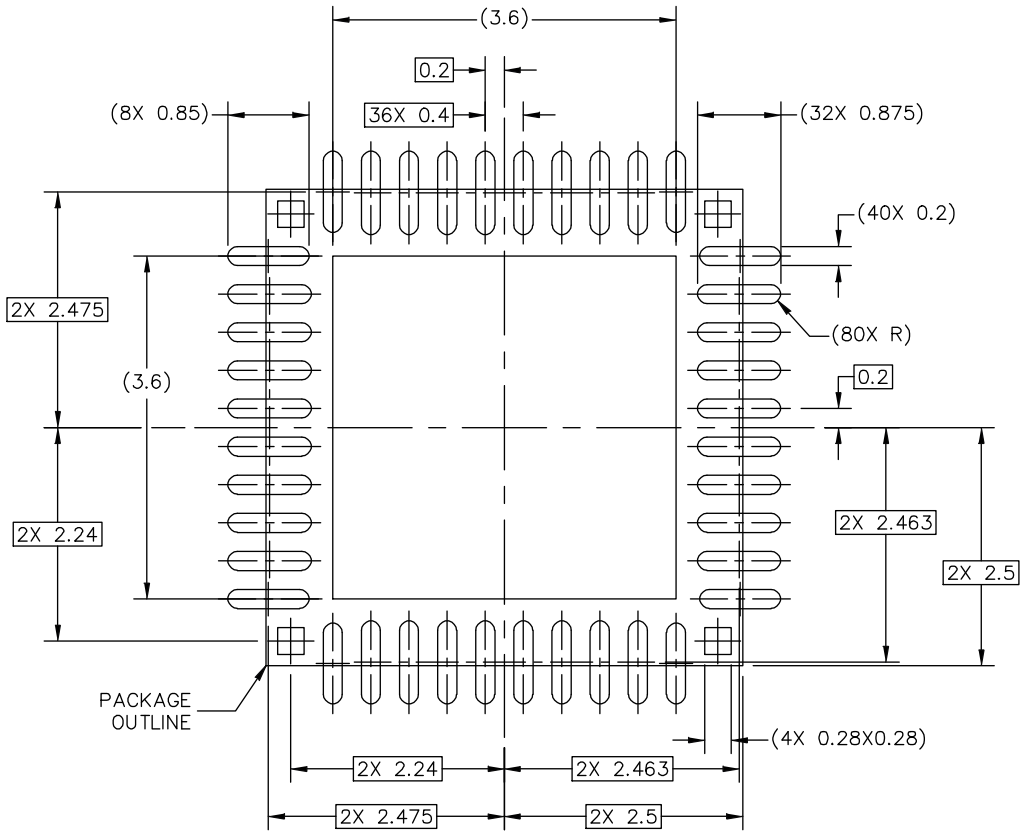
Figure 14. SOT2231-1 solder mask opening pattern



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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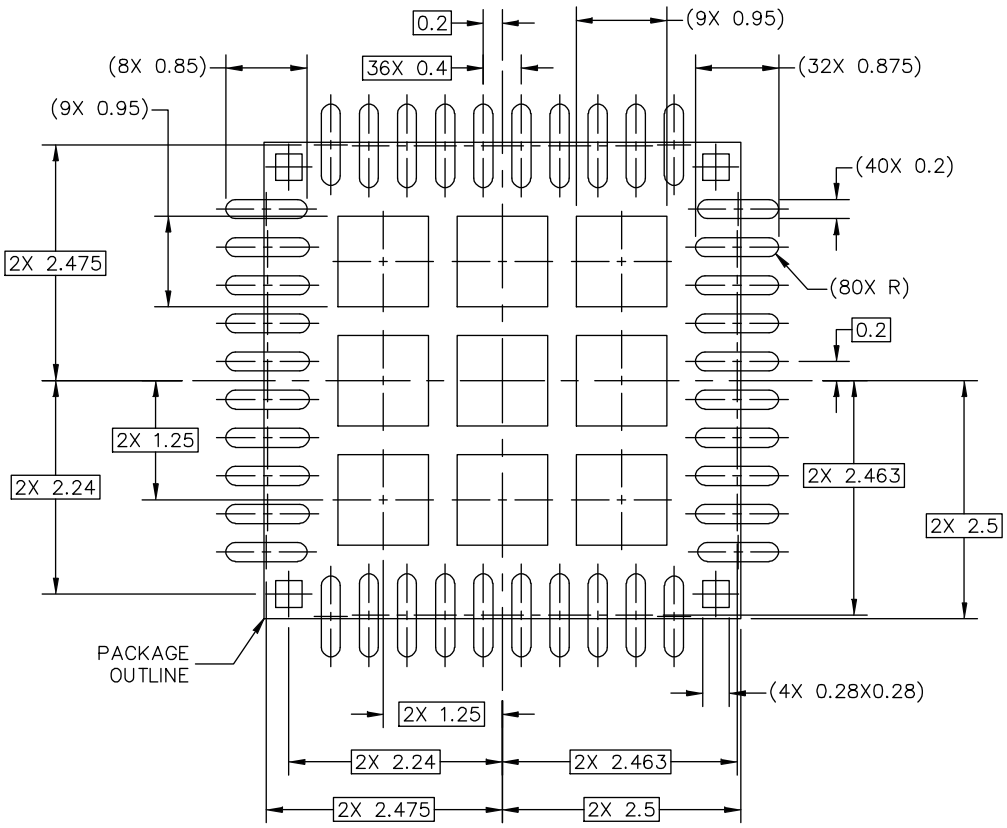
Figure 15. SOT2231-1 I/O pads and solderable area



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 16. SOT2231-1 solder paste stencil

Figure 17. SOT2231-1 notes

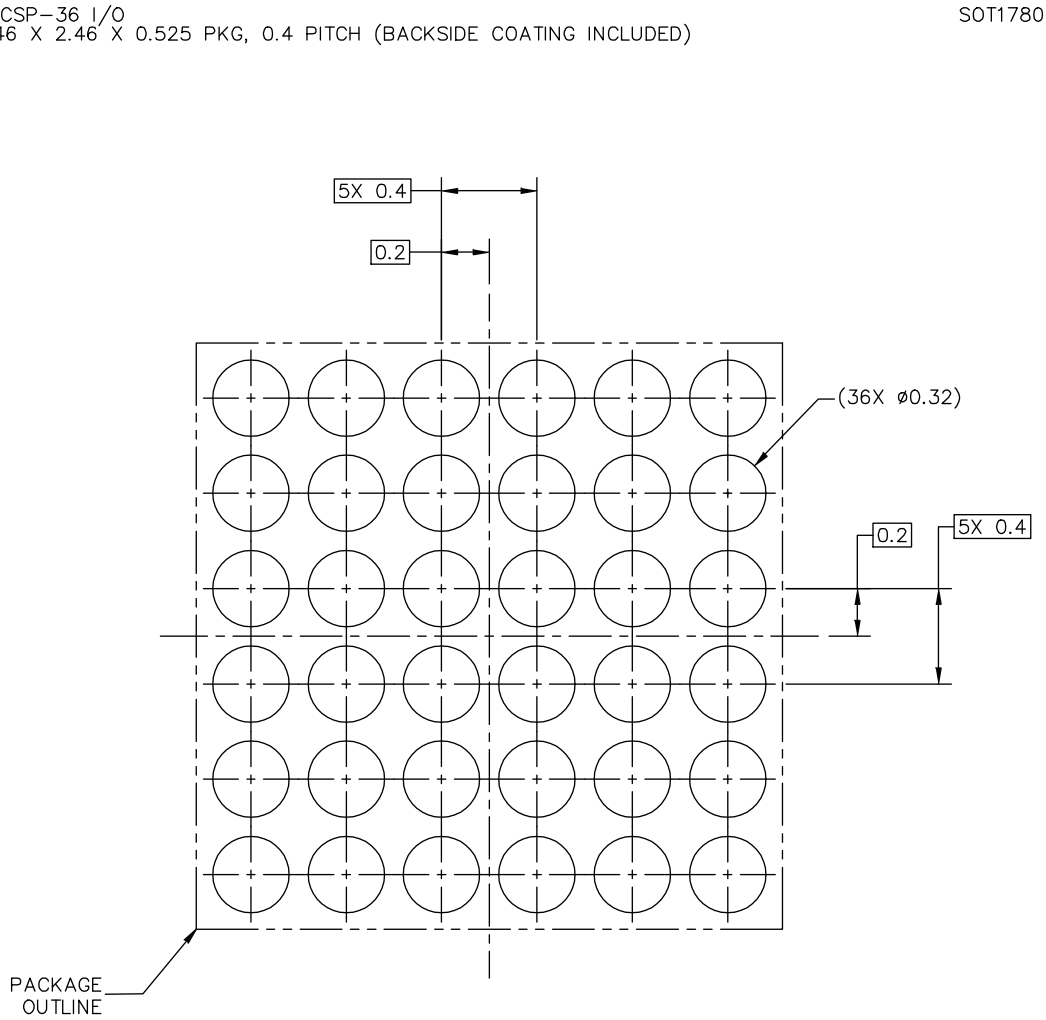
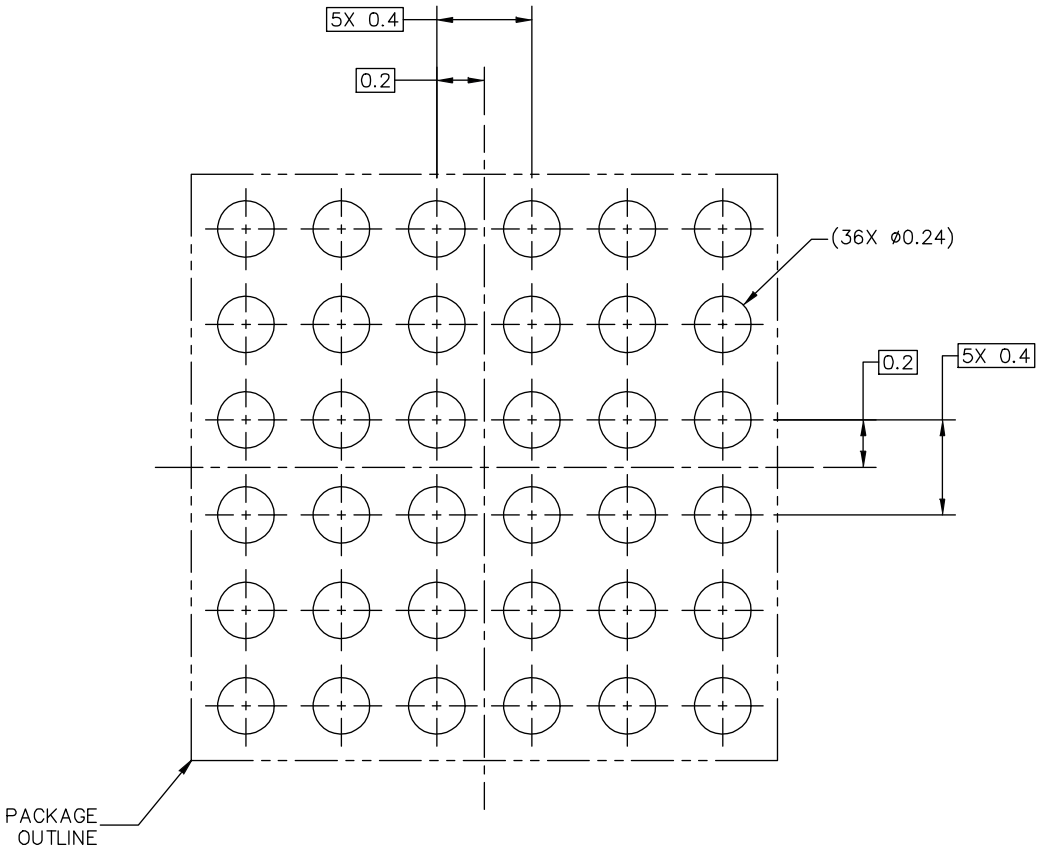


Figure 18. SOT1780-14 solder mask opening pattern

WLCSP–36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780–14



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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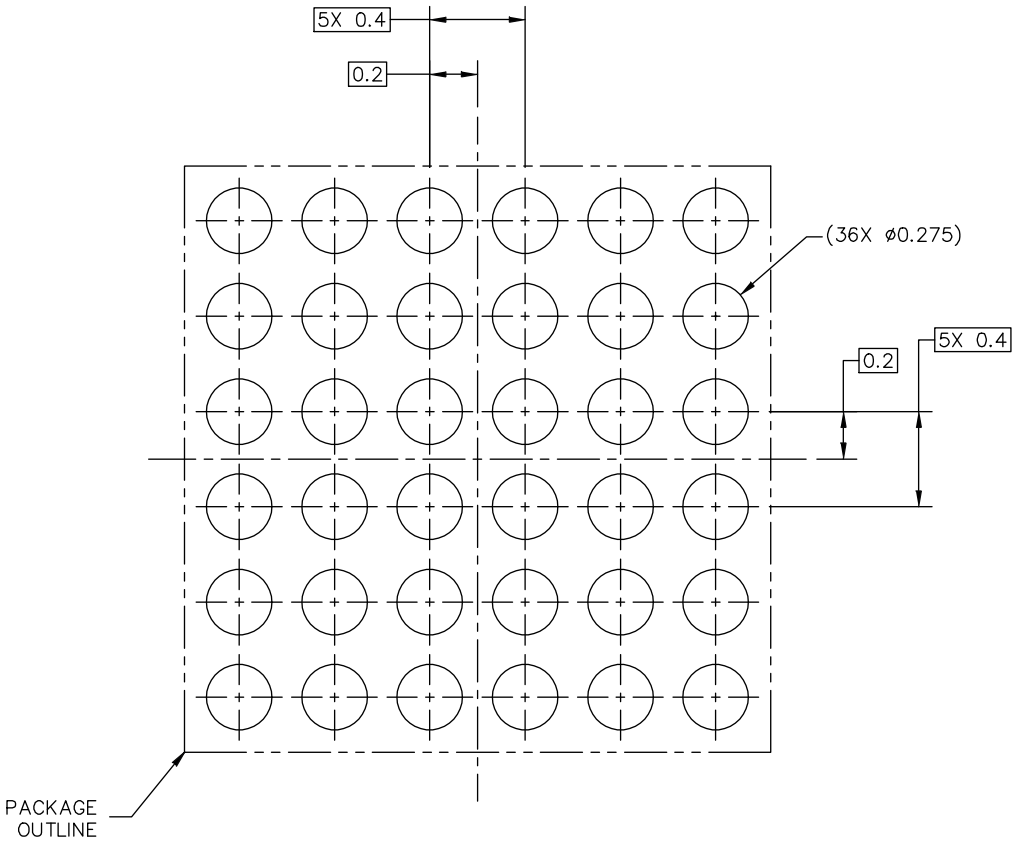
DATE: 28 MAR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02052D	REVISION: O	

Figure 19. SOT1780-14 I/O pads and solderable area

WLCSP–36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780–14



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 28 MAR 2023

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Figure 20. SOT1780-14 solder paste stencil

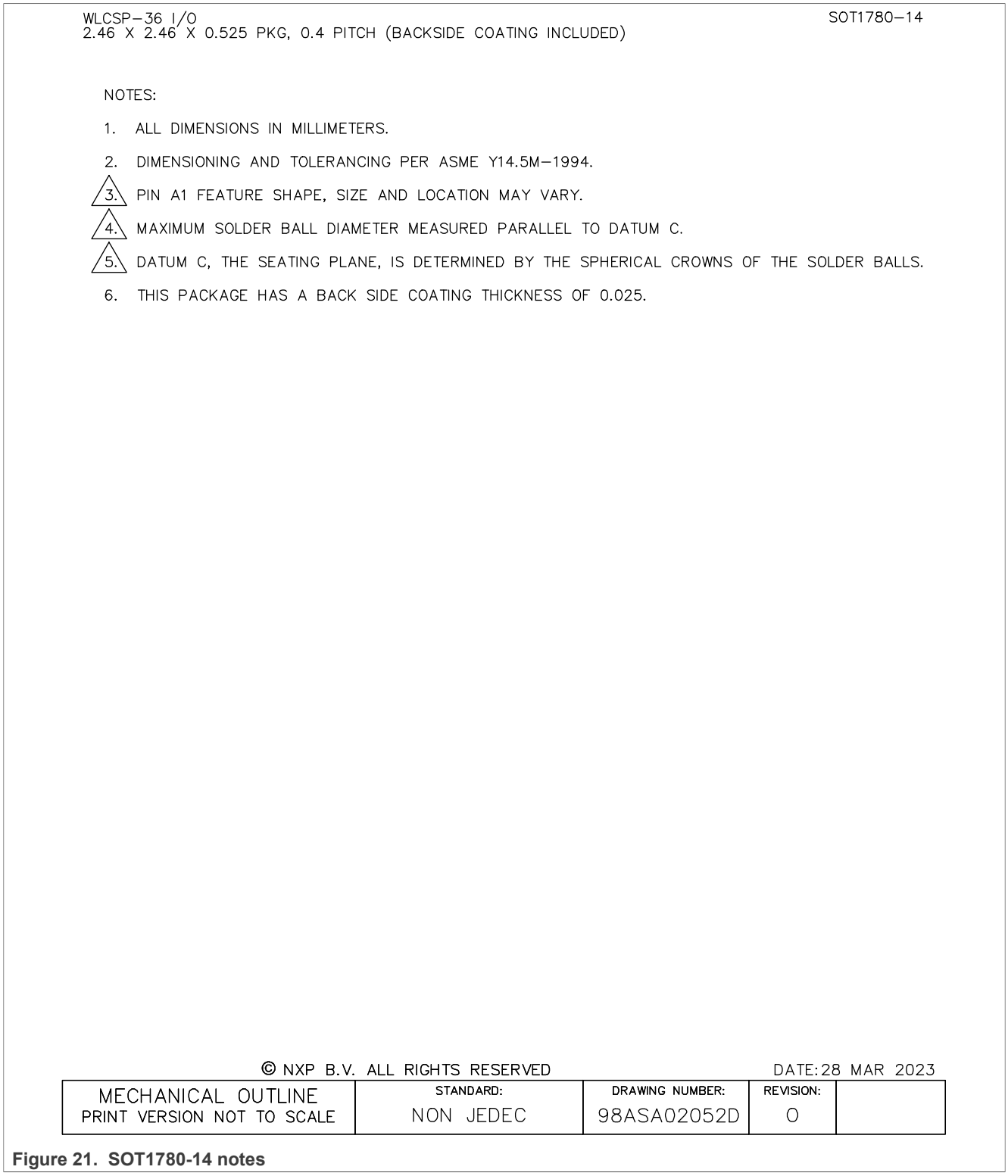

Figure 21. SOT1780-14 notes

12 Revision history

Table 6. Revision history

Document ID	Release date	Description
PF9453_SDS v.1.0	14 August 2024	• Initial version

Legal information

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Document status[1][2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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