PCA9422

Power management IC for low-power microcontroller applications

Rev. 1.0 — 14 August 2024 Objective short data sheet

1 General description

The PCA9422 is a highly-integrated Power Management IC (PMIC), targeted to provide a full power management solution for low power microcontroller applications or other similar applications.

The device consists of a linear battery charger capable of charging up to 640 mA current. It has an I^2C programmable Constant Current (CC) and Constant Voltage (CV) values for flexible configuration. Various built-in protection features such as input overvoltage protection, overcurrent protection, thermal protection, etc. are also provided for safe battery charging. It also features JEITA compliant charging.

The device also integrates three step-down DC/DC converters (bucks) which have I^2C programmable output voltage. All buck regulators have integrated high-side and low- side switches and related control circuitry, to minimize the external component counts, a Pulse-Frequency Modulation (PFM) approach is utilized to achieve better efficiency under light load condition. Other protection features such as overcurrent protection, under-voltage lockout (UVLO), etc. are also provided. By default, the input for these regulators is powered from either VIN or VBAT, whichever is greater.

One ultra-low quiescent Buck-Boost converter is designed to power system peripherals that require voltages higher and/or lower than the battery voltage, it seamlessly transitions between buck, buck-boost, and boost modes, minimizing discontinuities and subharmonics in the output voltage ripple.

In addition, four on-chip LDO regulators are provided to power up various voltage rails in the system. One LDO is for SNVS core power supply, two 200 mA NMOS LDOs with load switch feature are capable of regulating to low output voltage from buck regulator output. One 200 mA PMOS LDO is purposed to supply power to microcontroller or peripheral devices.

Other features such as FM+ I^2C-bus interface, chip enable, interrupt signal, OTP configurations etc. are also provided.

The chip is offered in 2.90 mm x 3.00 mm, 7 x 7 bump, 0.4 mm pitch WLCSP package.

2 Features and benefits

- Linear battery charger for charging single cell Li-Ion battery
  - 26 V tolerance on VIN pin
  - Programmable input OVP (5.75 V)
  - Programmable constant current (up to 640 mA) and pre-charge low voltage current threshold
  - Programmable constant voltage regulation
  - Programmable automatic recharge voltage and termination current threshold
  - Built-in protection features such as input OVP (Over Voltage Protection), battery OCP (Over Current Protection), thermal protection
  - JEITA compliant
  - Battery attached detection
  - Over-temperature protection
- Three step-down DC/DC converters
  - Very low quiescent current
  - Programmable output voltage
  - SW1: core buck converter, 0.4 V~1.975 V output, 6.25 mV/step, up to 300 mA
  - SW2: system buck converter, 0.4 V~3.4 V output, 25 mV/step, up to 500 mA
  - SW3: core buck converter, 0.4 V~1.975 V output, 6.25 mV/step, up to 300 mA
  - Low power mode for extra power saving
- One Buck-Boost converter
  - Ultra-low quiescent current
  - High-efficient Boost mode
  - Seamlessly transition between Buck, Boost and Buck-Boost modes
  - 2.5 V~5.5 V input and 1.8 V~5.0 V output, 25 mV/step, up to 500 mA
- Four LDOs
  - Programmable output voltage regulation
  - LDO1: always-on LDO, 0.8 V~3.0 V output, 25 mV/step, up to 10 mA
  - LDO2: system LDO/Load switch, 0.5 V~1.95 V output, 25 mV/step, up to 200 mA
  - LDO3: system LDO/Load switch, 0.5 V~1.95 V output, 25 mV/step, up to 200 mA
  - LDO4: LDO, 0.8 V~3.3 V output, 25 mV/step, up to 200 mA
- 1 MHz I^2C-bus slave interface
- -40 °C to +85 °C ambient temperature range
- Offered in 7 x 7 bump-array WLCSP

3 Applications

- Low power microcontroller application
- Wearable Devices
- IoT

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package			Processor
		Name	Description	Version	
PCA9422AUK	PCA9422A	WLCSP49	Wafer Level Chip Scale Package, 49 terminals, 0.4 mm pitch, 2.90 mm x 3.00 mm x 0.57 mm body	SOT1444-13	i.MX RT500/RT600
PCA9422BUK	PCA9422B	WLCSP49	Wafer Level Chip Scale Package, 49 terminals, 0.4 mm pitch, 2.90 mm x 3.00 mm x 0.57 mm body	SOT1444-13	i.MX RT700

Details of the OTP programming for each device can be found in Table 5.

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9422AUK	PCA9422AUKZ	WLCSP49	REEL 7" Q1 DP CHIPS	3000	-40°C to +85°C
PCA9422BUK	PCA9422BUKZ	WLCSP49	REEL 7" Q1 DP CHIPS	3000	-40°C to +85°C

5 Simplified block diagram

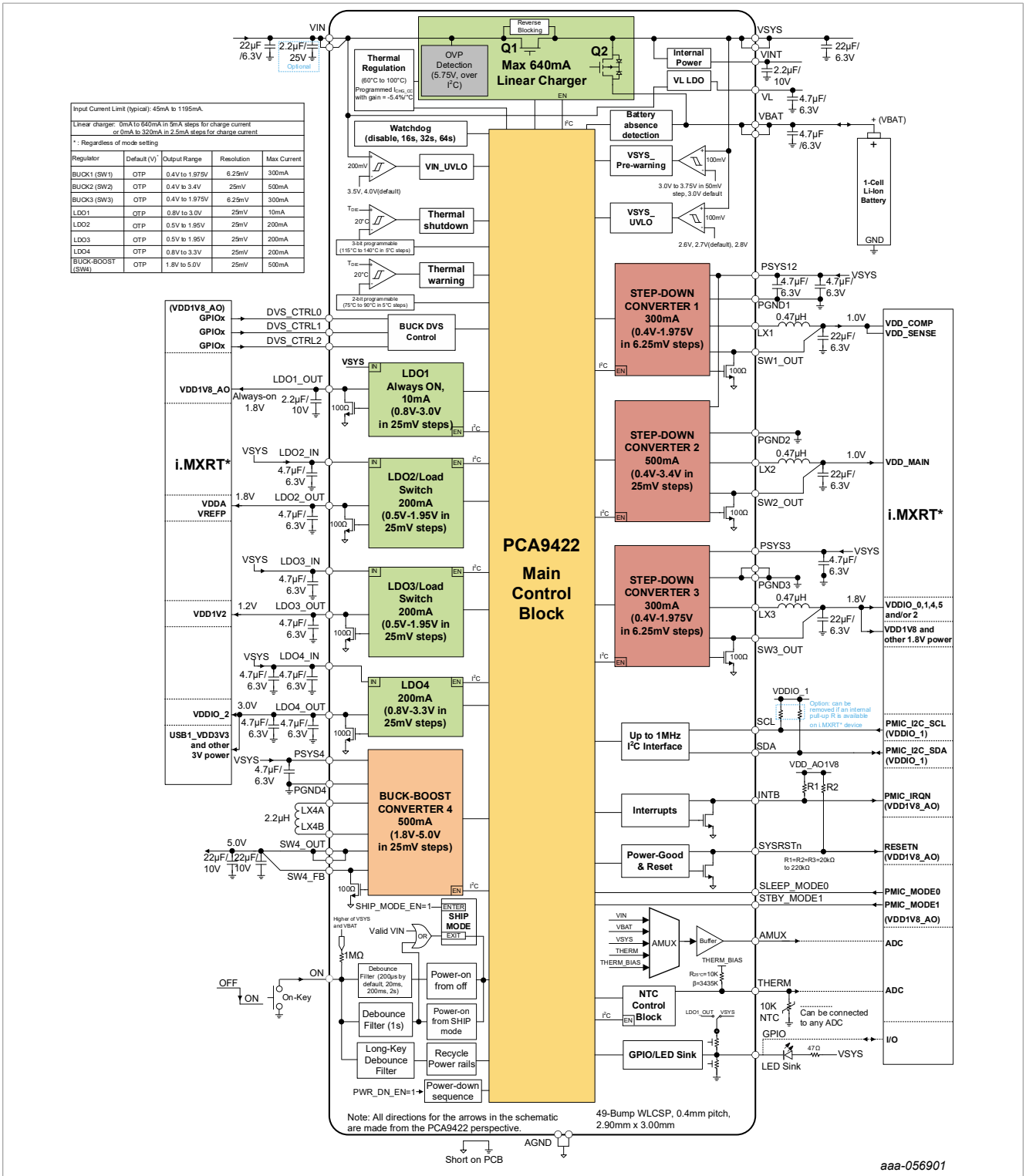


Figure 1. Block diagram

6 Pinning information

6.1 Pinning

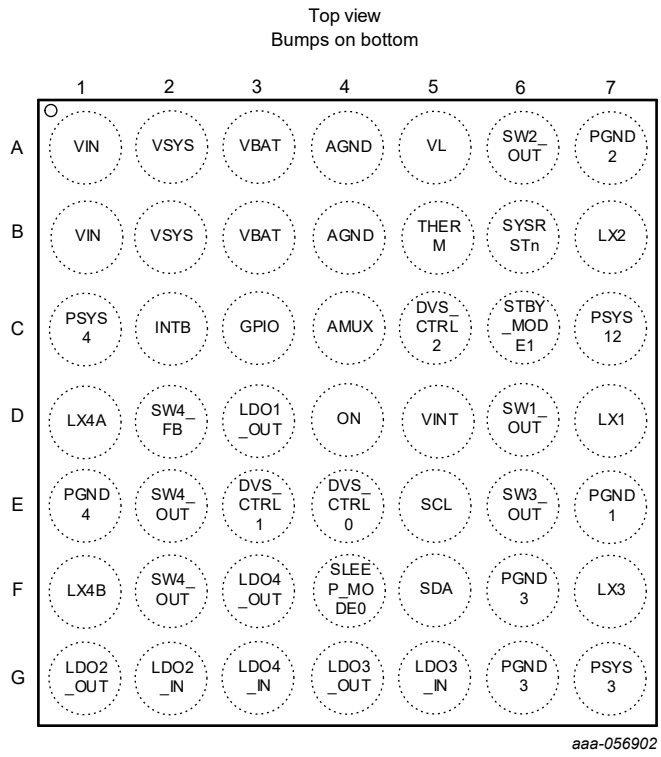


Figure 2. PCA9422UK pinout (WLCSP49) – top view

6.2 Pin description

Table 3. Pin description

Symbol	Pin WLCSP49	Pin Type	Description
INPUT SUPPLY			
VIN	A1, B1	P	Input supply voltage. Bypass with a 4.7µF/6.3V ceramic capacitor and a 2.2µF/25V capacitor (optional).
VSYS	A2, B2	P	Bypass output of VIN, connect with a typical 22µF/10V decoupling capacitor.
VINT	D5	P	Internal power supply output, bypass with 2.2µF/10V to GND.
LINEAR CHARGER			
VBAT	A3, B3	P	Battery (+) connection point. One typical 4.7µF/6.3V decoupling capacitor should be connected between VBAT to system ground.
VL	A5	P	Internal charger 3.0V logic supply powered from VIN. Bypass with a 4.7µF/6.3V ceramic capacitor.
THERM	B5	I	Battery temperature sensing pin. An external 10K ohm thermistor is connected between THERM pin and system ground.

Table 3. Pin description...*continued*

Symbol	Pin WLCSP49	Pin Type	Description
BUCK1 STEP_DOWN CONVERTER (SW1)			
PSYS12	C7	P	Input supply for SW1 and SW2. Bypass with two typical 4.7µF/6.3V ceramic capacitors. Connect to VSYS power domain as short as possible in the system.
LX1	D7	P	Switching node for SW1. Connect to a 0.47µH inductor.
SW1_OUT	D6	I	Feedback pin. Bypass with a 22µF/6.3V ceramic capacitor.
PGND1	E7	P	Power ground for buck 1 (SW1). Connect ground nodes of bypass capacitors for PSYS12 and SW1_OUT as close to PGND1 pin as possible in the system.
BUCK2 STEP_DOWN CONVERTER (SW2)			
LX2	B7	P	Switching node for SW2. Connect to a 0.47µH inductor.
SW2_OUT	A6	I	Feedback pin. Bypass with a 22µF/6.3V ceramic capacitor.
PGND2	A7	P	Power ground for buck 2 (SW2). Connect ground nodes of bypass capacitors for PSYS12 and SW2_OUT as close to PGND2 pin as possible in the system.
BUCK3 STEP_DOWN CONVERTER (SW3)			
PSYS3	G7	P	Input supply for SW3. Bypass with one typical 4.7µF/6.3V ceramic capacitor. Connect to VSYS power domain as short as possible in the system.
LX3	F7	P	Switching node for SW3. Connect to a 0.47µH inductor.
SW3_OUT	E6	I	Feedback pin. Bypass with a 22µF/6.3V ceramic capacitor.
PGND3	F6, G6	P	Power ground for buck 3 (SW3). Connect ground nodes of bypass capacitors for PSYS3 and SW3_OUT as close to PGND3 pin as possible in the system.
BUCK-BOOST CONVERTER (SW4)			
PSYS4	C1	P	Input supply for SW4. Bypass with a typical 4.7µF/6.3V ceramic capacitor. Connect to VSYS power domain as short as possible in the system.
LX4A	D1	P	Switching node for SW4. Connect to a 2.2µH inductor.
LX4B	F1	P	Switching node for SW4. Connect to a 2.2µH inductor.
SW4_OUT	E2, F2	P	SW4 output, bypass with two 22µF/10V ceramic capacitors.
SW4_FB	D2	I	SW4 feedback pin.
PGND4	E1	P	Power ground for SW4. Connect ground nodes of bypass capacitors for PSYS4 and SW4_OUT as close to PGND4 pin as possible in the system.
LOW_DROPOUT REGULATORS			
LDO1_OUT	D3	P	LDO1 output. It is always-ON supply. The input supply is VSYS internally. Bypass with a 2.2µF/10V ceramic capacitor.
LDO2_OUT	G1	P	LDO2 output. The input supply is VSYS. Bypass with a 4.7µF/6.3V ceramic capacitor.
LDO3_OUT	G4	P	LDO3 output. The input supply is VSYS. Bypass with a 4.7µF/6.3V ceramic capacitor.

Table 3. Pin description...*continued*

Symbol	Pin WLCSP49	Pin Type	Description
LDO4_OUT	F3	P	LDO4 output. The input supply is VSYS. Bypass with two 4.7µF/6.3V ceramic capacitors.
LDO2_IN	G2	P	LDO2 input. Bypass with a 4.7µF/6.3V ceramic capacitor.
LDO3_IN	G5	P	LDO3 input. Bypass with a 4.7µF/6.3V ceramic capacitor.
LDO4_IN	G3	P	LDO4 input. Bypass with two 4.7µF/6.3V ceramic capacitors.
LOGIC INPUTS			
ON	D4	I	ON pin with an internal pull-up resistor, 1MΩ typ, to higher of VSYS and VBAT.
SLEEP_MODE0	F4	I	SLEEP mode input or Mode selection input pin #0 from Application processor
STBY_MODE1	C6	I	STANDBY mode input or Mode selection input pin #1 from Application processor.
DVS_CTRL0	E4	I	BUCK DVS (Dynamic Voltage Scaling) control input pin #0
DVS_CTRL1	E3	I	BUCK DVS control input pin #1
DVS_CTRL2	C5	I	BUCK DVS control input pin #2
LOGIC OUTPUTS			
INTB	C2	O	Interrupt output, Open-drain type. Place a pull-up resistor from 20kΩ to 220kΩ to a system I/O supply rail.
SYSRSTn	B6	O	Reset output for external MCU, Open-drain type. Place a pull-up resistor from 20kΩ to 220kΩ to a system I/O supply rail.
LOGIC INPUTS AND OUTPUTS			
GPIO	C3	I/O	General Purpose IO or LED current sink channel. LED current sink channel is connected to the cathode of an LED and is capable of sinking up 6mA.
ANALOG OUTPUTS			
AMUX	C4	O	Analog multiplex output.
SERIAL I^2C INTERFACE			
SCL	E5	I	I^2C Interface clock pin. Place a pull-up resistor between 2.2kΩ and 10kΩ to a system I/O supply rail.
SDA	F5	I/O	I^2C Interface data pin. Place a pull-up resistor between 2.2kΩ and 10kΩ to a system I/O supply rail.
DEVICE GROUND			
AGND	A4, B4	P	Analog ground. It shall be connected to system ground through a via. Do not connect AGND to PGND1, PGND2, PGND3, or PGND4 on the top PCB layer in the system.

7 System block diagram

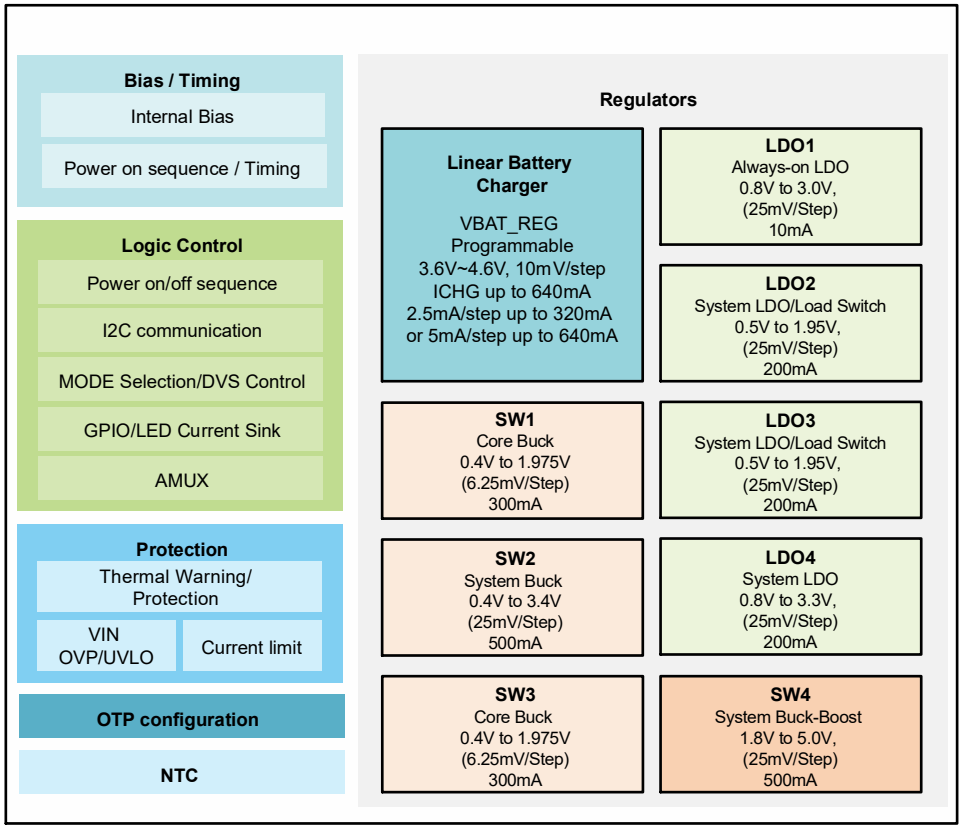


Figure 3. PCA9422 functional block diagram

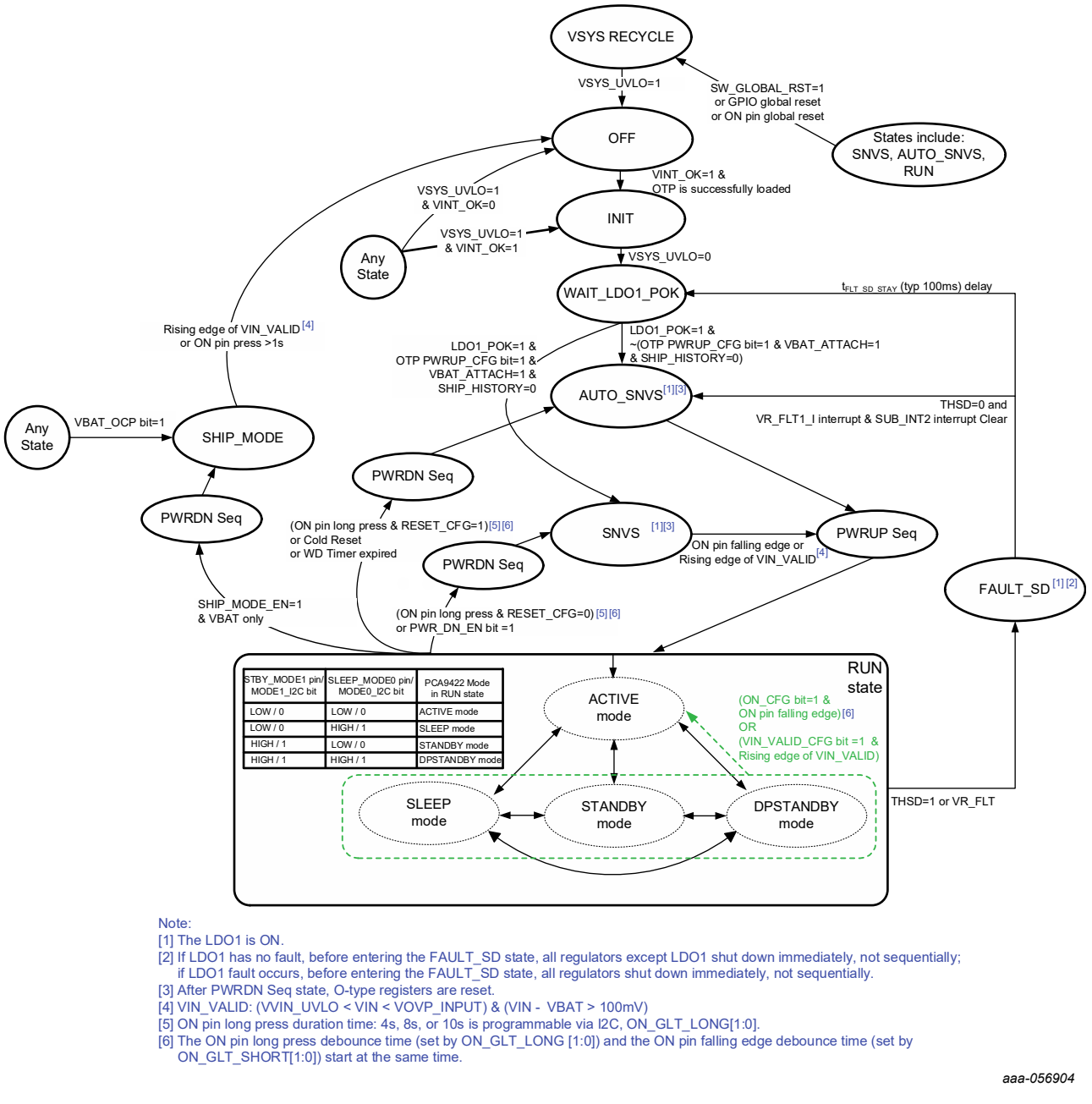
Table 4. Power up sequence

Regulator	PCA9422A	PCA9422B
LDO1	1.8V, always-on	1.8V, always-on
SW1	T6, 1.0 V	T4, 1.0 V
SW2	T5, 1.0 V	T4, 1.1 V
SW3	T1, 1.8 V	T4, 1.0 V
SW4	T7, 5.0 V	T2, 1.8 V
LDO2	T2, 1.8 V	T3, 1.8 V
LDO3	T3, 1.2 V	T3, 1.2 V
LDO4	T4, 3.3 V	T3, 3.3 V

Details of the OTP programming for each device can be found in Table 5.

8 Functional description

8.1 Power states



STBY_MODE1 pin/ MODE1_I2C bit	SLEEP_MODE0 pin/ MODE0_I2C bit	PCA9422 Mode in RUN state
LOW / 0	LOW / 0	ACTIVE mode
LOW / 0	HIGH / 1	SLEEP mode
HIGH / 1	LOW / 0	STANDBY mode
HIGH / 1	HIGH / 1	DPSTANDBY mode

Note:
[1] The LDO1 is ON.
[2] If LDO1 has no fault, before entering the FAULT_SD state, all regulators except LDO1 shut down immediately, not sequentially; if LDO1 fault occurs, before entering the FAULT_SD state, all regulators shut down immediately, not sequentially.
[3] After PWRDN Seq state, O-type registers are reset.
[4] VIN_VALID: (VVIN_UVLO < VIN < VOVP_INPUT) & (VIN - VBAT > 100mV)
[5] ON pin long press duration time: 4s, 8s, or 10s is programmable via I2C, ON_GLT_LONG[1:0].
[6] The ON pin long press debounce time (set by ON_GLT_LONG [1:0]) and the ON pin falling edge debounce time (set by ON_GLT_SHORT[1:0]) start at the same time.

Figure 4. Power state diagram

8.2 Linear battery charger

The battery charger is a linear charger. Its charging is done through a linear switch with the following output protections:

- Reverse current protection
  - (triggers when VIN < VBAT+ V_{CHG_ENABLE})
- Charging current limiting
  - (a function of programmed V_{INPUT_AICL} threshold and battery temperature)
- VBAT overcurrent and overvoltage protection

After Charging Qualification Process is passed, if the battery voltage is below the $V_{VBAT\_PRECHARGE}$ threshold, the battery is considered discharged and a pre-charge cycle begins. The amount of pre-charge current ($I_{VBAT\_PRECHARGE}$) can be programmed through I^2C register setting. This feature is useful when there is a load connected directly across the battery (at VBAT pin) “stealing” the battery current. The pre-charge current can be set higher to account for the system loading while allowing the battery to be properly conditioned. Once the battery voltage has charged to the $V_{VBAT\_PRECHARGE}$ threshold, fast charge is initiated and a programmed fast charge current (I_{FAST_CHG}) is applied. The fast charge constant current is programmed using I^2C register. The constant current provides the bulk of the charge. Power dissipation in the device is greatest in fast charge with a lower battery voltage.

If the device reaches a programmed thermal regulation threshold temperature from 60°C to 100°C in 10°C steps, the device enters thermal regulation. Thermal regulation reduces the charge current by -5.4%/°C to keep the temperature from rising any further when battery charger works in constant current charging mode, or at a reduced regulated voltage when battery charger works in constant voltage charging mode.

Figure 5 shows the charging profile begins with a dead battery condition. Once the cell has charged to the regulation voltage (V_{BAT_REG}) the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold ($I_{TOP\_OFF\_CURRENT}$).

8.2.1 Battery charging management

Battery charging management supports typical constant current / constant voltage charging profile for single cell Li-Ion battery, as well as pre-qualification (dead battery, low battery), top-off mode, etc.; JEITA and thermal regulation compliant.

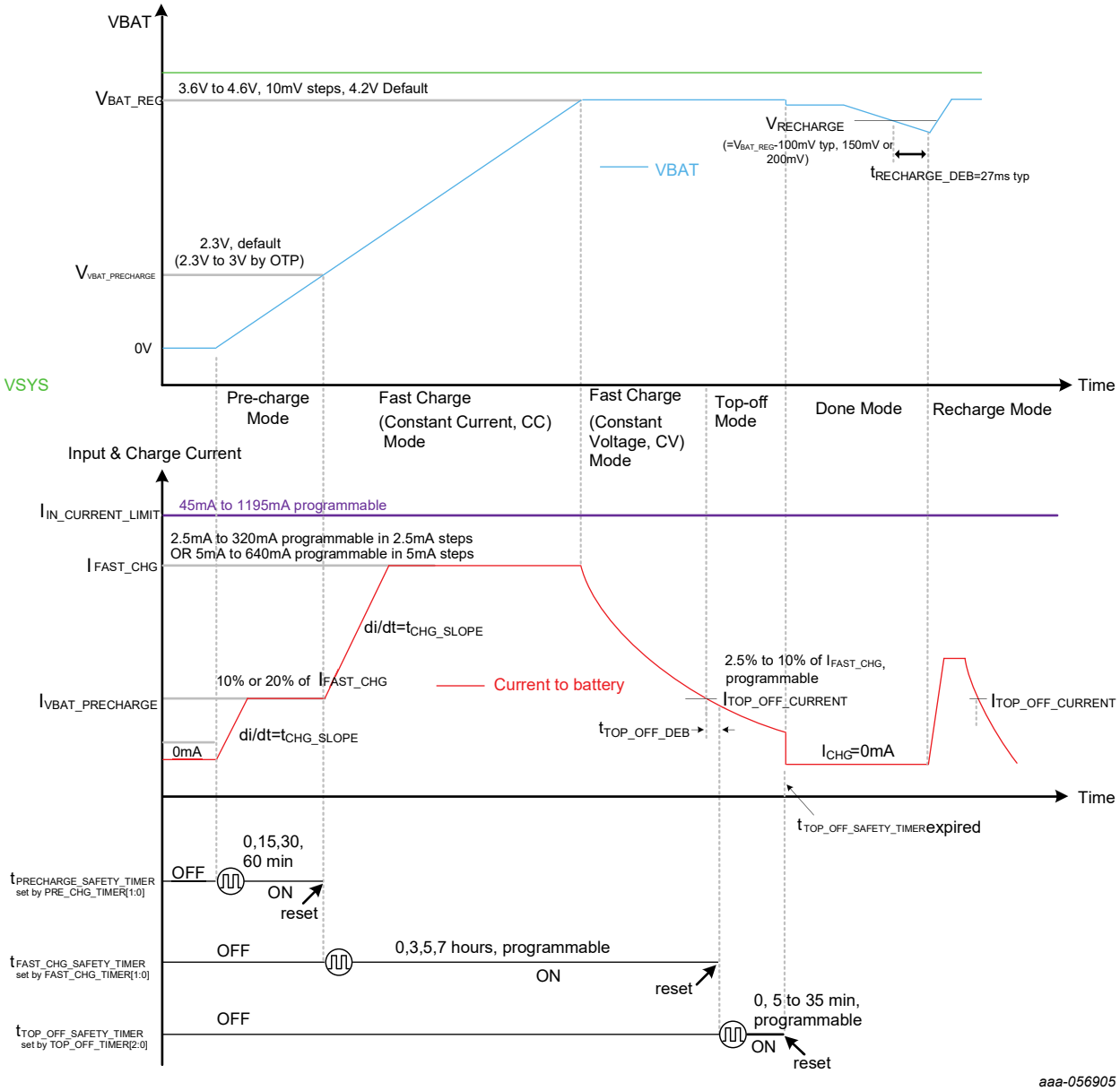


Figure 5. Typical charging profile example

9 PCA9422 OTP version

The PCA9422 can be configured to each regulator default voltage and start-up sequence from the internal OTP configuration. Table 5 shows each OTP configuration for all devices.

Table 5. OTP configuration

Description	Register	PCA9422A	PCA9422B
Power up configuration	OTP_PWRUP_CFG	0b	0b
LDO1 (always-on LDO)	-	1.8 V	1.8 V
BUCK1 output voltage	OTP_B1_DVS0	1.0 V	1.0 V
BUCK1 start up sequence	OTP_PSEQ_BK1	T6	T4
BUCK1 output voltage maximum	OTP_B1_MAX_LIMIT	1.2 V	1.2 V
BUCK2 output voltage	OTP_B2_DVS0	1.0 V	1.1 V
BUCK2 start up sequence	OTP_PSEQ_BK2	T5	T4
BUCK2 output voltage maximum	OTP_B2_MAX_LIMIT	1.2 V	1.4 V
BUCK3 output voltage	OTP_B3_DVS0	1.8 V	1.0 V
BUCK3 start up sequence	OTP_PSEQ_BK3	T1	T4
BUCK3 output voltage maximum	OTP_B3_MAX_LIMIT	1.975 V	1.2 V
BUCK-BOOST output voltage	OTP_BB_VOUT	5.0 V	1.8 V
BUCK-BOOST start up sequence	OTP_PSEQ_BB	T7	T2
BUCK-BOOST output voltage maximum	OTP_BB_MAX_LMT	5.0 V	5.0 V
LDO2 Load Switch mode selection	OTP_LDO2_MODE	LDO	LDO
LDO3 Load Switch mode selection	OTP_LDO3_MODE	LDO	LDO
LDO2 output voltage	OTP_L2_OUT	1.8 V	1.8 V
LDO2 start up sequence	OTP_PSEQ_LDO2	T2	T3
LDO3 output voltage	OTP_L3_OUT	1.2 V	1.2 V
LDO3 start up sequence	OTP_PSEQ_LDO3	T3	T3
LDO4 output voltage	OTP_L4_OUT	3.3 V	3.3 V
LDO4 start up sequence	OTP_PSEQ_LDO4	T4	T3
BUCK1 switching frequency	OTP_CFG2_BK1	4 MHz	4 MHz
BUCK2 switching frequency	OTP_CFG2_BK2	4 MHz	4 MHz
BUCK3 switching frequency	OTP_CFG2_BK3	4 MHz	4 MHz
BUCK1 Active Discharge	OTP_B1_AD	Enabled	Enabled
BUCK2 Active Discharge	OTP_B2_AD	Enabled	Enabled
BUCK3 Active Discharge	OTP_B3_AD	Enabled	Enabled
LDO2 Active Discharge	OTP_L2_AD	Enabled	Enabled
LDO3 Active Discharge	OTP_L3_AD	Enabled	Enabled
LDO4 Active Discharge	OTP_L4_AD	Enabled	Enabled
BUCK1 Forced PWM mode	OTP_B1_FPWM	Auto	Auto

Table 5. OTP configuration*...continued*

Description	Register	PCA9422A	PCA9422B
BUCK2 Forced PWM mode	OTP_B2_FPWM	Auto	Auto
BUCK3 Forced PWM mode	OTP_B3_FPWM	Auto	Auto
BUCK-BOOST Forced PWM mode	OTP_BB_FPWM	Auto	Auto
Time step configuration of power up	OTP_PSQ_TON_STEP	2 ms	2 ms
Time step configuration of power down	OTP_PSQ_TOFF_STEP	8 ms	8 ms
GPIO output setting	OTP_GPIO_CFG	Buffered ON pin signal	Buffered ON pin signal
GPIO pulled up voltage	OTP_GPIO_PULLUP_CFG	LDO1	LDO1
VSYS_UVLO	OTP_VSYS_UVLO_SEL	2.7 V	2.7 V
CHGIN_UVLO	OTP_CHGIN_UVLO	4.0 V	4.0 V
Enable/Disable charger	OTP_CHARGER_EN	Enabled	Enabled
Program input current limit on VIN	OTP_CHGIN_IN_LIMIT	470 mA	470 mA
Program current step on the battery charge current	OTP_CHG_CURRENT_STEP	2.5 mA	2.5 mA
Program VBAT regulation voltage	OTP_VBAT_REG	4.2 V	4.2 V
Program fast charge current	OTP_I_FAST_CHG	100 mA	100 mA
Program pre-charge current	OTP_PRECHG_CURRENT	10% of fast charge current	10% of fast charge current
Battery presence detection	OTP_BAT_PRESENCE_DET_DISABLE	Enabled	Enabled
AUTOSTOP function	OTP_AUTOSTOP_CHG_EN	Enabled	Enabled
Program a threshold for V_{WARM_50C}	OTP_V_WARM_50C	45 °C	45 °C

10 PCB layout

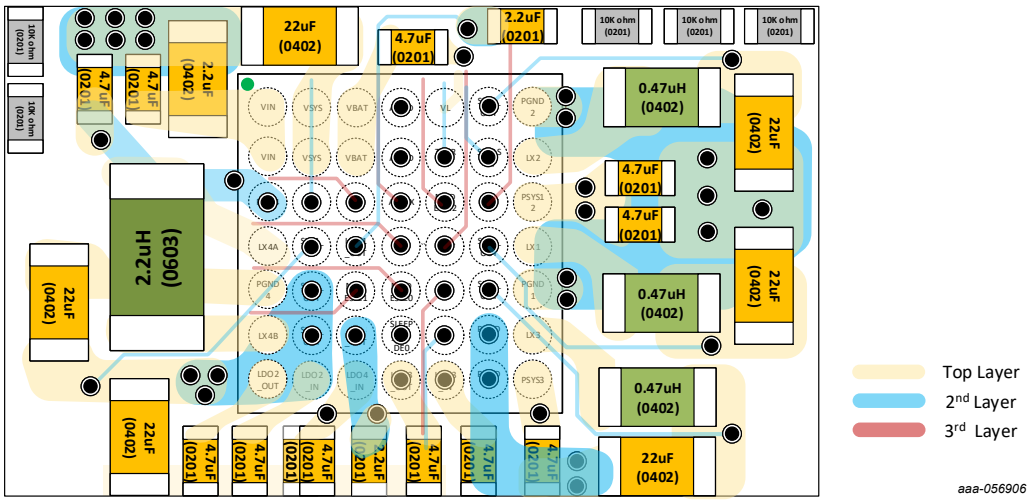


Figure 6. PCA9422 PCB layout Guide

11 Package outline

This PCA9422 uses a 49-pin WLCSP 2.90 mm x 3.00 mm package, case number 98ASA01877D.

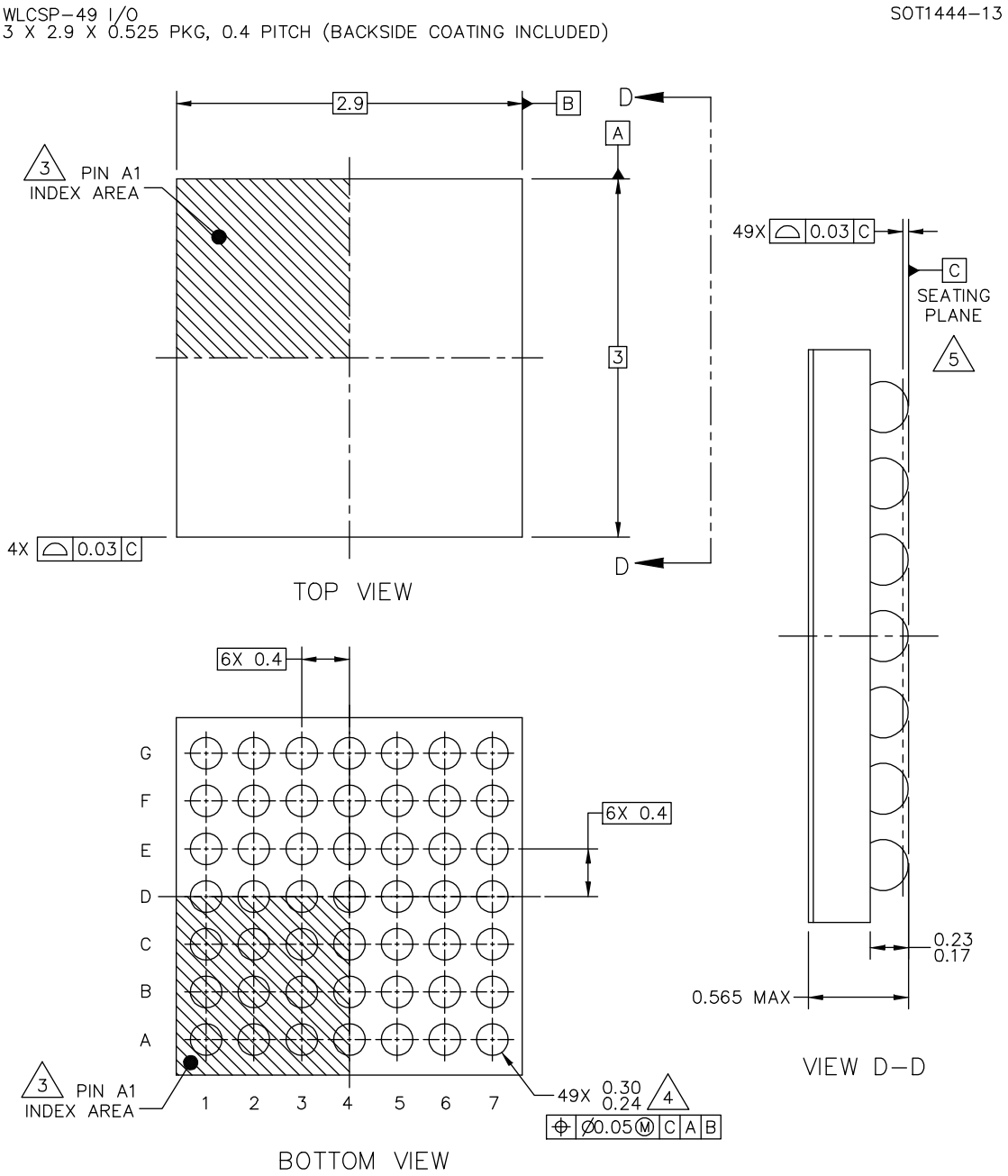


Figure 7. Package outline for WLCSP-49 (SOT1444-13)

12 Soldering

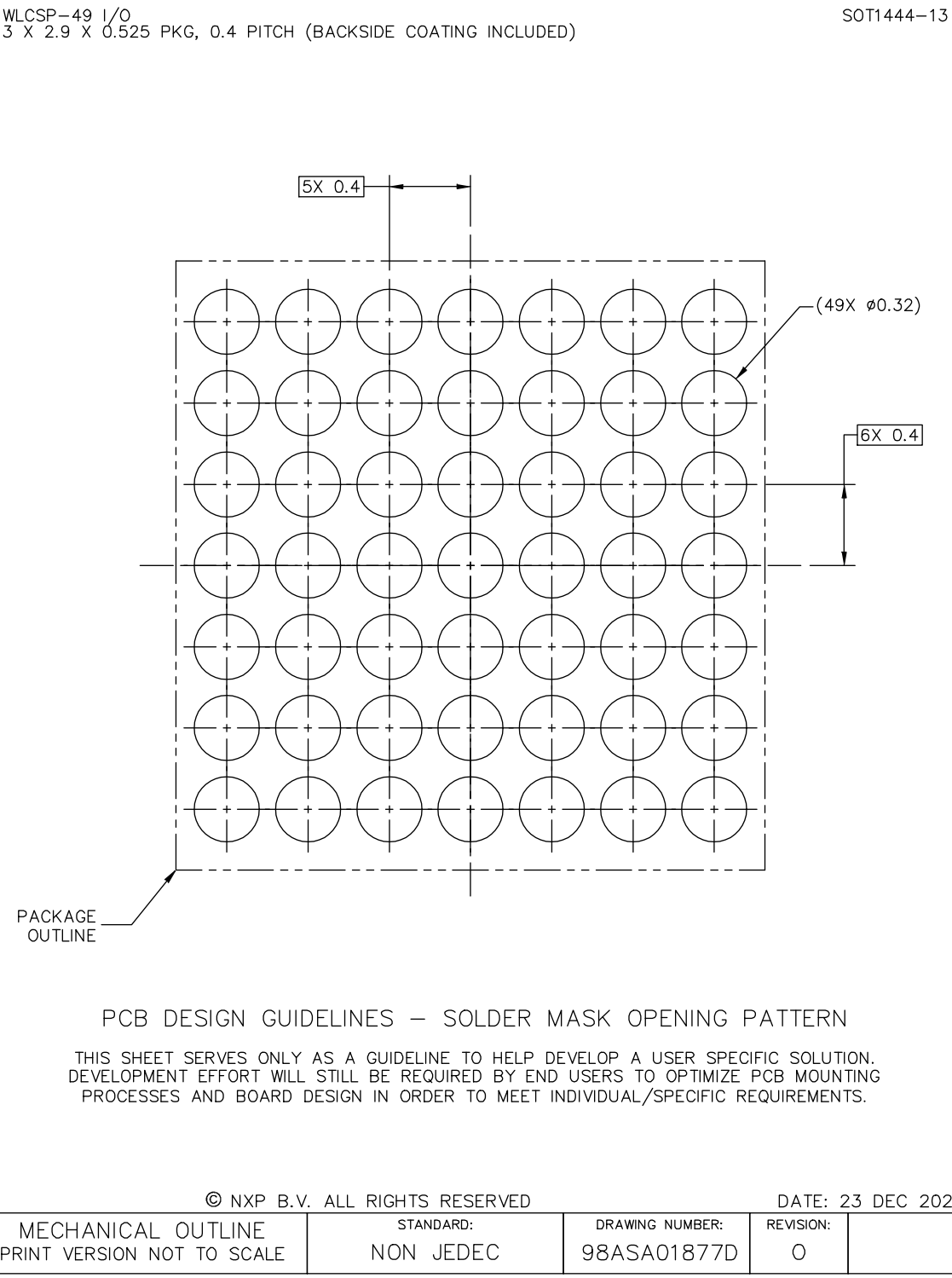


Figure 8. WLCSP-49 (SOT1444-13) solder mask opening pattern

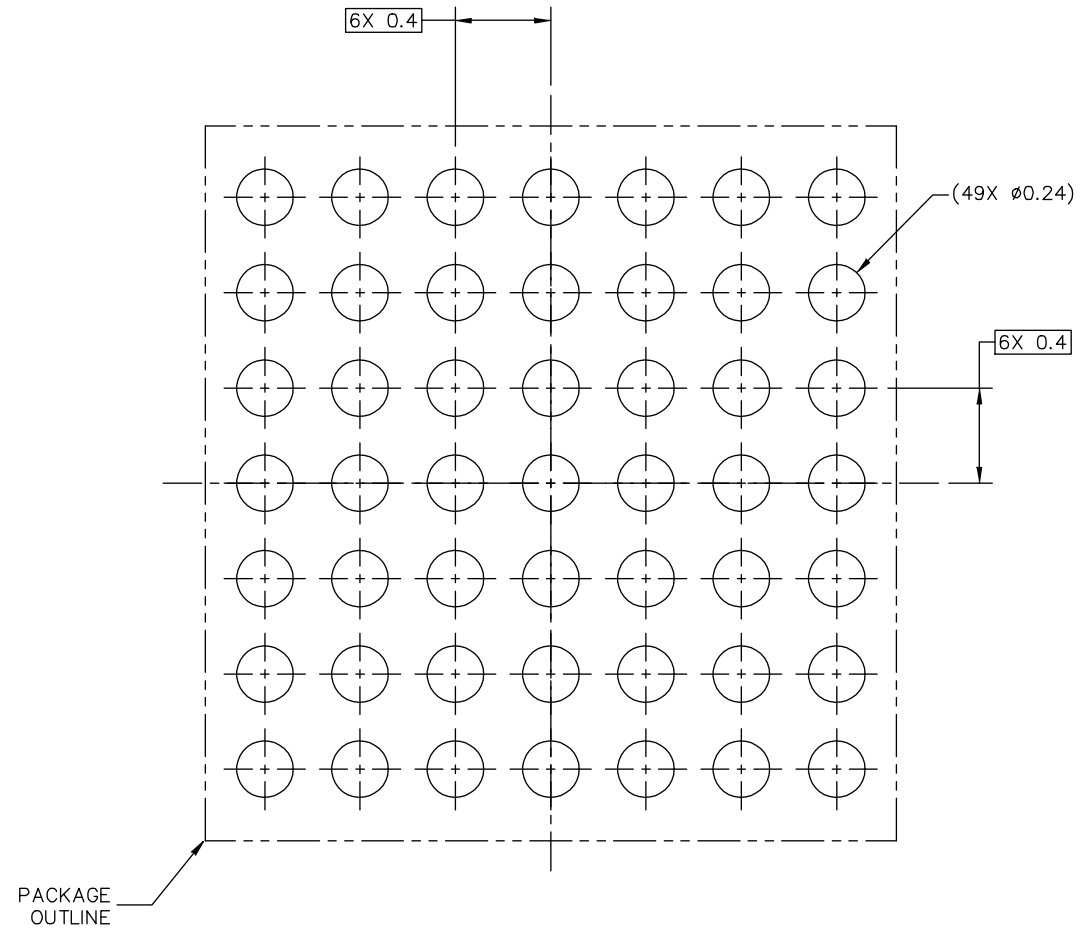


Figure 9. WLCSP-49 (SOT1444-13) I/O pads and solderable area

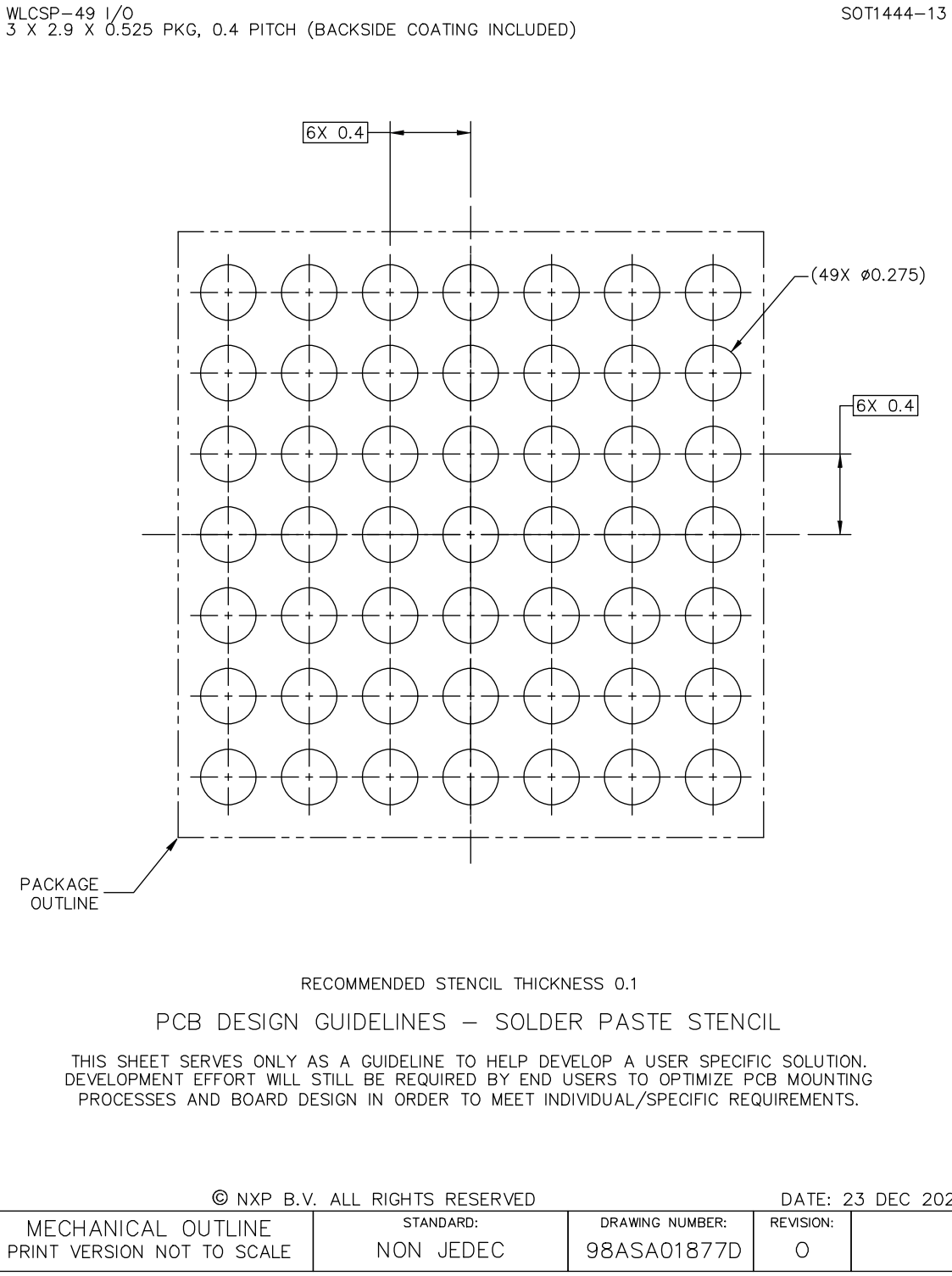


Figure 10. WLCSP-49 (SOT1444-13) solder paste stencil

Figure 11. WLCSP-49 (SOT1444-13) notes

13 Revision history

Table 6. Revision history

Document ID	Release date	Description
PCA9422_SDS v.1.0	14 August 2024	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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