

# P3S0210BQ

Dual bidirectional I3C-bus, 1:2 and 2:1 switch, and voltage level translator

Rev. 1.0 — 15 December 2023

Product data sheet

## 1 General description

The P3S0210BQ is a dual bidirectional I3C-bus 1:2 (one controller to two targets) and 2:1 (two controllers to one target) switch and voltage level translator. It includes a reference supply ( $V_{CCR}$ ), supplies for ports 1, 2, and S ( $V_{CCP1}$ ,  $V_{CCP2}$ , and  $V_{CCS}$  respectively), and a supply for OE and SEL pins ( $V_{CCE}$ ).

The supply voltage of  $V_{CCP1}$ ,  $V_{CCP2}$ ,  $V_{CCS}$ , and  $V_{CCE}$  is between 0.72 V to 3.63 V. The reference supply  $V_{CCR}$  is between 1.62 V to 3.63 V and should be greater or equal to  $V_{CCP1}$ ,  $V_{CCP2}$ ,  $V_{CCS}$  and  $V_{CCE}$ .

Pins A1 and B1 are referenced to  $V_{CCP1}$ , pins A2 and B2 are referenced to  $V_{CCP2}$ , and pins A and B are referenced to  $V_{CCS}$ . The OE and SEL pins are defined for enable and port selection that are referenced to  $V_{CCE}$ .

P3S0210BQ can be used for both open-drain as well as push-pull application which allows for I3C-bus and other applications like I<sup>2</sup>C-bus, SMBus and SPI protocols.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2 Features and benefits

- I3C switch and voltage level translation
  - 2:1; two controllers  $\leftrightarrow$  one target
  - 1:2; one controller  $\leftrightarrow$  two targets
- Wide supply voltage range:
- $V_{CCP1}$ : 0.72 V to 3.63 V (port 1)
- $V_{CCP2}$ : 0.72 V to 3.63 V (port 2)
- $V_{CCS}$ : 0.72 V to 3.63 V (port S)
- $V_{CCE}$ : 0.72 V to 3.63 V (OE and SEL pins)
- $V_{CCR}$ : 1.62 V to 3.63 V (reference)
- $V_{CCP1}$ ,  $V_{CCP2}$ ,  $V_{CCS}$  and  $V_{CCE} \leq V_{CCR}$
- Auto direction sensing, bidirectional voltage level translation
- Support both open-drain and push-pull application
  - I3C, I<sup>2</sup>C and SPI protocols
  - Data rate up to 52 Mbps
- IOFF circuitry provides partial Power-down mode operation
- Provided voltage level translation for I3C, I<sup>2</sup>C-bus, SMBus and SPI devices
- ESD protection:
  - HBM JESD22-A114E Class 2 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78F Class II
- Available in DHVQFN14 package (2.5 mm x 3 mm x 0.85 mm body)
- Specified from and -40 °C to +125 °C



### 3 Applications

- Server and data center
- Networking
- Desktop and laptop computers
- Smart phone and mobile devices

### 4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
P3S0210BQ	S0210	DHVQFN14	plastic, dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 mm x 3 mm x 0.85 mm, 0.5 mm pitch	SOT762-1

#### 4.1 Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
P3S0210BQ	P3S0210BQAZ	DHVQFN14	REEL 7" Q1 NDP SSB	3000	T <sub>amb</sub> = -40 °C to +125 °C

### 5 Block diagram

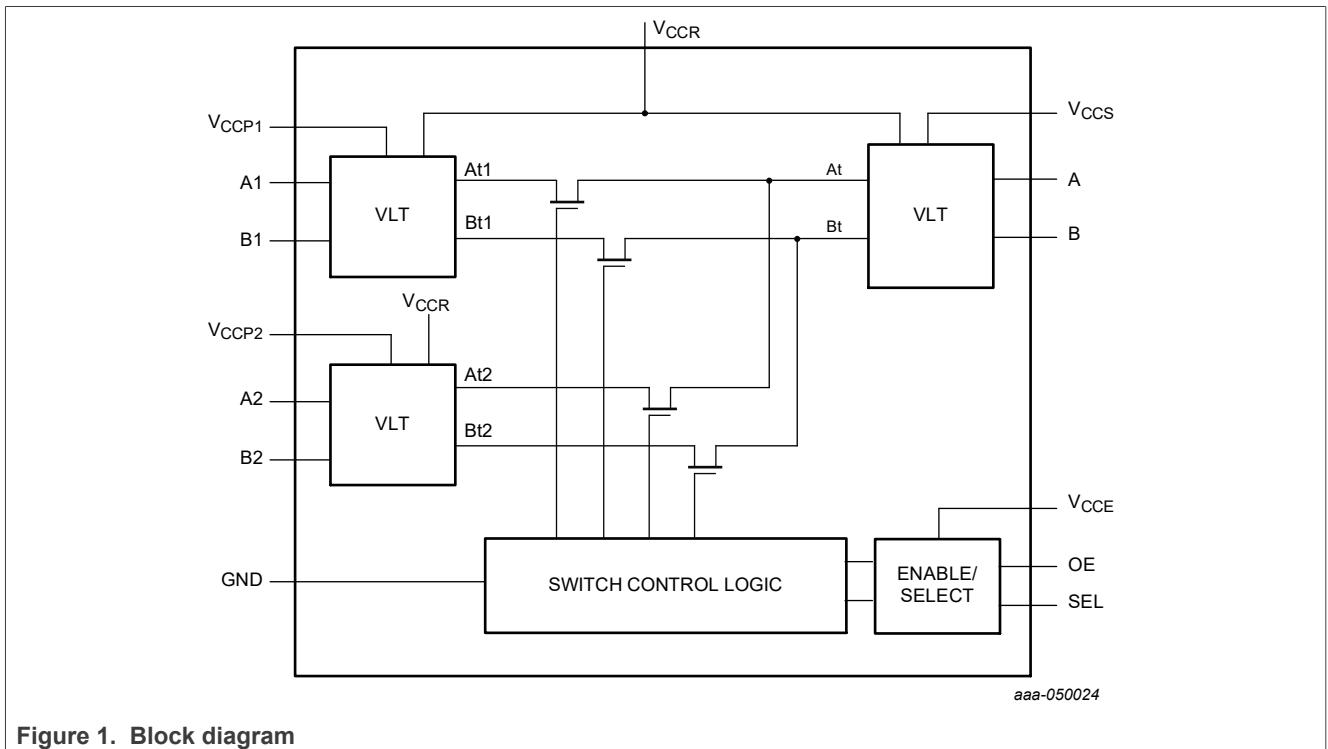


Figure 1. Block diagram

## 6 Pinning information

### 6.1 Pinning

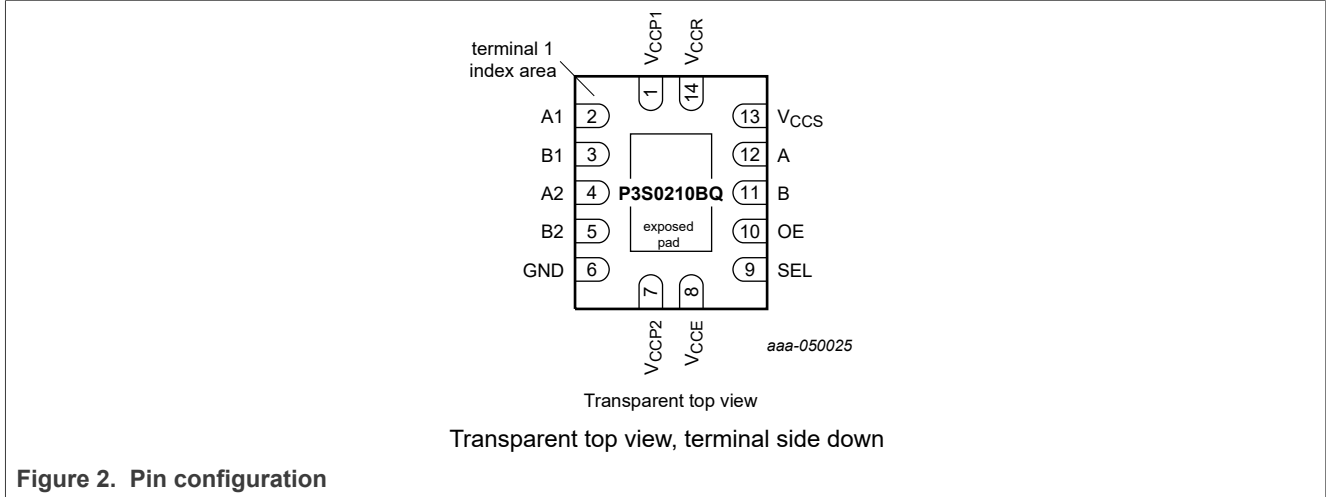


Figure 2. Pin configuration

### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type <sup>[1]</sup>	Description
V <sub>CCP1</sub>	1	S	supply voltage for port 1
A1	2	I/O	input or output of port 1 (referenced to V <sub>CCP1</sub> )
B1	3	I/O	input or output of port 1 (referenced to V <sub>CCP1</sub> )
A2	4	I/O	input or output of port 2 (referenced to V <sub>CCP2</sub> )
B2	5	I/O	input or output of port 2 (referenced to V <sub>CCP2</sub> )
GND	6	S	supply ground
V <sub>CCP2</sub>	7	S	supply voltage for port 2
V <sub>CCE</sub>	8	S	supply voltage for EN & SEL
SEL	9	I	port 1 or 2 selection (referenced to V <sub>CCE</sub> )
OE	10	I	enable pin, active HIGH (referenced to V <sub>CCE</sub> )
B	11	I/O	common input or output of port S (referenced to V <sub>CCS</sub> )
A	12	I/O	common input or output of port S (referenced to V <sub>CCS</sub> )
V <sub>CCS</sub>	13	S	supply voltage for port S
V <sub>CCR</sub>	14	S	reference supply voltage
Exposed pad	-	-	connect to PCB GND

[1] I = input, O = output, I/O = input and output, S = power supply

## 7 Functional description

### 7.1 Architecture

The architecture is DPDT (Double Pole Double Throw) switch with VLT (Voltage Level Translation) to achieve 2:1 or 1:2 I3C-bus switch function. The VLT uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high), N-channel Pass gate transistor and a 10 kΩ pullup resistor (to provide DC-bias and drive capabilities) to meet these requirements. All of the ports (A/A1/A2 and B/B1/B2) have pullup resistors when enabled and the I/O status is HIGH. When I/O status is LOW or is disabled, the pullup resistors are disconnected

The design is directionless and does not need direction control signal. The implementation supports both low-speed Open-drain operation (I<sup>2</sup>C-bus) as well as high speed push-pull operation (I3C-bus or SPI-bus). The N-channel Pass device is on only during LOW input cycle and off during HIGH input cycle.

P3S0210BQ can be enabled/disabled by OE pin when all the power rails (V<sub>CCP1</sub>, V<sub>CCP2</sub>, V<sub>CCS</sub>, V<sub>CCE</sub>, and V<sub>CCR</sub>) are available.

The SEL pin provides the port select function.

- SEL = L, the port 1 is connected to port S. The port 2 is disconnected.
- SEL = H, the port 2 is connected to port S. The port 1 is disconnected.

See [Table 3](#) function table for port status vs V<sub>CCP1</sub>, V<sub>CCP2</sub>, V<sub>CCS</sub>, V<sub>CCR</sub>, OE and SEL.

**Table 3. Function table**<sup>[1]</sup>

H = HIGH voltage level; L = LOW voltage level; X = don't care

Supply voltage			Input		Input/output
<b>V<sub>CCR</sub> = 1.62 V to 3.63 V and V<sub>CCE</sub> = 0.72 to V<sub>CCR</sub></b>					
<b>V<sub>CCP1</sub></b>	<b>V<sub>CCP2</sub></b>	<b>V<sub>CCS</sub></b>	<b>OE</b> <sup>[2]</sup>	<b>SEL</b> <sup>[2]</sup>	
0.72 to V <sub>CCR</sub>	0.72 to V <sub>CCR</sub>	0.72 to V <sub>CCR</sub>	L	X	disconnected
0.72 to V <sub>CCR</sub>	0.72 to V <sub>CCR</sub>	0.72 to V <sub>CCR</sub>	H	L	port 1 = port S <sup>[3]</sup> A1 = A B1 = B
0.72 to V <sub>CCR</sub>	0.72 to V <sub>CCR</sub>	0.72 to V <sub>CCR</sub>	H	H	port 2 = port S <sup>[3]</sup> A2 = A B2 = B
GND	X	X	X	X	disconnected
X	GND	X	X	X	disconnected
X	X	GND	X	X	disconnected
<b>V<sub>CCR</sub> = GND or V<sub>CCE</sub> = GND</b> <sup>[4]</sup>					
<b>V<sub>CCP1</sub></b>	<b>V<sub>CCP2</sub></b>	<b>V<sub>CCS</sub></b>	<b>OE</b>	<b>SEL</b>	
X	X	X	X	X	disconnected

[1] At disconnected condition, port 1, port 2 and port S. (i.e. A1/A2/A & B1/B2/B pins) are high-Z.

[2] V<sub>IL</sub> max = 0.35V<sub>CCE</sub> and V<sub>IH</sub> min = 0.65 V<sub>CCE</sub>. The V<sub>CCE</sub> can be connected to an external device that is powered by either V<sub>CCP1</sub>, V<sub>CCP2</sub>, V<sub>CCS</sub> or V<sub>CCR</sub>.

[3] At this condition, there are internal 10 kΩ pullup resistors for port 1, port 2 and port S. (i.e. A1/A2/A & B1/B2/B pins)

[4] When V<sub>CCR</sub> is at GND level, the device goes into Power-down mode.

## 7.2 Input driver requirements

The continuous DC- current sinking or sourcing capability is determined by the external system-level; open-drain or push-pull drivers that are interfaced to the P3S0210BQ IO pins.

The high bandwidth of these IO circuits used to facilitate this fast change from an input to an output and an output to an input, they have a modest sourcing capability of hundreds of micro-amperes, as determined by the pullup resistor.

The fall time of a signal depends on the edge-rate and output impedance of the external driving the P3S0210BQ data IOs, as well as the capacitive loading at the data lines.

## 7.3 Power-up/power-down and enable/disable

It requires all the power rails ready and OE pin ready to power up P3S0210BQ.

If any power rail or OE are not ready, this part is disabled, and all the ports are disconnected. There is no special power sequence requirement between  $V_{CCP1}$ ,  $V_{CCP2}$ ,  $V_{CCS}$ ,  $V_{CCR}$ ,  $V_{CCE}$ , and OE pin. After power up,  $V_{CCR}$  should be greater or equal to the maximum value of  $V_{CCP1}$ ,  $V_{CCP2}$ ,  $V_{CCS}$ ,  $V_{CCE}$ , and 1.62 V.

Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time ( $t_{dis}$  with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND, OE pin should not be left floating in any condition.

OE ( $V_{IL(max)} = 0.35V_{CCE}$  and  $V_{IH(min)} = 0.65V_{CCE}$ ) allows the control signal by the device  $V_{cc}$  range from 0.72 V to  $V_{CCR}$ .

## 7.4 Pullup or pulldown resistors on I/O lines

Each I/O pin of port 1, port 2 and port S has an internal 10 kΩ pullup resistor to  $V_{CCP1}$ ,  $V_{CCP2}$  and  $V_{CCS}$ , respectively.

The pullup resistors are connected only when P3S0210BQ is enabled and the I/O status is HIGH. When I/O status is low or P3S0210BQ is disabled, the pullup resistors are disconnected.

When SEL is set LOW, A2 and B2 are pulled up HIGH ( $V_{CCP2}$ ) due to internal 10 kΩ pullup resistance. When SEL is set HIGH under  $V_{CCE}$  domain, A1 and B1 are tied to  $V_{CCP1}$  by internal pullup resistance.

If a smaller pullup resistor is required, add an external resistor in parallel to the internal 10 kΩ. The smaller value affects the  $V_{OL}$  level.

If an external pulldown resistor is required, the  $V_{OH}$  level is decreased by the voltage divider from the internal 10 kΩ pullup R and the external pulldown R. The pulldown resistor value is recommended to be greater than 200 kΩ. It ensures  $V_{OH}$  level drops less than 5 % of the associated supply voltage.

## 8 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCR}$	reference supply voltage		-0.5	+4.2	V
$V_{CCP1}$	supply voltage for port 1		-0.5	+4.2	V
$V_{CCP2}$	supply voltage for port 2		-0.5	+4.2	V

## Dual bidirectional I3C-bus, 1:2 and 2:1 switch, and voltage level translator

Table 4. Limiting values...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCS</sub>	supply voltage for port S		-0.5	+4.2	V
V <sub>CCE</sub>	supply voltage for OE and SEL		-0.5	+4.2	V
V <sub>I</sub>	input voltage	at I/O pins supplied by V <sub>CCP1</sub> <sup>[1]</sup>	-0.5	+4.2	V
		at I/O pins supplied by V <sub>CCP2</sub> <sup>[1] [2] [3]</sup>	-0.5	+4.2	V
		at I/O pins supplied by V <sub>CCS</sub> <sup>[1]</sup>	-0.5	+4.2	V
		OE, SEL	-0.5	+4.2	V
V <sub>O</sub>	output voltage	Active mode	-0.5	V <sub>CCO</sub> +0.25	V
		Power-down <sup>[4]</sup>	-0.5	+4.2	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	-	125	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V<sub>CCO</sub> is the supply voltage associated with the output.[3] V<sub>CCO</sub> + 0.25 V should not exceed 4.2 V.[4] V<sub>CCR</sub> = GND or V<sub>CCE</sub> = GND

## 9 Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCR</sub>	supply voltage	at V <sub>CCR</sub> supply pin	1.62	3.63	V
V <sub>CCP1</sub>		at V <sub>CCP1</sub> supply pin	0.72	V <sub>CCR</sub>	V
V <sub>CCP2</sub>		at V <sub>CCP2</sub> supply pin	0.72	V <sub>CCR</sub>	V
V <sub>CCS</sub>		at V <sub>CCS</sub> supply pin	0.72	V <sub>CCR</sub>	V
V <sub>CCE</sub>		at V <sub>CCE</sub> supply pin	0.72	V <sub>CCR</sub>	V
V <sub>I</sub>	input voltage	at I/O pins supplied by V <sub>CCP1</sub>	-0.3	V <sub>CCP1</sub>	V
		at I/O pins supplied by V <sub>CCP2</sub>	-0.3	V <sub>CCP2</sub>	V
		at I/O pins supplied by V <sub>CCS</sub>	-0.3	V <sub>CCS</sub>	V
		OE, SEL	-0.3	V <sub>CCE</sub>	V
V <sub>O</sub>	output voltage	at I/O pins supplied by V <sub>CCP1</sub>	-0.3	V <sub>CCP1</sub>	V
		at I/O pins supplied by V <sub>CCP2</sub>	-0.3	V <sub>CCP2</sub>	V
		at I/O pins supplied by V <sub>CCS</sub>	-0.3	V <sub>CCS</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
T <sub>j</sub>	junction temperature <sup>[1]</sup>		-40	+150	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CCO</sub> = 0.72 V to V <sub>CCR</sub>	-	<5.3	ns/V

[1] The T<sub>j</sub> limits shall be supported by proper thermal PCB design.

10 Static characteristics

Table 6. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>OH</sub>	HIGH-level output voltage	port 1, 2 and S; I <sub>O</sub> = -10 μA	0.8xV <sub>CCO</sub>	-	-	V
V <sub>OL</sub>	LOW-level output voltage	port 1, 2 and S; I <sub>O</sub> = 10 μA; V <sub>I</sub> = 0.1 V	-	-	0.25xV <sub>CCO</sub>	V
I <sub>i</sub>	input leakage current	OE input; V <sub>I</sub> = 0 V or 1.98 V; V <sub>CCI</sub> = 0.72 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	-	-	±1	μA
I <sub>OZ</sub>	OFF-state output current	OE = 0; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CCO</sub> = 0.72 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	-	-	±1	μA
I <sub>OFF</sub>	power-off leakage current	port 1, 2; V <sub>I</sub> or V <sub>O</sub> = 0 V or V <sub>CCR</sub> ; V <sub>CCP1</sub> = 0 V; V <sub>CCP2</sub> = 0 V; V <sub>CCS</sub> = 0 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	-	-	±1	μA
		port S; V <sub>I</sub> or V <sub>O</sub> = 0 V or 1.98V; V <sub>CCS</sub> = 0 V; V <sub>CCP1</sub> = 0 V to V <sub>CCR</sub> ; V <sub>CCP2</sub> = 0 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	-	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A; I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CCS</sub> , I <sub>CCR</sub> ; V <sub>CCO</sub> = 0.72 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	-	5	-	μA
C <sub>I</sub>	input capacitance	OE, SEL input; V <sub>CCO</sub> = 0.72 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	-	1.5	-	pF
C <sub>I/O</sub>	input/output capacitance	I/O of port 1, 2 and S; V <sub>CCO</sub> = 0.72 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	-	4.0	-	pF

[1] The typical value is V<sub>CCI</sub> = 1.0 V, V<sub>CCO</sub> = 1.8 V, V<sub>CCR</sub> = 1.8 V or 3.3 V

[2] V<sub>CCO</sub> is the supply voltage associated with the output.

[3] The resistance between input and output at low stage. R<sub>on</sub> max = 370 Ω at min (V<sub>CCI</sub>, V<sub>CCO</sub>) < 0.9 V. R<sub>on</sub> max = 220 Ω at min (V<sub>CCI</sub>, V<sub>CCO</sub>) ≥ 0.9 V.

[4] V<sub>CCI</sub> is the supply voltage associated with the input.

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = -40\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	HIGH-level input voltage	port 1,2 and S; V <sub>CCI</sub> = 0.72 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	0.65 x V <sub>CCI</sub>	-	-	V
		OE, SEL input	0.65 x V <sub>CCE</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	port 1,2 and S; V <sub>CCI</sub> = 0.72 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	-	-	0.35 V <sub>CCX</sub>	V
		OE, SEL input	-	-	0.35 V <sub>CCE</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub> = -10 μA; V <sub>CCO</sub> = 0.72 V to V <sub>CCR</sub> ; V <sub>CCR</sub> = 1.62 V to 3.63 V	0.75 x V <sub>CCO</sub>	-	-	V

Dual bidirectional I3C-bus, 1:2 and 2:1 switch, and voltage level translator

Table 7. Static characteristics...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{OL}$	LOW-level output voltage	$V_I = 0\text{ V}$ ; $I_O = 10\text{ }\mu\text{A}$ ; $V_{CCO} = 0.72\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$	[3] [4]	-	-	$0.25 \times V_{CCO}$	V
$I_I$	input leakage current	OE, SEL input; $V_I = 0\text{ V}$ to $V_{CCI}$ ; $V_{CCO} = 0.72\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$		-	-	$\pm 5$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	port 1,2 and S; $V_O = 0\text{ V}$ or $V_{CCO}$ ; $V_{CCO} = 0.72\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$	[3]	-	-	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	port 1,2; $V_I$ or $V_O = 0\text{ V}$ or $V_{CCR}$ ; $V_{CCP1} = 0\text{ V}$ ; $V_{CCP2} = 0\text{ V}$ ; $V_{CCS} = 0\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$		-	-	10	$\mu\text{A}$
		port S; $V_I$ or $V_O = 0\text{ V}$ or $1.98\text{ V}$ ; $V_{CCS} = 0\text{ V}$ ; $V_{CCP1} = 0\text{ V}$ to $V_{CCR}$ ; $V_{CCP2} = 0\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$		-	-	10	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 0\text{ V}$ or $V_{CCI}$ ; $I_O = 0\text{ A}$	[1]	-	-		
		$I_{CC1}$ , $I_{CC2}$		-	-		
		OE = LOW; $V_{CCO} = 0.72\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$		-	-	15	$\mu\text{A}$
		OE = HIGH; $V_{CCO} = 0.72\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$		-	-	20	$\mu\text{A}$
		$V_{CCP1} = V_{CCP2} = 1.98\text{ V}$ ; $V_{CCS} = 0\text{ V}$		-	-	15	$\mu\text{A}$
		$V_{CCP1} = V_{CCP2} = 0\text{ V}$ ; $V_{CCS} = 1.98\text{ V}$		-	-	-15	$\mu\text{A}$
		$I_{CCS}$		-	-		
		OE = LOW; $V_{CCO} = 0.72\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$		-	-	29	$\mu\text{A}$
		OE = HIGH; $V_{CCO} = 0.72\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$		-	-	36	$\mu\text{A}$
		$V_{CCP1} = V_{CCP2} = 1.98\text{ V}$ ; $V_{CCS} = 0\text{ V}$		-	-	-15	$\mu\text{A}$
		$V_{CCP1} = V_{CCP2} = 0\text{ V}$ ; $V_{CCS} = 1.98\text{ V}$		-	-	20	$\mu\text{A}$
		$I_{CC1} + I_{CC2} + I_{CCS}$		-	-		
OE = LOW; $V_{CCO} = 0.72\text{ V}$ to $V_{CCR}$ ; $V_{CCR} = 1.62\text{ V}$ to $3.63\text{ V}$		-	-	56	$\mu\text{A}$		

[1]  $V_{CCI}$  is the supply voltage associated with the input.

[2]  $V_{CCX}$  is the minimum of  $V_{CCP1}$  and  $V_{CCS}$ , where  $V_{CCP1}$  is the selected port of  $V_{CCP1}$  and  $V_{CCP2}$ .

[3]  $V_{CCO}$  is the supply voltage associated with the output.

[4] The resistance between input and output at low stage.  $R_{on\ max} = 370\ \Omega$  at  $\min(V_{CCI}, V_{CCO}) < 0.9\text{ V}$ .  $R_{on\ max} = 220\ \Omega$  at  $\min(V_{CCI}, V_{CCO}) \geq 0.9\text{ V}$ .



## 11 Dynamic characteristics

Table 8. Dynamic characteristics for temperature range -40 °C to +125 °C<sup>[1]</sup>

$V_{CCR} = 1.62\text{ V to }3.63\text{ V}$ , voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 5](#); for waveform see [Figure 3](#)

Symbol	Parameter	Conditions	$V_{CCS}$			$V_{CCS}$			Unit
			1 V, 1.2 V ± 10 %			1.8 V ± 10 %			
			Min	Typ	Max	Min	Typ	Max	
<b><math>V_{CCP1} = V_{CCP2} = 1\text{ V} \pm 10\%</math></b>									
$t_{pd}^{[1]}$	propagation delay	port1,2 to port S; $C_L = 68\text{ pF}$	-	5.5	8	-	5.5	8	ns
		port S to port1,2; $C_L = 68\text{ pF}$	-	6	9	-	4	6	ns
$t_{en}^{[2]}$	enable time	OE to port1,2 and S; $C_L = 68\text{ pF}$	-	1.4	1.8	-	1.4	1.8	µs
$t_{dis}^{[2]}$	disable time	OE to port1,2; no external $C_L$ <sup>[3]</sup>	-	190	220	-	180	210	ns
		OE to port S; no external $C_L$ <sup>[3]</sup>	-	190	220	-	180	210	ns
		OE to port1,2; $C_L = 68\text{ pF}$	-	460	600	-	450	540	ns
		OE to port S; $C_L = 68\text{ pF}$	-	460	600	-	450	540	ns
$t_{sel\_en}$	SEL enable time	OE = HIGH, $V_I = L$ or H SEL: H→L ( or L→H) Port 1 (or port 2) connect to port S, $C_L = 68\text{ pF}$	-	1.5	1.9	-	1.5	1.9	µs
$t_{sel\_dis}$	SEL disable time	OE = HIGH, $V_I = L$ or H SEL: L→H (or H→L) Port 1 (or port 2) disconnect to port S, $C_L = 68\text{ pF}$	-	140	210	-	130	200	ns
$t_t$	transition time	port1,2 ; $C_L = 68\text{ pF}$	1.1	4	6.5	0.7	3	5	ns
		port S; $C_L = 68\text{ pF}$	1.1	4	7	0.7	2.5	4	ns
$t_{sk(o)}$	output skew time	delta between channels <sup>[4]</sup>	0	0.2	0.4	0	0.2	0.4	ns
$t_W$	pulse width	data inputs	15	-	-	13.5	-	-	ns
$f_{data}$	data rate		0.064	-	52	0.064	-	52	Mbps

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[2] Guaranteed by design.

[3] Delay between OE going LOW and when the outputs are actually disabled ( $R_L = 50\text{ k}\Omega$  and no  $C_L$ ).

[4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C<sup>[1]</sup>

$V_{CCR} = 1.62\text{ V to }3.63\text{ V}$ , Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 5; for waveform see Figure 3

Symbol	Parameter	Conditions	$V_{CCS}$			$V_{CCS}$			Unit
			1.2 V ± 10 %			1.62 V to $V_{CCR}$			
			Min	Typ	Max	Min	Typ	Max	
<b><math>V_{CCP1} = 0.9\text{ V to }V_{CCR}</math>; <math>V_{CCP2} = 0.9\text{ V to }V_{CCR}</math></b>									
$t_{pd}$	propagation delay	port1,2 to port S; $C_L = 68\text{ pF}$	-	5.5	8	-	5.5	8	ns
		port S to port1,2; $C_L = 68\text{ pF}$	-	5.5	6.9	-	5.5	6	ns
		port1,2 to port S; $C_L = 80\text{ pF}$	-	7.5	10	-	5.4	7	ns
		port S to port1,2; $C_L = 30\text{ pF}$	-	5	9	-	4	6	ns
$t_{en}^{[2]}$	enable time	OE to port1,2 and S; $C_L = 15\text{ pF}$	-	1.4	1.8	-	1.4	1.8	µs
$t_{dis}^{[2]}$	disable time	OE to port1,2; no external $C_L^{[3]}$	-	180	210	-	180	210	ns
		OE to port S; no external $C_L^{[3]}$	-	180	210	-	180	210	ns
		OE to port1,2; $C_L = 68\text{ pF}$	-	450	580	-	450	540	ns
		OE to port S; $C_L = 68\text{ pF}$	-	450	580	-	450	540	ns
$t_{sel\_en}$	SEL enable time	OE = HIGH, $V_I = L$ or H SEL: H→L (or L→H) Port 1 (or port 2) connect to port S, $C_L = 68\text{ pF}$	-	1.5	1.9	-	1.5	1.9	µs
$t_{sel\_dis}$	SEL disable time	OE = HIGH, $V_I = L$ or H SEL: L→H (or H→L) Port 1 (or port 2) disconnect to port S, $C_L = 68\text{ pF}$	-	140	210	-	130	200	ns
$t_t$	transition time	port1,2; $C_L = 68\text{ pF}$	0.8	1.8	5	0.6	3	5	ns
		port S; $C_L = 68\text{ pF}$	1.1	4	7	0.6	2.5	4	ns
$t_{tc}$	transition time	port1,2; $C_L = 30\text{ pF}$	-	3.5	7	-	2	3	ns
		port S; $C_L = 80\text{ pF}$	-	5	10	-	4	5	ns
$t_{sk(o)}$	output skew time	delta between channels <sup>[4]</sup>	0	0.1	0.5	0	0.3	0.4	ns
$t_W$	pulse width	data inputs	15	-	-	13.5	-	-	ns
$f_{data}$	data rate		0.064	-	52	0.064	-	52	Mbps

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[2] Guaranteed by design.

[3] Delay between OE going LOW and when the outputs are actually disabled ( $R_L = 50\text{ k}\Omega$  and no  $C_L$ ).

[4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Dual bidirectional I3C-bus, 1:2 and 2:1 switch, and voltage level translator

Table 10. Dynamic characteristics for temperature range -40 °C to +125 °C<sup>[1]</sup>

V<sub>CCR</sub> = 1.62 V to 3.63 V, Voltages are referenced to GND (ground = 0 V); for test circuit see

Figure 5; for waveform see Figure 3

Symbol	Parameter	Conditions	V <sub>CCS</sub>			Unit
			1.8 V ± 10 %			
<b>V<sub>CCP1</sub> = V<sub>CCP2</sub> = 1.8 V ± 10 %</b>						
t <sub>pd</sub>	propagation delay	port1,2 to port S; C <sub>L</sub> = 68 pF	-	4	6	ns
		port S to port1,2; C <sub>L</sub> = 68 pF	-	4	6	ns
t <sub>en</sub> <sup>[2]</sup>	enable time	OE to port1,2 and S; C <sub>L</sub> = 68 pF	-	1.4	1.8	µs
t <sub>dis</sub> <sup>[2]</sup>	disable time	OE to port1,2; no external C <sub>L</sub> <sup>[3]</sup>	-	180	210	ns
		OE to port S; no external C <sub>L</sub> <sup>[3]</sup>	-	180	210	ns
		OE to port1,2; C <sub>L</sub> = 68 pF	-	440	540	ns
		OE to port S; C <sub>L</sub> = 68 pF	-	440	540	ns
t <sub>sel_en</sub>	SEL enable time	OE = HIGH, V <sub>I</sub> = L or H SEL: H→L (or L→H) Port 1 (or port 2) connect to port S, C <sub>L</sub> = 68 pF	-	1.5	1.9	µs
t <sub>sel_dis</sub>	SEL disable time	OE = HIGH, V <sub>I</sub> = L or H SEL: L→H (or H→L) Port 1 (or port 2) disconnect to port S, C <sub>L</sub> = 68 pF	-	130	200	ns
t <sub>t</sub>	transition time	port1,2; C <sub>L</sub> = 68 pF	0.5	1.5	2	ns
		port S; C <sub>L</sub> = 68 pF	0.7	2.5	4	ns
t <sub>sk(o)</sub>	output skew time	delta between channels <sup>[4]</sup>	0	0.2	0.3	ns
t <sub>w</sub>	pulse width	data inputs	13.5	-	-	ns
f <sub>data</sub>	data rate		0.064	-	52	Mbps

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PHZ</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

[2] Guaranteed by design.

[3] Delay between OE going LOW and when the outputs are actually disabled (R<sub>L</sub> = 50 kΩ and no C<sub>L</sub>).

[4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C<sup>[1]</sup>

V<sub>CCR</sub> = 1.62 V to 3.63 V, Voltages are referenced to GND (ground = 0 V); for test circuit see

Figure 5; for waveform see Figure 3

Symbol	Parameter	Conditions	V <sub>CCS</sub>			V <sub>CCS</sub>			Unit
			0.72 V to 0.9V			0.9 V to V <sub>CCR</sub>			
			Min	Typ	Max	Min	Typ	Max	
<b>V<sub>CCP1</sub> = 0.72 V to 0.9 V; V<sub>CCP2</sub> = 0.72 V to 0.9 V</b>									
t <sub>pd</sub>	propagation delay	port1,2 to port S; C <sub>L</sub> = 68 pF	-	7	13	-	7.5	8.5	ns

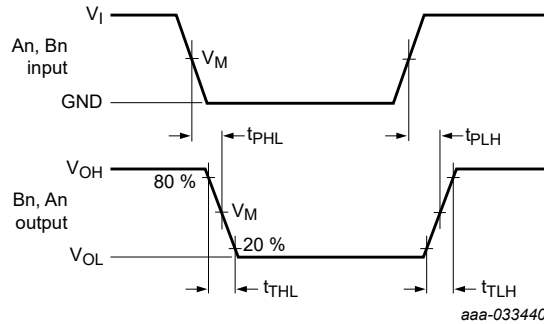
Dual bidirectional I3C-bus, 1:2 and 2:1 switch, and voltage level translator

**Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C<sup>[1]</sup>...continued**  
 $V_{CCR} = 1.62\text{ V to }3.63\text{ V}$ , Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 5](#); for waveform see [Figure 3](#)

Symbol	Parameter	Conditions	V <sub>CCS</sub>			V <sub>CCS</sub>			Unit
			0.72 V to 0.9V			0.9 V to V <sub>CCR</sub>			
			Min	Typ	Max	Min	Typ	Max	
		port S to port1,2; C <sub>L</sub> = 68 pF	-	8	14	-	8	9	ns
t <sub>en</sub> <sup>[2]</sup>	enable time	OE to port1,2 and S; C <sub>L</sub> = 15 pF	-	1.4	12	-	1.4	1.8	µs
t <sub>dis</sub> <sup>[2]</sup>	disable time	OE to port1,2; no external C <sub>L</sub> <sup>[3]</sup>	-	240	270	-	230	260	ns
		OE to port S; no external C <sub>L</sub> <sup>[3]</sup>	-	240	270	-	230	260	ns
		OE to port1,2; C <sub>L</sub> = 68 pF	-	490	650	-	470	620	ns
		OE to port S; C <sub>L</sub> = 68 pF	-	490	650	-	470	620	ns
t <sub>sel_en</sub>	SEL enable time	OE = HIGH, V <sub>I</sub> = L or H SEL: H→L (or L→H) Port 1 (or port 2) connect to port S, C <sub>L</sub> = 68 pF	-	1.5	1.9	-	1.5	1.9	µs
t <sub>sel_dis</sub>	SEL disable time	OE = HIGH, V <sub>I</sub> = L or H SEL: L→H (or H→L) Port 1 (or port 2) disconnect to port S, C <sub>L</sub> = 68 pF	-	150	220	-	140	210	ns
t <sub>t</sub>	transition time	port1,2 ; C <sub>L</sub> = 68 pF	-	3	16	0.75	2.5	9	ns
		port S; C <sub>L</sub> = 68 pF	-	6.5	16	0.8	6.5	9	ns
t <sub>sk(o)</sub>	output skew time	delta between channels <sup>[4]</sup>	0	0.2	0.3	0	0.2	0.7	ns
t <sub>W</sub>	pulse width	data inputs	37	-	-	17	-	-	ns
f <sub>data</sub>	data rate		0.064	-	26	0.064	-	40	Mbps

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.  
 [2] Guaranteed by design.  
 [3] Delay between OE going LOW and when the outputs are actually disabled (R<sub>L</sub> = 50 kΩ and no C<sub>L</sub>).  
 [4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

12 Waveforms



Measurement points are given in [Table 12](#)

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Figure 3. Data input (port 1/2, port S) to data output (port S, port 1/2) propagation delay times

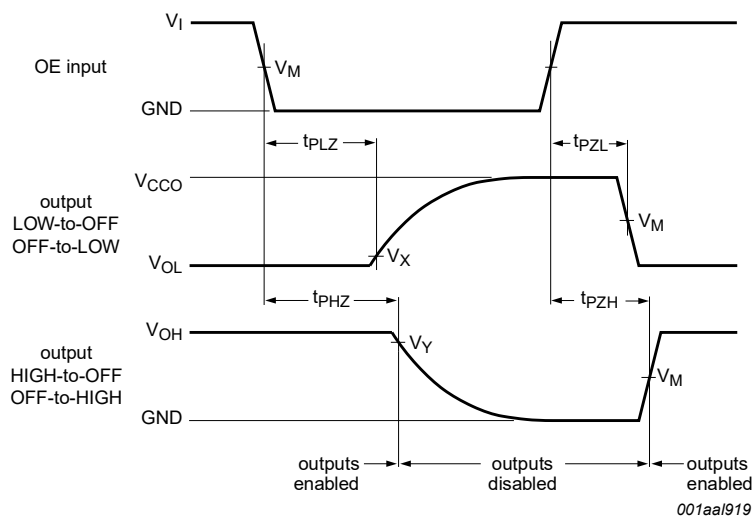
Table 12. Measurement points

$V_{CCI}$  is the supply voltage associated with the input and  $V_{CCO}$  is the supply voltage associated with the output.

Supply voltage	Input <sup>[1]</sup>	Output <sup>[2]</sup>		
$V_{CCO}$	$V_M$	$V_M$	$V_X$	$V_Y$
$0.8V \pm 10\%$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.08V$	$V_{OH} - 0.08V$
$1.0V \pm 10\%$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.10V$	$V_{OH} - 0.10V$
$1.2V \pm 10\%$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.12V$	$V_{OH} - 0.12V$
$1.8V \pm 10\%$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.18V$	$V_{OH} - 0.18V$

[1]  $V_{CCI}$  is the supply voltage associated with the input.

[2]  $V_{CCO}$  is the supply voltage associated with the output.



Measurement points are given in [Table 12](#)

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Figure 4. Enable and disable times

Dual bidirectional I3C-bus, 1:2 and 2:1 switch, and voltage level translator

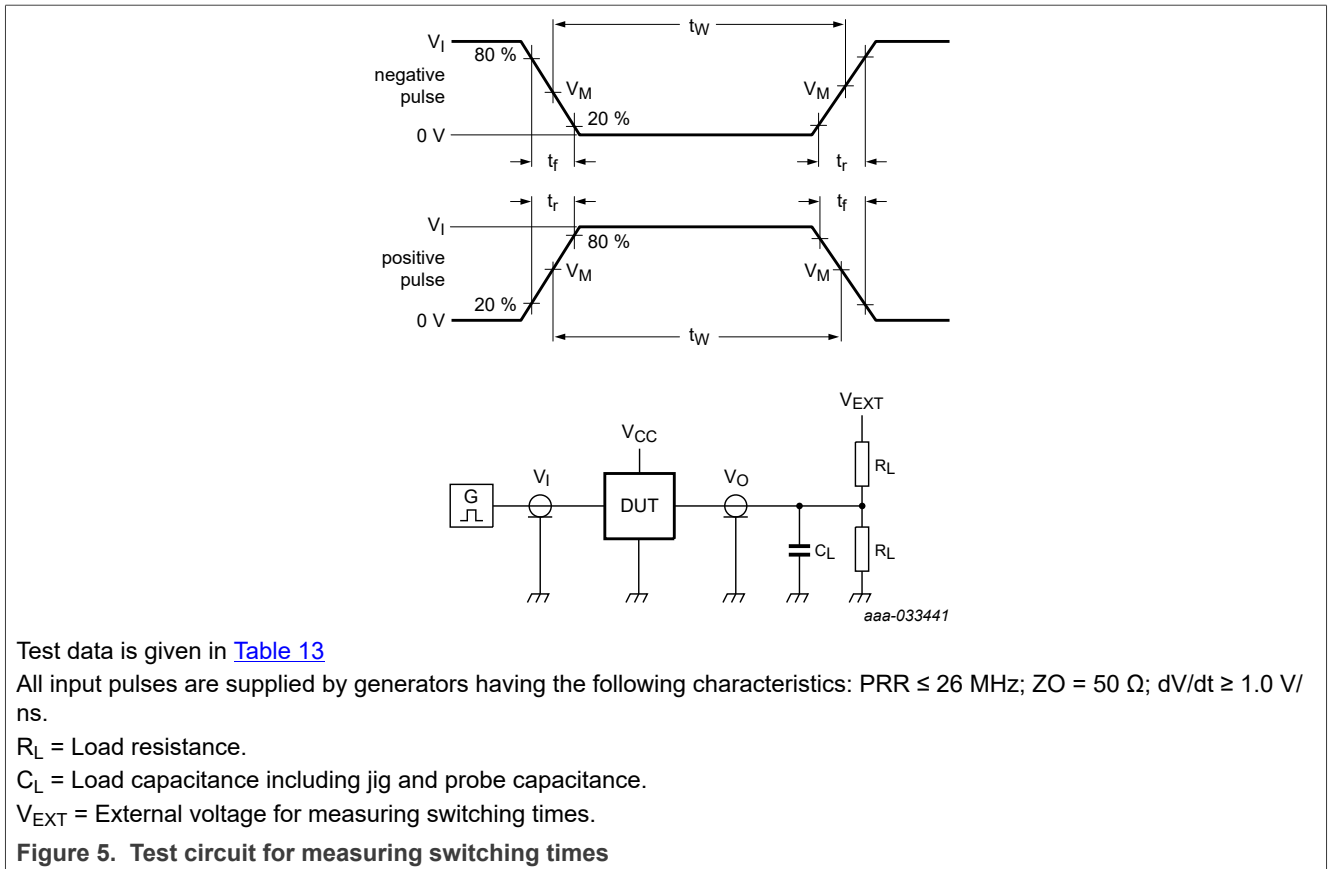


Table 13. Test data

Supply voltage (V <sub>CCR</sub> = 1.62 V to 3.6 V)			Input		Load		V <sub>EXT</sub>		
V <sub>CCP1</sub>	V <sub>CCP2</sub>	V <sub>CCS</sub>	V <sub>I</sub>	Δt/ΔV	C <sub>L</sub> <sup>[1]</sup>	R <sub>L</sub> <sup>[2]</sup>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
0.72 to V <sub>CCR</sub>	0.72 to V <sub>CCR</sub>	0.72 to V <sub>CCR</sub>	V <sub>CCI</sub> <sup>[3]</sup>	≤ 1.0 ns/V	68 pF	50 kΩ, 1 MΩ	open	open	2V <sub>CCO</sub> <sup>[4]</sup>

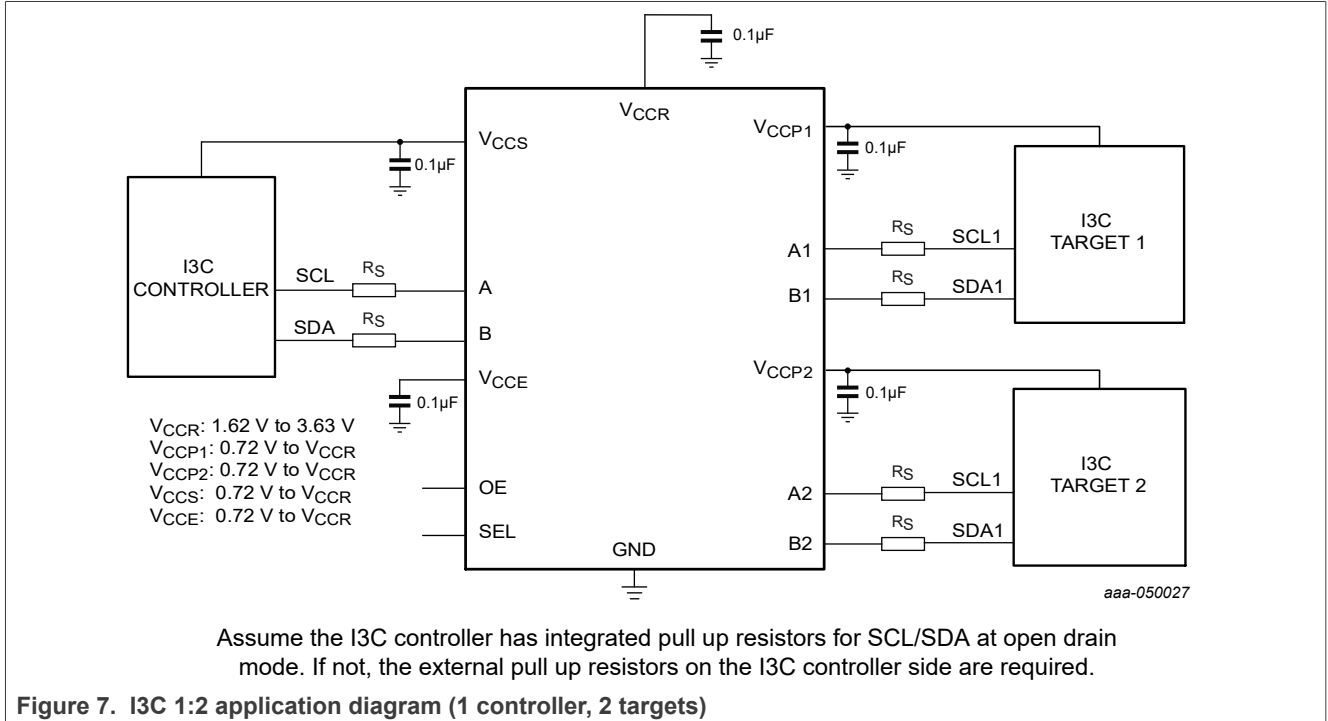
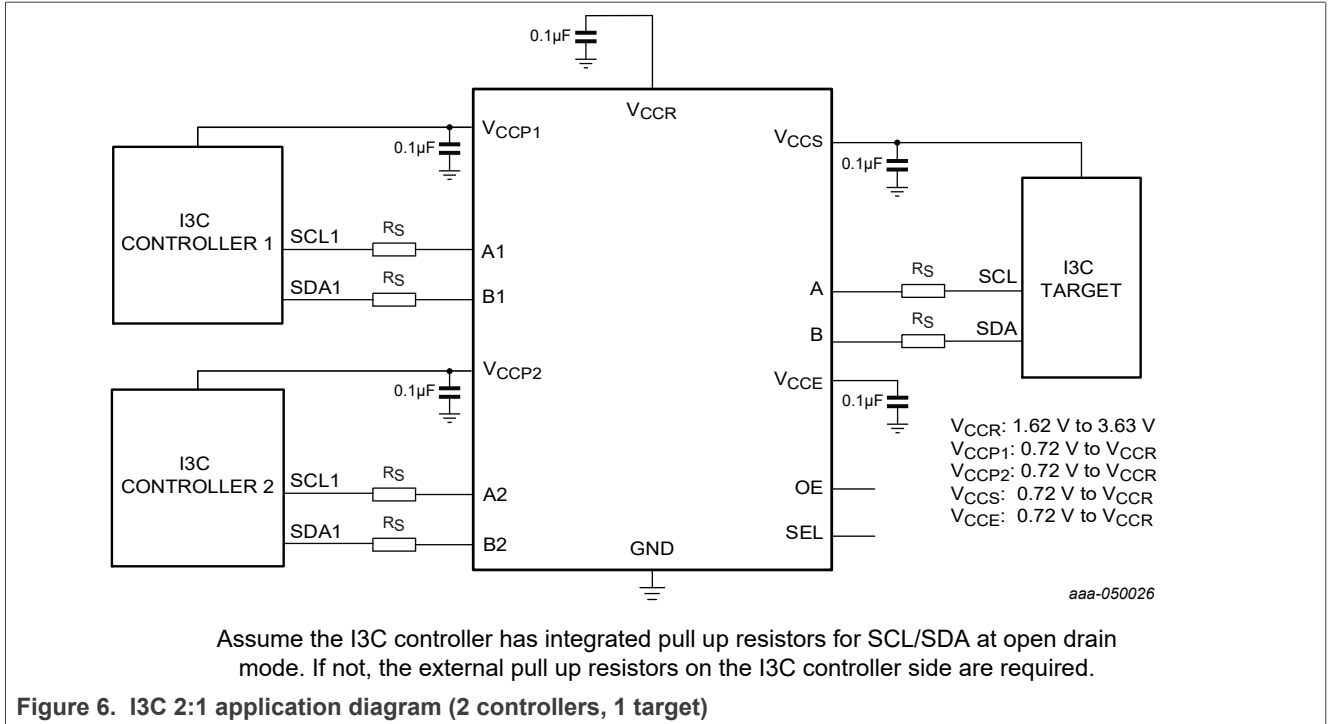
- [1] Different C<sub>L</sub> values are specified in [Dynamic characteristics](#).
- [2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R<sub>L</sub> = 1 MΩ; for measuring enable and disable times, R<sub>L</sub> = 50 kΩ.
- [3] V<sub>CCI</sub> is the supply voltage associated with the input.
- [4] V<sub>CCO</sub> is the supply voltage associated with the output.

### 13 Application information

The P3S0210BQ can be used to interface between two I3C controllers to one target or one I3C controller to two targets at different supply voltages on port 1, port 2 and port S.

A series resistor R<sub>s</sub> on each I/O pin is required to reduce the overshoot/undershoot. The recommended value is 30 Ω. Adjust the R<sub>s</sub> value for optimized signal integrity is needed with different wire lengths, parasitic inductance and capacitance. Please ensure the R<sub>s</sub> should not be too high to affect the V<sub>OL</sub> level.

See [Figure 6](#) and [Figure 7](#) for I3C and [Figure 8](#) and [Figure 9](#) for I<sup>2</sup>C typical operating circuit.



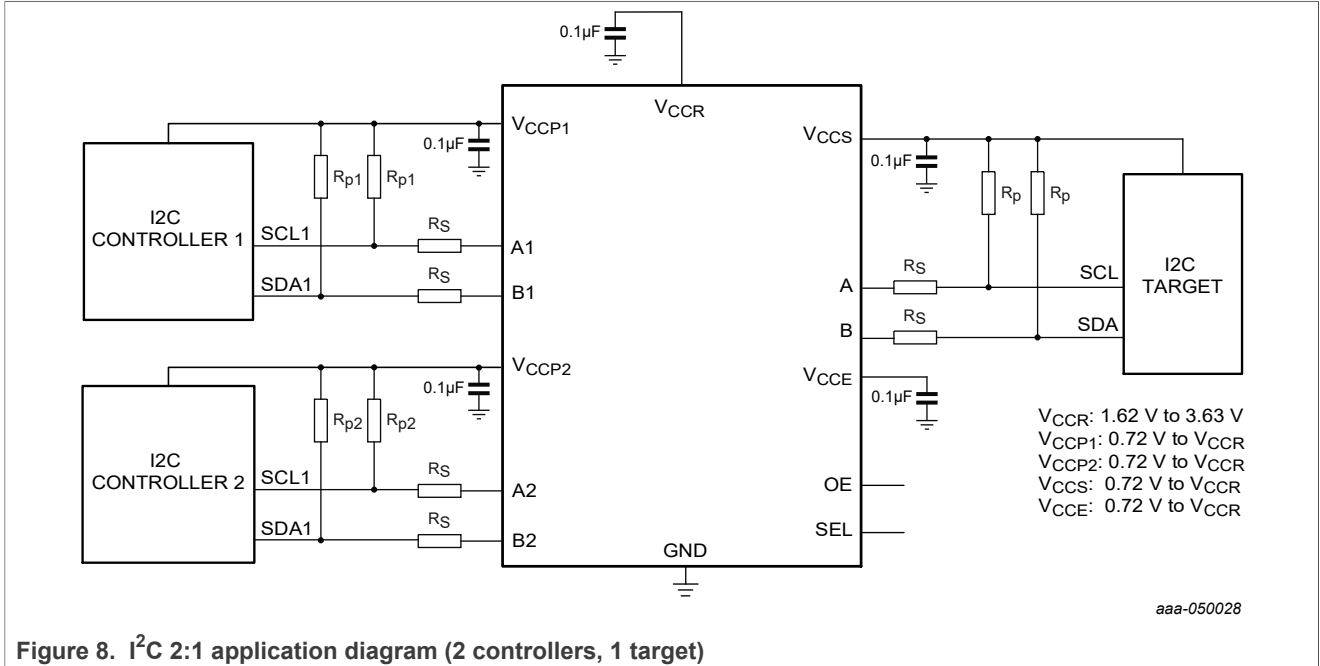


Figure 8. I<sup>2</sup>C 2:1 application diagram (2 controllers, 1 target)

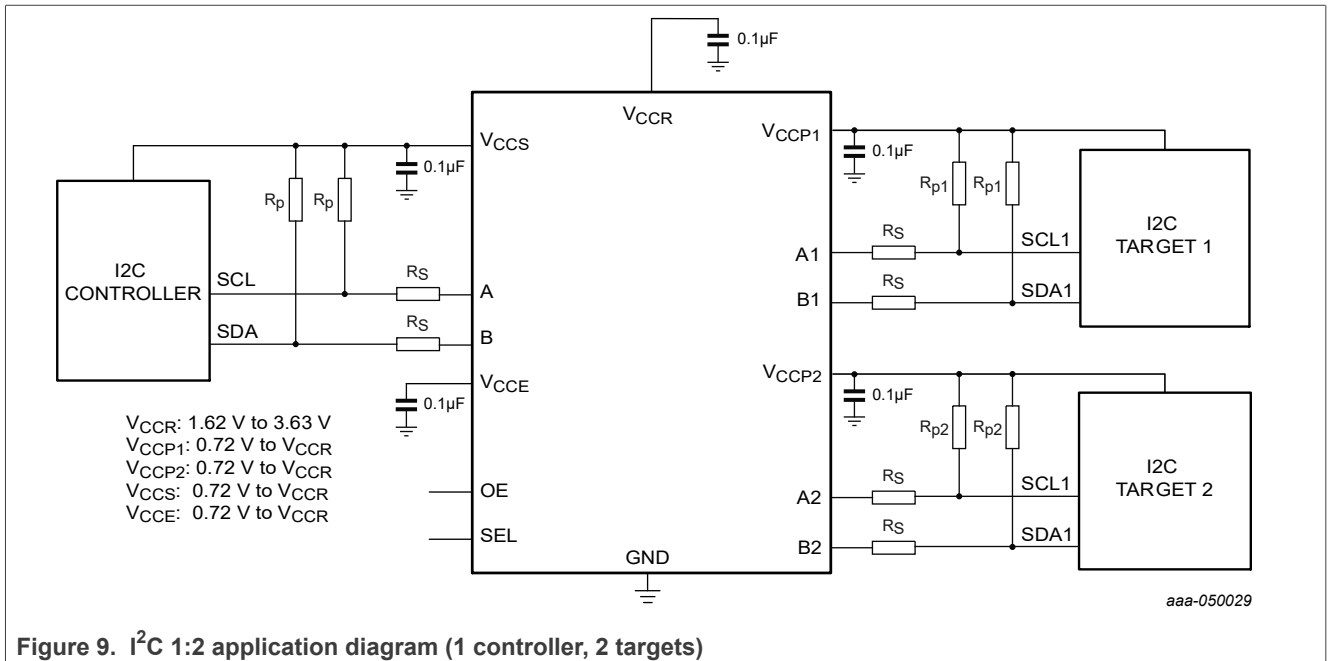


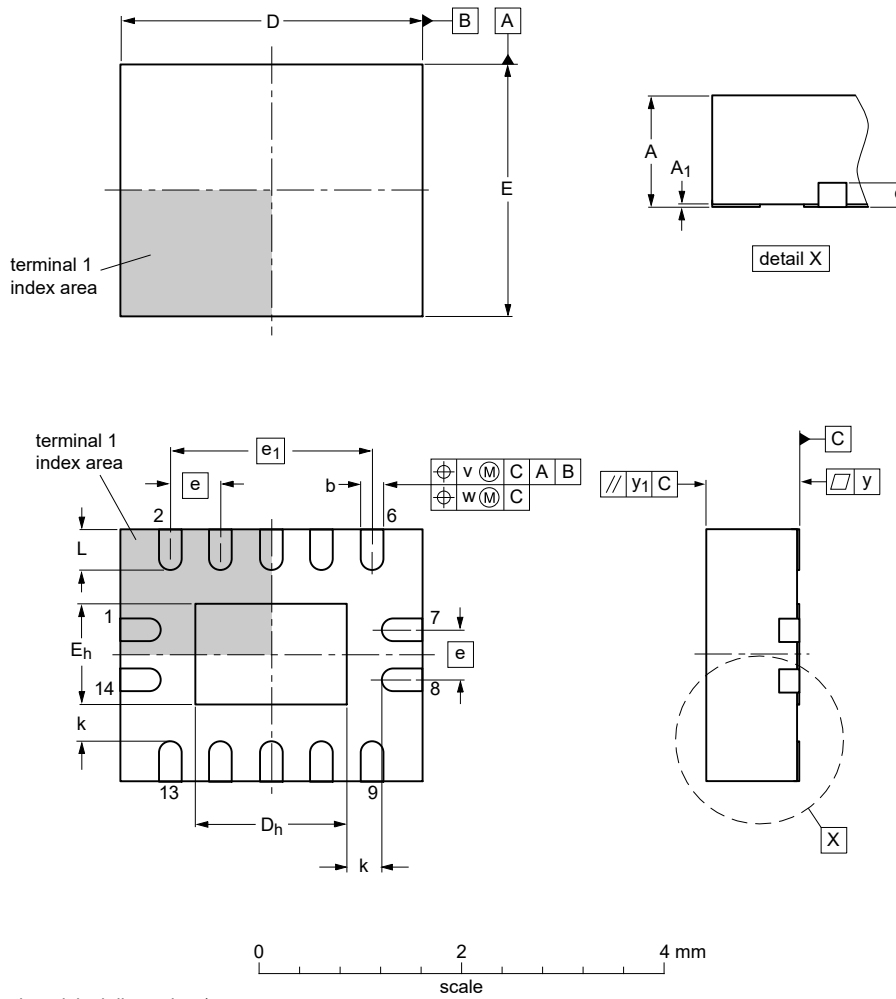
Figure 9. I<sup>2</sup>C 1:2 application diagram (1 controller, 2 targets)



14 Package outline

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	k	L	v	w	y	y <sub>1</sub>
max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT762-1	MO-241				15-04-10 15-05-05

Figure 10. Package outline DHVQFN14 (SOT762-1)

## 15 Soldering PCB footprints

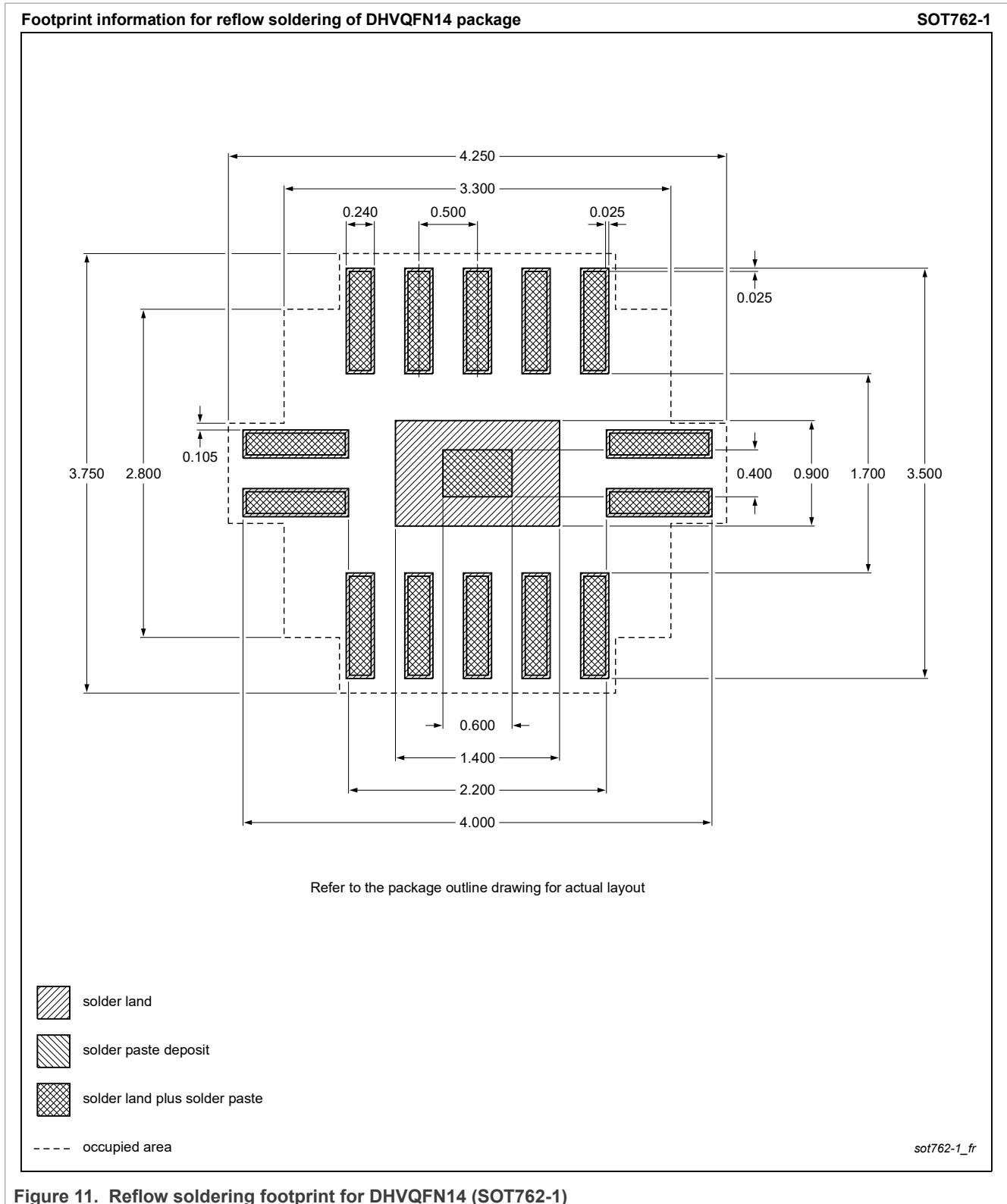


Figure 11. Reflow soldering footprint for DHVQFN14 (SOT762-1)

## 16 Revision history

Table 14. Revision history

Document ID	Release date	Description
P3S0210BQ v.1.0	15 December 2023	• Initial version

## Legal information

### Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

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## Dual bidirectional I3C-bus, 1:2 and 2:1 switch, and voltage level translator

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